Transformer-less High Gain Three-Port Converter with Low Voltage Stress and Reduced Switches for Standalone PV Systems

Ling Qin, *Member, IEEE,* Tianhong Qian, John Long Soon, *Member, IEEE,* Waqas Hassan, *Member, IEEE,* Min Tian, Lei Zhou, Lei Ren

***Abstract*—This paper proposes a high gain transformer-less three-port converter (TPC) for standalone photovoltaic (PV) systems. The TPC is designed and developed based on a dual-inductor high gain two-port converter by utilizing one of the buffer capacitors to derive the third part for PV input. A hybrid pulse frequency modulation (PFM) scheme unified with a pulse width modulation (PWM) control strategy is adopted, which realizes the maximum power point tracking (MPPT) control, load voltage regulation, and bidirectional energy flow at the battery port. The proposed TPC offers the unique advantages of high voltage gain, continuous battery port current, reduced power semiconductors, lower voltage stresses, the common ground shared by all ports, low-cost gate driver, and small size of the rear-end inductor. The working principle, steady-state characteristics, small signal models and control method, including design conditions, are comprehensively analyzed. The correctness of the theoretical analysis is verified by developing a 300W experimental prototype, which shows the maximum efficiency is 97.7%.**

***Index Terms*—Three-port converter, photovoltaic (PV), standalone, PWM+PFM, high gain.**

I. Introduction

STANDALONE photovoltaic (PV) power generation systems have been widely used in rural and remote areas where utility power is unavailable to provide access to electricity to end-users [1]. Standalone PV systems are frequently equipped with batteries storages and regulate energy due to the intermittent and randomness of PV output to provide continuous and stable power to various DC loads, including inverters [2]. A unidirectional converter and a bidirectional converter are required to balance the voltage levels of PV cells, batteries, and the load. These two converters can achieve the maximum power point tracking (MPPT) control of PV cells and constant load voltage control. The advantage of this architecture is easy implementation and greater control flexibility. However, the higher number of devices leads to a larger size, higher cost, and lower efficiency [3].

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L. Qin, T. Qian, M. Tian, L. Zhou and L. Ren are with the Department of Electrical Engineering, Nantong University, Nantong 226019, China (e-mail: qin.l@ntu.edu.cn; qiantianhong007@sina.com; tmjsnt@foxmail.com; zhoulei_1996@163.com; renleinuaa@163.com.)

J. L. Soon is with the School of Electrical and Information Technologies, University of Sydney, Australia. (e-mail: jsoo3118@uni.sydney.edu.au).

W. Hassan is with the School of Engineering, University of Tasmania, Tasmania, Australia (e-mails: waqas.hassan@utas.edu.au).

To mitigate the aforementioned issues, the two-port dc-dc converters can be substituted by a three-port converter (TPC) with at least one bidirectional current path. TPCs offer voltage control and power management of each port with a lower component count, thus effectively reducing the volume and cost of the system [4]. In general, to further reduce the cost and improve the conversion efficiency, power density and reliability, TPCs for standalone PV systems should optimally satisfy the following performance requirements:

- The continuous battery current with low current ripple to reduce the requirements of battery port filter [5];
- The high voltage boosting capability without extreme duty cycle operation to integrate battery with low input voltage (48V) to dc buses or loads with high voltage, typically (300V-400V) [6];
- The MPPT control of PV port and constant voltage control of load port [7];
- Typical operation modes, including dual-input single-output (DISO) and single-input dual-output (SIDO) to overcome the intermittence of PV output power;
- The number of components and the independent power supplies for the driving circuits as small as possible;
- Reduced voltage stress to leverage the low rated voltage power semiconductors with lower on-state resistance or forward voltage drop;
- Soft switching ability to reduce the power loss at higher switching frequency for the requirements of miniaturization and high conversion efficiency;
- A common ground for all ports to reduce the complexity of sampling and control circuits and improve electromagnetic interference (EMI) characteristics [5].

Several TPC solutions with transformers, including the coupled inductor [6, 8-11], and transformers-less structures [12]-[24], have been proposed in the literature for standalone PV systems. The transformer-less TPCs usually have advantages of smaller volume, fewer components, lower cost, easier control and parameters design, and higher conversion efficiency [2]. Moreover, the voltage spikes and EMI problems caused by leakage inductance discharge of high-frequency transformers are also eliminated [3]. Hence, the transformer-less TPCs show better characteristics for applications without electrical isolation or extremely high voltage gain requirements [8].

By introducing a storage-switch-diode cell into the two-switch buck-boost converter, a family of wide operation range

transformer-less TPCs with variable structures can be derived [12]. These variable structure TPCs can be compact, benefiting from only one inductor. Inspired by this method, a simple systematic approach for deriving transformer-less TPCs with low cost and compact structure from two-port converters is introduced [13]. However, an additional switch and diode are mandatory for this type of TPCs to embed the battery port with a floating ground and pulsating current. To account for a small internal resistance of the battery, large electrolytic capacitors are usually needed to avoid the impact of excessive current ripple on the lifespan of the battery [5]. The capacitance of electrolytic capacitors in PV power generation systems is prone to drop under high-temperature conditions [25], resulting in decreased system reliability.

TPCs can also be derived by sharing the magnetic elements or semiconductor devices in different two-port converters. The transformer-less integrated TPC in [14] can reduce the number of inductors and relieve voltage stress. Nevertheless, two additional diodes are introduced, the ground is floating, the current of the battery port is pulsating, and the floating gate drivers are essential for all switches. Most of these issues can also be observed in the pulse-width-modulation (PWM) plus pulse-frequency-modulation (PFM) single-switch integrated TPC [15]. In [16], an integrated TPC is developed without introducing any additional semiconductor. However, a new inductor is added to the battery port to ensure the continuous current. Ten viable triple-switch dual-inductor TPCs are derived from a programmable topology derivation method [17]. Although the power of all ports can bidirectionally flow, at least one port has floating ground. In the integrated TPC in [18], the PV cells and battery cannot provide power to the load simultaneously, and the current spike caused by the buffer capacitor charging results in considerable conduction loss.

A TPC presented in [19] offers a reconfigurable structure and more flexible power flow to integrate regenerative loads into a dc microgrid; however, the voltage stress on devices is high, resulting in low efficiency. A family of multiport buck-boost converters is derived based on the dc-link inductors concept in [20]. This method eliminates the bulky dc-link capacitor requirement, reducing size and cost. Another family of nonisolated TPC based on dual-input converters (DIC) and dual-output converters (DOC) is derived in [21], which features single-stage power conversion, resulting in high integration and high efficiency. However, all the derivatives of [20], [21] suffer discontinuous battery port current.

Furthermore, the transformer-less TPCs proposed in [11]-[21] have the common drawbacks of low voltage gain, high voltage stress and hard switching operation. In [22] and [23], the reported TPCs can achieve soft switching of all semiconductors. In [24], a stacked TPC based on a buck/boost converter is proposed. It has high voltage gain and low voltage stress and realizes ZVS of all switches. However, the number of switches is high (four), and only one switch driving circuit shares the ground with the three ports.

In this paper, a novel transformers-less high-gain TPC is derived from the dual-inductor high-gain converter in [26], as shown in Fig. 1(a), using one of the buffer capacitors as the third port (PV port). Furthermore, an additional diode is connected in series with the rear-end inductor, and the diode directly connected to the main power switch is replaced with a synchronous switch. The front-end and rear-end inductors work in continuous conduction mode (CCM) and discontinuous conduction mode (DCM), respectively. Hence, the PWM pulse PFM hybrid modulation strategy [15] can be utilized to realize the MPPT control and load voltage regulation. The main merits of the proposed TPC are as follows: i) all ports share a common ground; ii) the battery port current is continuous; iii) the count of semiconductors is reduced (two switches and two diodes); iv) the voltage stresses across all the power components are almost half of the load port voltage; v) the voltage gain is almost twice that of the conventional boost converter; vi) the ZVS of one switch and the natural turn-off of one diode can be realized; vii) two switches form a bridge leg and work complementary, hence any commercial bootstrap drivers integrated circuit (IC) chips can be chosen; viii) the size of the rear-end inductor is very small due to the DCM operation and the low average current.

This paper is organized as follows. Section II presents the derivation process of the proposed transformer-less high-gain TPC. The working principle and steady-state characteristics are analyzed in Sections III and IV, respectively. Subsequently, the TPC control method and implementation conditions are discussed in Section V. The small signal models are established in Section VI. The parameters design process is given in Section VII. Section VIII deals with experimental validation of the designed TPC. Finally, concluding remarks are provided in Section IX.

II. TOPOLOGY DERIVATION OF PROPOSED HIGH GAIN TPC

Fig. 1(a) shows the dual-inductor single-switch high gain boost converter reported in [26]. Compared to the counterparts such as the conventional switched inductor boost converter and the quadratic boost converter, the converter in Fig. 1(a) has fewer diodes and lower voltage stress. This paper proposes a high gain TPC capable of achieving the bidirectional energy flow based on existing topology by adding a minimum component, as highlighted in Fig. 1(b). The battery source is connected at the input port, and the terminals of the buffer capacitors C_2 can be used as the PV port. The load is connected to the output port. Meanwhile, the freewheeling diode D_2 is replaced with a synchronous switch S_2. Thus, the proposed TPC is able to switch the configuration to charge the battery by controlling the S_2 and S_1 to operate as buck converter mode based on the PV port, as shown in Fig. 1(b). Therefore, when the battery is discharged to the load, the proposed TPC can be operated as a boost converter by utilizing the S_1 and S_2 to step up the output voltage. The proposed TPC can partly achieve ZVS since its body diode is forced on before the main switch is turned on. Since the MOSFETs S_1 and S_2 are switching complementary, only the duty cycle (d) of S_1 can be used as a control degree of freedom. However, two control objectives need to be achieved in the proposed TPC: the load voltage regulation and the MPPT. Thus, another control variable is required. If the front-end inductor L_1 is

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operated in CCM, and the rear-end inductor L_2 is connected with a blocking diode D_1 and operated in DCM, then the voltage gain of the proposed TPC is closely related to the switching frequency f_s. Consequently, f_s can be used as the second degree of control freedom. Therefore, the PWM+PFM method can be adopted for the proposed TPC, where d realizes the load voltage regulation and f_s is controlled to implement the MPPT operation for the PV cells.

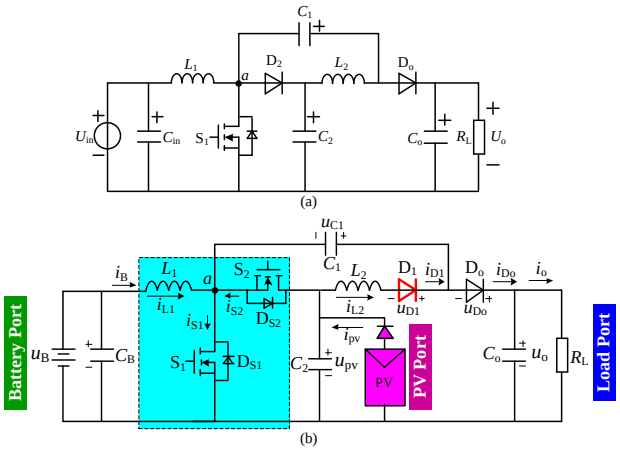

Fig. 1. Topological evolution of the proposed high-gain TPC. (a) the dual-inductor high-gain boost converter in [26]. (b) the proposed high-gain TPC.

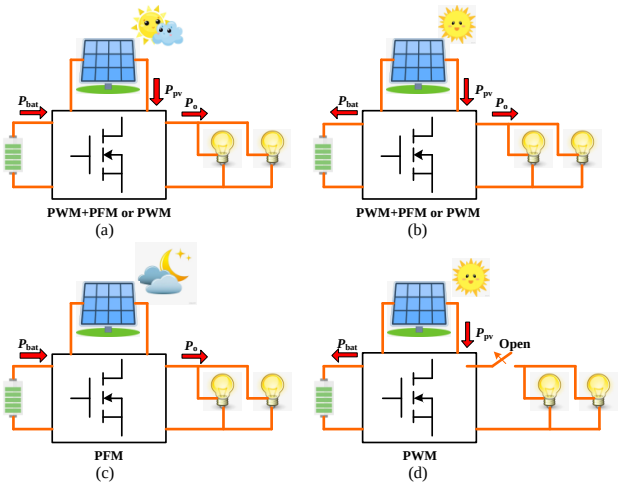

Fig. 2. Operation modes. (a) DISO. (b) SIDO. (c) SISO I. (d) SISO II.

III. OPERATION PRINCIPLE ANALYSIS

The proposed high gain TPC consists of four main operation modes: DISO, SIDO, SISO I and SISO II, as shown in Fig. 2. The micro-controller automatically configures various operation modes depending on weather and daylight conditions.

Fig. 2(a) shows the applications where the PV panel is under partial shading due to the cloudy weather and the load demands more energy to support. In this case, the DISO mode is activated by utilizing the battery storage along with the PV panel to provide sufficient output power P_o. The sum of power P_{pv} and P_{bat} flows to the load, as indicated in Fig. 2(a).

Fig. 2(b) shows that the intensity of sunlight is strong, and PV is under full power conditions. In this case, the PV cells generate sufficient energy to support the battery charging and load application simultaneously; thus, TPC operates in the SIDO mode. The flow of P_{pv} and P_{bat} is shown in Fig. 2(b).

Fig. 2(c) shows the scenarios when PV panels are completely shut down at night. In this case, the TPC operates in SISO I mode by utilizing the battery source as backup storage in order to provide sufficient output power P_o. The unidirectional power flow, P_{bat} to the load, is shown in Fig. 2(c).

Fig. 2(d) shows the proposed TPC enters the SISO II mode when the PV power P_{pv} sufficiently support the battery charging with no load condition, analogous to the case of Fig. 2(b).

The proposed TPC shows five stages under steady-state operation in DISO mode. The operating principle in other modes is analogous. The equivalent circuit operation in each stage is shown in Fig. 3. The key waveforms are illustrated in Fig. 4.

Stage 1 [t_0, t_1]: This stage begins from t_0 when S_1 is turned on, as shown in Fig. 3(a). D_o and D_{S2} (body diode of S_2) are reverse biased, and the diode D_1 is forward biased. Meanwhile, the inductor currents i_{L1} and i_{L2} increase linearly, which can be expressed as

$$i_{L1}(t)=\frac{U_B}{L_1}(t-t_0)+i_{L1}(t_0) \tag{1}$$

$$i_{L2}(t)=\frac{U_{pv}-U_{C1}}{L_2}(t-t_0)+i_{L2}(t_0) \tag{2}$$

where U_B and U_{pv} are the average voltage of battery port and PV port, respectively, and U_{C1} is the average voltage across the capacitor C_1.

Until t_1, S_1 is turned off and stage 1 ends. The duration of stage 1 is expressed as

$$\Delta t_1 = t_1 - t_0 = dT_s \tag{3}$$

where d is the duty cycle of S_1 and T_S is the switching period.

Stage 2 [t_1, t_2]: At the time t_1, as shown in Fig. 3(b), i_{L1} and part of i_{L2} flow into the node a, and D_{S2} is forward biased. Meanwhile, both i_{L1} and i_{L2} decrease linearly, which can be expressed as

$$i_{L1}(t)=-\frac{U_{pv}-U_B}{L_1}(t-t_1)+i_{L1}(t_1) \tag{4}$$

$$i_{L2}(t)=-\frac{U_o-U_{pv}}{L_2}(t-t_1)+i_{L2}(t_1) \tag{5}$$

where U_o is the average voltage of the load port.

At time t_2, S_2 is ZVS turned on and the body diode D_{S2} is naturally turned off at the end of stage 2. The duration of stage 2 is $\Delta t_2=t_2-t_1=T_d$, where T_d is the dead time.

Stage 3 [t_2, t_3]: In stage 3, as shown in Fig. 3(c), the inductor currents i_{L1} and i_{L2} keep the same changing slope as those in stage 2. At time t_3, i_{L2} decreases to zero, and D_1 turns off naturally and stage 3 ends. The duration of stage 3 can be expressed as

$$\Delta t_3 = t_3 - t_2=d_1T_s \tag{6}$$

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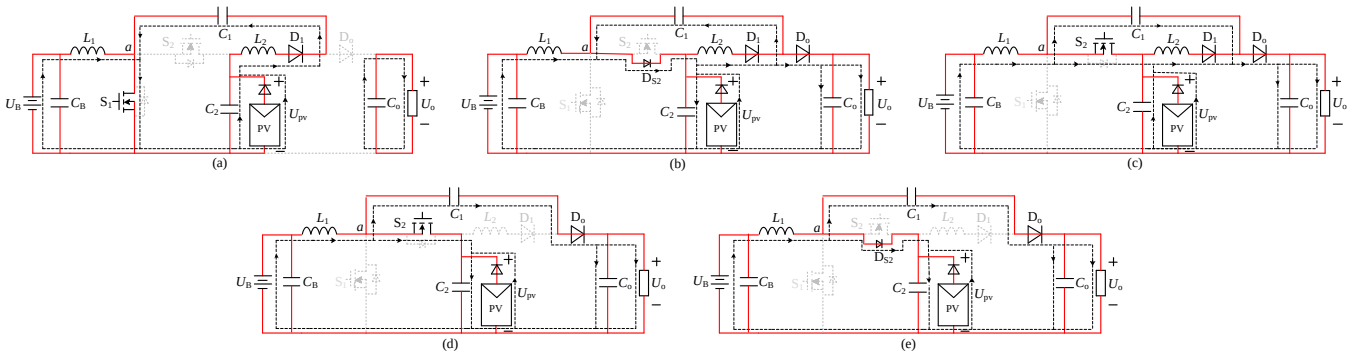

Fig. 3. Equivalent circuit in each stage in DISO mode. (a) stage 1 [t_0, t_1]. (b) stage 2 [t_1, t_2]. (c) stage 3 [t_2, t_3]. (d) stage 4 [t_3, t_4]. (e) stage 5 [t_4, t_5].

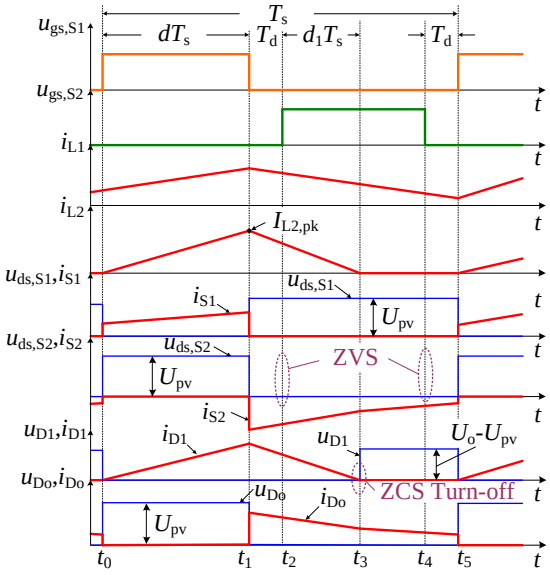

Fig. 4. Key waveforms during one switching period in DISO mode.

where d_1 is the ratio of Δt_3 to the switching period T_s.

Stage 4 [t_3, t_4]: In this stage, as illustrated in Fig. 3(d), i_{L1} keeps the same changing slope as that in stage 2. At time t_4, S_2 is turned off and D_{S2} is forward biased, and stage 4 ends. During the turn off of S_2, the current follows through the body diode D_{S2}, hence the voltage across the switch S_2 is clamped at zero; thus, its turn-off switching loss can be neglected.

Stage 5 [t_4, t_5]: In this stage, as shown in Fig. 3(e), i_{L1} keeps the same changing slope as that in stage 2. At time t_5, S_1 is turned on and diodes D_{S2} and D_o are forced off. Stage 5 ends at this time and the next period begins. The duration of stage 5 is Δt_5=t_5-t_4=T_d.

The operation of the proposed TPC in SIDO mode is analogous to DISO mode, except that the highlighted circuit works as a synchronous buck, and S_1 achieves ZVS while S_2 operates under hard-switching conditions. The SISO I mode can be seen as the particular case of the DISO mode that the current of the PV port is zero. Hence, the operation in both SIDO mode and SISO I mode is not described here. In SISO II mode, the load current of the proposed TPC is zero, and its operation in a switching period can be divided into four stages. The equivalent circuit corresponding to each stage is shown in Fig. 5. It can be seen that its working principle is the same as the conventional bidirectional buck/boost converter, which is not repeated in this paper.

IV. STEADY-STATE CHARACTERISTICS

A. Voltage and Current Characteristics

By applying the volt-second balance on L_1 and L_2, the following relationship can be obtained as

$$\begin{cases} dU_B T_s = (1-d)\left(U_{pv} - U_B\right) T_s \\ d\left(U_{pv} - U_{C1}\right) T_s = d_1 U_{C1} T_s \end{cases} \tag{7}$$

where the dead time T_d is ignored. In addition, it can be obtained from Fig. 3(c) that

$$U_{pv} + U_{C1} = U_o \tag{8}$$

Then, the voltage relationship between the three ports can be derived as

$$\begin{cases} U_{pv} = \frac{1}{1-d} U_B \\ U_o = \frac{2d+d_1}{d+d_1} U_{pv} < 2U_{pv} \end{cases} \tag{9}$$

The voltage gain is defined by U_o/min(U_B, U_{pv}), where min(U_B, U_{pv}) represents the smaller of the two values. Since U_{pv}>U_B in the proposed TPC, the ideal voltage gain can be obtained as

$$G_1 = \frac{U_o}{U_B} = \frac{2d + d_1}{(1-d)(d+d_1)} \tag{10}$$

Since 0<d_1<(1-d), the following can be written as

$$\frac{1+d}{1-d} < G_1 < \frac{2}{1-d} \tag{11}$$

According to the power conservation theorem, the current relationship between the three ports can be further derived as

$$I_o = \frac{d+d_1}{2d+d_1} I_{pv} + \frac{(1-d)(d+d_1)}{2d+d_1} I_B \tag{12}$$

where I_o is the average load current, I_{pv} and I_B are the average output current of PV cells and the average current of batteries, respectively.

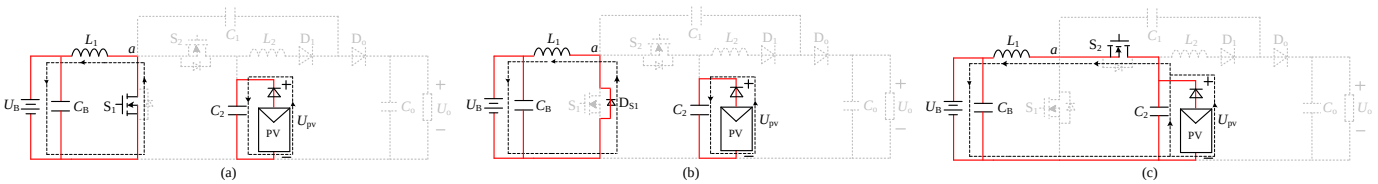

Fig. 5. Equivalent circuit in each stage in SISO II mode. (a) stage 1 [t_0, t_1]. (b) stage 2 [t_1, t_2] and stage 4 [t_3, t_4]. (c) stage 3 [t_2, t_3].

B. Voltage Stress

In the proposed TPC, the voltage stresses across S_1, S_2, D_1 and D_o can be expressed as

$$\begin{cases} U_{S1} = U_{S2}{=}U_{Do} = U_{pv} = \frac{d+d_1}{2d+d_1}U_o \in (\frac{1}{2}U_o, \frac{U_B+U_o}{2}) \\ U_{D1} = U_o - U_{pv} = \frac{d}{2d+d_1}U_o < \frac{1}{2}U_o \end{cases} \tag{13}$$

The voltage stress across each capacitor can be expressed as

$$\begin{cases} U_{C1} = \frac{d}{2d+d_1}U_o < \frac{1}{2}U_o \\ U_{C2} = \frac{d+d_1}{2d+d_1}U_o \in (\frac{1}{2}U_o, \frac{U_B+U_o}{2}) \\ U_{Co} = U_o \end{cases} \tag{14}$$

C. Current Stress

The inductor L_2 works in DCM, and its current peak can be expressed as

$$I_{L2,pk} = \frac{d(2U_{pv} - U_o)}{L_2 f_s} \tag{15}$$

The average current through L_2 is obtained as

$$I_{L2} = I_o = \frac{I_{L2,pk}(d+d_1)}{2} = \frac{d(2U_{pv} - U_o)(d+d_1)}{2L_2 f_s} \tag{16}$$

The RMS currents of L_1 and L_2 can be respectively expressed as

$$\begin{cases} I_{rms,L1} = \sqrt{I_{L1}^2 + \frac{\Delta I_{L1}^2}{12}} \\ I_{rms,L2} = \sqrt{\frac{d+d_1}{3}}I_{L2,pk} \end{cases} \tag{17}$$

where ΔI_{L1} is the peak-to-peak value of inductor current i_{L1}.

The RMS values of the currents through S_1 and S_2 are obtained as

$$\begin{cases} I_{rms,S1} = \sqrt{\left[\frac{(\Delta I_{L1}+I_{L2,pk})^2}{12} + \left(I_{L1} + \frac{I_{L2,pk}}{2}\right)^2\right]d} \\ I_{rms,S2} \approx \sqrt{\left[\frac{(\Delta I_{L1}+I_{L2,pk})^2}{12} + \left(I_{L1} - \frac{I_{L2,pk}}{2}\right)^2\right](1-d)} \end{cases} \tag{18}$$

The average currents through D_1 and D_o are expressed as

$$I_{D1} = I_{Do} = I_o \tag{19}$$

D. Performance Comparison

The proposed TPC is compared with other transformer-less TPCs [12, 14-16, 18-24] suitable for standalone PV systems. Fig. 6 shows the ideal voltage gain characteristics of these TPC topologies. As can be seen, similar to the TPC in [24], the proposed TPC shows the advantages of higher voltage gain, lower voltage stress, soft switching ability, common ground for all three ports, continuous and bidirectional battery current, and fewer power semiconductors, when compared to many other TPCs.

Since the TPCs proposed in this paper and [24] show many common advantages, Table II further shows the count of bootstrap drivers, the control strategies, the circulating current, and the operation region of the two TPCs under the same conditions. As can be seen, all switches of the TPC in [24] can realize soft-switching, hence the switching frequency can be set higher to optimize the sizes of the passive components. In addition, the PWM+PSM method adopted in [24] can realize the decoupling control of each port voltage in a wider range; however the inherent circulation current poses challenges to achieve soft-switching within the entire working range. Hence, GaN switches with higher costs are essential to achieve high conversion efficiency. Moreover, the TPC in [24] contains four switches and requires one more bootstrap driver than the proposed TPC. Therefore, the proposed TPC offers advantages in terms of cost and converter design. Although one switch and one diode of the proposed TPC are operated in a hard switching condition, the power losses of these two semiconductors are relatively low due to the reduced voltage stress. Hence, the proposed TPC also obtained high conversion efficiency, which is experimentally validated in Section VIII.

E. Analysis of Non-ideal Parameters of the Proposed TPC

1) Impact on voltage gain: The parasitics of components, such as resistors of inductors and MOSFETs and the forward voltages of diodes, can degrade the voltage gain and the conversion efficiency. According to the volt-second balance of L_1 and L_2, the practical voltage gain G_2=U_o/U_B of the proposed TPC with component parasitics is obtained as follows

$$\begin{cases} U_B = AE + (AC + B + C)(\frac{d}{A} + \frac{d}{d_1+d}) + B + C \\ d_1 = \frac{\sqrt{[d^2(E-C)-F]^2+8d^2F(E-C)}-[d^2(E-C)-F]}{2d(E-C)} \end{cases} \tag{20}$$

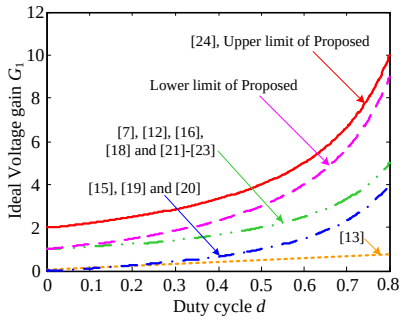

Fig. 6. The curves of ideal voltage gain G_1 versus duty cycle d.

TABLE I
PERFORMANCE COMPARISON OF THE PROPOSED TPC WITH OTHER TRANSFORMER-LESS TPCS SUITABLE FOR STANDALONE PV SYSTEM

Ref.	Device count S	D	L	C	Voltage stress on switches	Voltage gain	Switching technique	Common ground	Battery current	$U_B/U_{pv}/U_o$ (V)	Power/switching frequency/maximum efficiency
[12]	3	3	1	0	U_{pv},U_b,U_b-U_o	≤1/(1-d)	Hard	Two ports	Pulsating	36/10-50/24	120W/20kHz/95.0%
[14]	3	3	1	0	U_{pv},U_b, U_b	d	Hard	No	Pulsating	250/380/200	500W/70kHz/98.4%
[15]	1	4	2	0	U_{pv}+U_b+U_o	d/(1-d)	Hard	No	Pulsating	12/16.8/17	24W/>20kHz/92%
[16]	3	1	3	1	U_o	1/(1-d)	1 S (ZVS)	Yes	Continuous	70/80/100	1.2kW/100kHz/97%
[18]	3	1	2	1	U_o	1/(1-d)	2 S (ZVS)	Yes	Continuous	24/60/48	240W/100kHz/97.3%
[19]	4	5	1	0	U_b,U_o,U_b,U_o-U_{pv}	d/(1-d)	Hard	Yes	Pulsating	36/17/24	50W/20kHz/93%
[20]	6	0	3	0	U_{pv},U_b,U_o	d/(1-d)	3 S (ZVS)	Yes	Pulsating	90-110	1000W/100kHz/97.8%
[21]	3	3	1	0	U_o,U_o-U_b,U_b-U_{pv}	≈1/(1-d)	Hard	Yes	Pulsating	100/70/100	500W/100kHz/98%
[22]	3	1	2	0	U_o,U_o,U_o-U_b	1/(1-d)	3 S (ZVS) 1 D (ZCS)	Two ports	Pulsating	48/40/220	200W/50kHz/96.0%
[23]	2	1	2	0	U_o	≈1/(1-d)	2 S (ZVS) 1 D (ZCS)	Yes	Continuous	48/<48/170	250W/ Not given/97.1%
[24]	4	0	2	1	U_o/2	2/(1-d)	4 S (ZVS)	Yes	Continuous	60/<200/400	1kW/100kHz/97.7%
Proposed	2	2	2	1	(13)	(11)	1 S (ZVS) 1 D (ZCS)	Yes	Continuous	48/160/300	300W/56k-168kHz/97.7%

TABLE II
COMPARISON BETWEEN TWO TPCS PROPOSED IN THIS PAPER AND [24]

Performances	[24]	Proposed
Count of bootstrap drivers	2	1
Control technique	PWM+PSM	PWM+PFM
Circulating current	Yes	No
Load voltage controllable region	full	full
MPPT controllable region	full	part

where $A = \frac{(1-d)(d+d_1)}{2d+d_1}$, $B = I_oR_{L1}$, $C = I_oR_{on}$, $E = U_o + 2U_F + I_oR_{L2}$, $F = 2L_2f_sI_o$. R_{L1} and R_{L2} are the winding resistances of the inductors L_1 and L_2, R_{on} denotes the $R_{ds(on)}$ resistances of MOSFETs S_1 and S_2, U_F is the forward voltage drop of the diodes D_1 and D_o.

The ideal and non-ideal voltage gains of the proposed TPC against the duty cycle under different load power are illustrated in Fig. 7, where R_{L1}=9mΩ, R_{L2}=65mΩ, R_{on}=19mΩ, U_F=0.7V, L_2=100μH, f_s=56kHz, U_o=300V. The voltage gain of non-ideal TPC is degraded at a higher duty cycle, primarily when the duty cycle is higher than 0.9, and there is a maximum point around d=0.97. The proposed converter cannot be optimally operated under the extreme duty cycle.

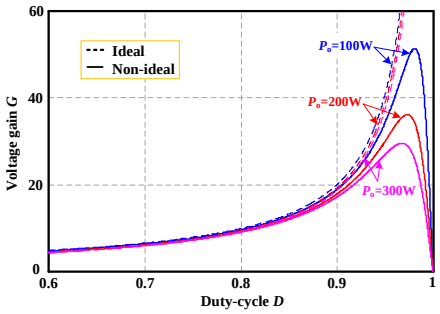

Fig. 7. Comparison of the ideal and practical voltage gains of the proposed TPC.

2) Impact on efficiency: When the switching losses of MOSFETs, reverse recovery loss of diode, and core losses are not considered, the efficiency of the proposed TPC in SISO I mode can be calculated by [27, 28]:

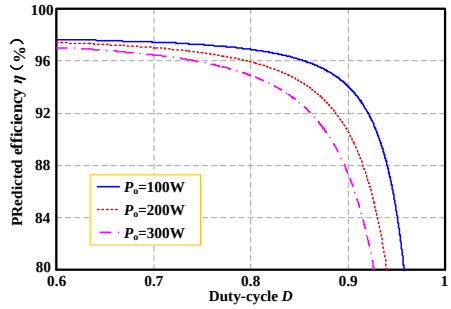

Fig. 8. The theoretical efficiency of the proposed TPC.

$$\eta_1 = \frac{G_2}{G_1} \tag{21}$$

In SISO I mode, the MOSFET S_1 operates in hard switching, and its switching loss can be derived as

$$P_{sw,S1} = \frac{1}{2}C_{oss}U_{S1}^2f_s + \frac{1}{6}U_{S1}f_s\left[I_{L1,val}t_r + (I_{L1,peak} + I_{L2,peak})t_f\right] \tag{22}$$

where C_{oss}, t_r and t_f are the output capacitance, rise time and fall time of MOSFET, respectively; $I_{L1,val}$ is the valley value of i_{L1}; and $I_{L1,peak}$ and $I_{L2,peak}$ are the peak currents of L_1 and L_2, respectively.

The MOSFET S_2 realizes ZVS, but the reverse recovery of the body diode D_{S2} occurs when S_1 is turned on. Hence, the switching loss of S_2 can be expressed as

$$P_{sw,S2} = Q_{rr1}U_{S2}f_s \tag{23}$$

where Q_{rr1} is the reverse recovery charge of D_{S2}.

The diode D_1 realizes ZCS turn-off, no reverse recovery loss. The diode D_2 is turned off with hard switching, and its switching loss can be obtained as

$$P_{sw,Do} = Q_{rr2}U_{Do}f_s \tag{24}$$

where Q_{rr2} is the reverse recovery charge of D_o.

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The core losses of L_1 and L_2 are expressed as

$$P_{\text{core}} = P_{\text{c1}}V_{\text{e1}} + P_{\text{c2}}V_{\text{e2}} \tag{25}$$

where P_{c1} and P_{c2} are the core loss densities of L_1 and L_2, respectively; V_{e1} and V_{e2} are the core volumes of L_1 and L_2, respectively.

The percentage of switching losses of S_1, S_2, D_o and the core losses of L_1, L_2 to an input power is obtained as [27, 28]:

$$\begin{aligned}\eta_{\text{loss}} &= \frac{P_{\text{sw,S1}}+P_{\text{sw,S2}}+P_{\text{sw,Do}}+P_{\text{core}}}{I_{\text{B}}U_{\text{B}}} \\ &= \frac{P_{\text{sw,S1}}+P_{\text{sw,S2}}+P_{\text{sw,Do}}+P_{\text{core}}}{U_{\text{B}}I_{\text{o}}G_1}\end{aligned} \tag{26}$$

Therefore, the conversion efficiency of the proposed TPC in SISO I mode can be calculated as

$$\eta = \eta_1 - \eta_{\text{loss}} \tag{27}$$

The calculated efficiency against the duty cycle considering all losses is shown in Fig. 8, where C_{oss}=800pF, t_{r}=85ns, t_{f}=55ns, Q_{rr1}=250nC, Q_{rr2}=180nC, P_{c1}=5kW/m^3, P_{c2}=20kW/m^3, V_{e1}=52.1cm^3, V_{e2}=4.16cm^3. The efficiency rapidly decreases when the duty cycle is higher than 0.8. Hence, the maximum duty cycle d_{max} of the of the proposed converter is limited to 0.8. Similarly, the proposed TPC efficiency can be obtained in the other three modes.

V. PWM+PFM Control Strategy

A. PWM+PFM Method

For the TPCs in standalone PV systems, the primary control target is to ensure the output voltage regulation under the entire operating conditions. The second objective is to achieve MPPT control of PV cells to maximize the use of solar energy. The most commonly used MPPT algorithms are disturbance and observation method, and incremental conductance method. These algorithms are implemented with dual-loop control. The outer loop samples the voltage u_{pv} and the current i_{pv} of the PV port and generates the PV port reference voltage $u_{\text{pv,ref}}$ through MPPT calculation. The inner loop regulates u_{pv} to track its reference value $u_{\text{pv,ref}}$, finally reaching the MPP voltage and ensuring the PV cells' maximum power output.

It can be noted from (9) that when the battery port voltage U_{B} remains unchanged, PV port voltage U_{pv} only relies on the PWM duty cycle d. Combining (9) with (16), the following can be obtained as

$$f_{\text{s}} = \frac{d^2U_{\text{pv}}U_{\text{o}}(2U_{\text{pv}} - U_{\text{o}})}{2L_2P_{\text{o}}(U_{\text{o}} - U_{\text{pv}})} \tag{28}$$

It can be seen from (10) that the voltage gain G_1 of the proposed TPC is related to d and d_1, hence U_{o} can be adjusted with d. U_{pv} and f_{s} are positively correlated for a given L_2, P_{o}, U_{o}, and d, as indicated in (28). Therefore, U_{pv} can be controlled by f_{s}. Fig. 9 shows the hybrid PFM and PWM controller design of the proposed TPC. The output signal (u_{r1}) of proportional integral (PI) controller 1 (i.e., PV port voltage controller) is converted to f_{s} by the PFM unit, to regulate u_{pv} and track the PV reference voltage $u_{\text{pv,ref}}$. The load port voltage u_{o} is controlled by changing d , which is generated from PWM unit and is corresponding to the output signal (u_{r2}) of PI controller 2 (i.e., load port voltage controller).

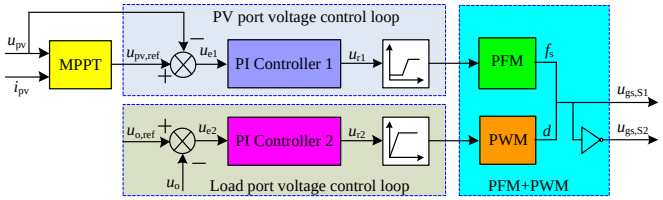

Fig. 9. The control system diagram of the proposed TPC.

B. Implementation Condition for PWM+PFM Method

The precondition for the PWM+PFM method is that L_2 works in DCM. Hence, the following relation should be satisfied.

$$d + d_1 < 1 \tag{29}$$

By substituting (9) into (29), the necessary and sufficient condition for inductor L_2 to work in DCM can be obtained as

$$U_{\text{pv}} < U_{\text{pv,upp}} = \frac{1}{2}(U_{\text{o}} + U_{\text{B}}) \tag{30}$$

where $U_{\text{pv,upp}}$ is the upper limit of U_{pv}.

If L_2 works in critical-conduction mode (CRM) or CCM, the PV port voltage U_{pv} must equal $U_{\text{pv,upp}}$. In other words, the MPP voltage U_{mpp} higher than $U_{\text{pv,upp}}$ cannot be tracked with the PWM+PFM method shown in Fig. 9.

In addition, due to the limitation of $U_{\text{o}}/U_{\text{pv}}$ shown in (9), the lower limit of PV port voltage is obtained as

$$U_{\text{pv,low}} = \frac{1}{2}U_{\text{o}} < U_{\text{pv}} \tag{31}$$

Hence, the MPP voltage lower than $U_{\text{pv,low}}$ cannot be tracked and reached because the PV port voltage u_{pv} is not dropped below its lower limit even if the duty cycle d reaches the maximum.

In theory, as long as U_{mpp} satisfies the conditions expressed in (30) and (31), the voltage control of the PV port and load port can be realized through PWM + PFM method in the entire load and voltage range. However, the minimum switching frequency $f_{\text{s,min}}$ is predefined to avoid the inductor saturation of L_1 during the output regulation. If f_{s} is too high, the switching loss and EMI increase enormously. Therefore, $f_{\text{s,max}}$ needs to be set under the appropriate range, as shown in Fig. 9. When f_{s} reaches upper or lower limits, the system switches to the PWM state. Therefore, the proposed TPC can only realize PWM + PFM control within a certain range.

According to (28), Fig. 10 shows the relationship curves between u_{pv} and P_{o} under different switching frequencies, when U_{B}=48V, U_{o}=300V, $P_{\text{o,max}}$=300W and L_2=100μH. The PWM + PFM working region for the proposed TPC is depicted in the blue shaded part in Fig. 10. The lower and upper boundaries of this region are under curves 1 and 3, which correspond to $f_{\text{s,min}}$=56kHz and $f_{\text{s,max}}$=168kHz, respectively. If $f_{\text{s,max}}$ is set higher, the curve obtained from (28) crosses the upper limit line of U_{pv}, as shown in curve 4 in Fig. 10. In other words, the upper boundary of PWM+PFM region is curve 4 and the line where U_{pv}=$U_{\text{pv,upp}}$. Although the controllable region can be expanded further, the power loss increases consequently.

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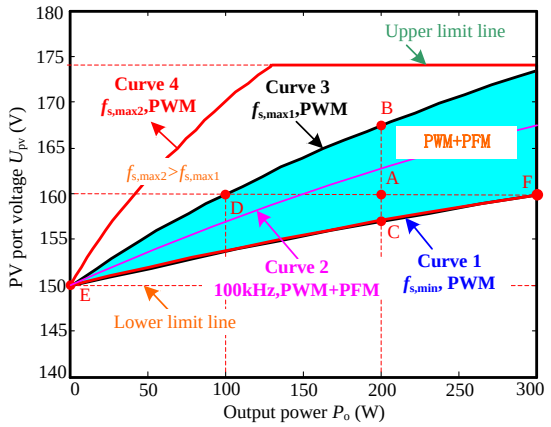

Fig. 10. PWM + PFM (dual control loop) and PWM (single control loop) working regions for the proposed TPC.

C. Functionality in Practical Cases

The modulation method and the trajectory of operating point (U_{pv}, P_o) of the proposed TPC in practical cases are analyzed in this subsection. By assuming that the initial operating point is dot A in Fig. 10, the following two cases are discussed.

1) U_{mpp} changes and P_o remains unchanged:

a) U_{mpp} increases: The switching frequency f_s gradually rises until $f_{s,max}$ with the increase of U_{mpp}. Accordingly, the operating point slides vertically from dot A to dot B. After that, if U_{mpp} continues to rise and is even higher than $U_{pv,upp}$, f_s keeps constant at $f_{s,max}$ and the operating point remains at dot B.

b) U_{mpp} decreases: When load power remains unchanged, f_s gradually decreases until $f_{s,min}$ with the decrease of U_{mpp}. Accordingly, the operating point slides vertically from dot A to dot C. After that, if U_{mpp} continues to decline and is even lower than $U_{pv,low}$, f_s remains unchanged at $f_{s,min}$ and the operating point remains at dot C.

2) U_{mpp} remains unchanged and P_o changes:

a) P_o increases: The switching frequency f_s gradually decreases as P_o increases, making U_{pv} track U_{mpp} until P_o=$P_{o,max}$. Accordingly, the operating point slides horizontally to the right from dot A to dot F.

b) P_o decreases: When MPP voltage remains unchanged, f_s gradually increases with the decrease of P_o until $f_{s,max}$. Accordingly, the operating point slides horizontally to the left from dot A to dot D. Thereafter, if P_o continues to decline, f_s keeps constant at $f_{s,max}$, the operating point slides from dot D along curve 3 to the decreasing direction of P_o, and U_{pv} gradually decreases. When the load power P_o drops to 0, the PV port voltage is equal to $U_{pv,low}$ (dot E).

It should be emphasized that the operating point trajectory and modulation method are only related to the P_o and U_{mpp}, not to the working mode of TPC. In other words, operating points of TPCs in various operation modes may correspond to the same dots in the blue area in Fig. 10.

VI. SMALL SIGNAL MODELS OF THE PROPOSED TPC

This section focuses on the small-signal models of the proposed TPC to derive the PWM control to output transfer function. The small-signal analysis of the proposed TPC based on the series coupling of the PFM+PWM control scheme is not analyzed. Due to the simultaneous variation of frequency and duty cycle to regulate the output voltage, it is challenging to accurately identify the converter dynamic modeling.

A. Dynamic Modeling in DISO Mode and SISO I Mode

The equivalent series resistance (ESR) r_C of the capacitor C_o is considered in the converter dynamic model. According to the equivalent circuits shown in Fig. 3 of the proposed TPC during one switching period, the average model can be obtained by using the state-space averaging method, as shown in (32). $u_B(t)$ and $i_{pv}(t)$ are the input variable, $u_o(t)$ is the output variable, and $d(t)$ is the control variable. The state variables are the inductor currents $i_{L1}(t)$, $i_{L2}(t)$ and the capacitor voltages $u_{C1}(t)$, $u_{C2}(t)$ and $u_{Co}(t)$. The symbol of $\langle\rangle$ represents the average value of each variable in a switching period,$\langle i_{L2}\rangle_{(d+d_1)T_s}$,represents the average value of i_{L2} during the interval of stages 1, 2 and 3.

The auxiliary equation is expressed as

$$\langle i_{L2}\rangle_{(d+d_1)T_s} = \frac{\langle u_{C1}\rangle - \langle u_{C2}\rangle}{2f_sL_2}\langle d\rangle \tag{33}$$

The output equation is described as

$$\langle u_o\rangle = \langle u_{Co}\rangle + r_C C_o \frac{d\langle u_{Co}\rangle}{dt} \tag{34}$$

The average value of each variable can be described by the steady-state component (denoted by upper-case letter) and the small-signal disturbance (denoted by subscript ^), which is derived as (35).

By manipulating (32)-(35), the small-signal model of the converter can be obtained as (36) and (37).

$$\hat{u}_o(s) = \hat{u}_{Co}(s) + sr_C C_o \hat{u}_{Co}(s) \tag{37}$$

From (36)-(37), the control to output transfer function $G_{ud1}(s)$ is derived as (38) and (39).

B. Dynamic Modeling in SIDO Mode and SISO II Mode

Compared to DISO and SISO I modes, the current direction of inductor L_1 in SIDO and SISO II modes is opposite, so the coefficients involving i_{L1} in the state average equation and transfer function $G_{ud2}(s)$ take the inverse number, and the other variables remain unchanged.

When C_1=C_2=C_o=20μF, L_1=320μH, L_2=100μH, r_C= 0.01Ω, R=300Ω, U_B=48V, D=0.7, the theoretical and simulated bode diagrams of $G_{ud1}(s)$ and $G_{ud2}(s)$ are plotted in Matlab/Simulink, as shown in the solid and dotted lines in Fig. 11, respectively. The theoretical and simulated results are consistent in the frequency band below 0.2f_s.

VII. PARAMETERS DESIGN

A. Specifications of The Prototype

To verify the feasibility of the proposed TPC and the correctness of the theoretical analysis, an experimental prototype is built in the laboratory, and the specifications are listed in Table III.

$$\begin{bmatrix} L_1\frac{d\langle i_{L1}\rangle}{dt} \\ L_2\frac{d\langle i_{L2}\rangle}{dt} \\ C_1\frac{d\langle u_{C1}\rangle}{dt} \\ C_2\frac{d\langle u_{C2}\rangle}{dt} \\ C_o\frac{d\langle u_{Co}\rangle}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \langle d\rangle-1 & 0 & 0 \\ 0 & 0 & \langle d\rangle & -\langle d\rangle-\langle d_1\rangle & 0 \\ 1-\langle d\rangle & -\langle d\rangle & \frac{\langle d\rangle-1}{r_C}+\frac{\langle d\rangle-1}{R}-\frac{1}{R_{pv}} & \frac{\langle d\rangle-1}{r_C}+\frac{\langle d\rangle-1}{R} & \frac{1-\langle d\rangle}{r_C} \\ 0 & \langle d\rangle+\langle d_1\rangle & \frac{\langle d\rangle-1}{r_C}+\frac{\langle d\rangle-1}{R} & \frac{\langle d\rangle}{r_C}-\frac{1}{r_C}+\frac{\langle d\rangle-1}{R} & \frac{1-\langle d\rangle}{r_C} \\ 0 & 0 & \frac{1-\langle d\rangle}{r_C} & \frac{1-\langle d\rangle}{r_C} & -\frac{1-\langle d\rangle}{r_C}-\frac{\langle d\rangle}{r_C+R} \end{bmatrix} \begin{bmatrix} \langle i_{L1}\rangle \\ \langle i_{L2}\rangle_{(d+d_1)T_s} \\ \langle u_{C1}\rangle \\ \langle u_{C2}\rangle \\ \langle u_{Co}\rangle \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}\langle u_B\rangle + \begin{bmatrix} 0 \\ 0 \\ 1 \\ 0 \\ 0 \end{bmatrix}\langle i_{pv}\rangle \tag{32}$$

$$\langle d\rangle = D+\hat{d}, \langle d_1\rangle = D_1+\hat{d}_1, \langle i_{pv}\rangle = I_{pv}+\hat{i}_{pv}, \langle i_{L1}\rangle = I_{L1}+\hat{i}_{L1}, \langle i_{L2}\rangle = I_{L2}+\hat{i}_{L2}, \langle i_{L2}\rangle_{(d+d_1)T_s} = I'_{L2}+\hat{i}_{L2},$$
$$\langle u_B\rangle = U_B+\hat{u}_B, \langle u_{C1}\rangle = U_{C1}+\hat{u}_{C1}, \langle u_{C2}\rangle = U_{C2}+\hat{u}_{C2}, \langle u_{Co}\rangle = U_{Co}+\hat{u}_{Co}, \langle u_o\rangle = U_o+\hat{u}_o \tag{35}$$

$$\begin{bmatrix} sL_1\hat{i}_{L1}(s) \\ sL_2\hat{i}_{L2}(s) \\ sC_1\hat{u}_{C1}(s) \\ sC_2\hat{u}_{C2}(s) \\ sC_o\hat{u}_{Co}(s) \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & D-1 & 0 & 0 \\ 0 & 0 & D & -(D+D_1) & 0 \\ 1-D & -D & \frac{D-1}{r_C}+\frac{D-1}{R}-\frac{1}{R_{pv}} & \frac{D-1}{r_C}+\frac{D-1}{R} & \frac{1-D}{r_C} \\ 0 & D+D_1 & \frac{D-1}{r_C}+\frac{D-1}{R} & \frac{D-1}{r_C}+\frac{D-1}{R} & \frac{1-D}{r_C} \\ 0 & 0 & \frac{1-D}{r_C} & \frac{1-D}{r_C} & -\left(\frac{1-D}{r_C}+\frac{D}{r_C+R}\right) \\ 0 & 2f_sL_2 & -D & D & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(s) \\ \hat{i}_{L2}(s) \\ \hat{u}_{C1}(s) \\ \hat{u}_{C2}(s) \\ \hat{u}_{Co}(s) \end{bmatrix}$$
$$+ \begin{bmatrix} 1 & 0 & U_{C1} & 0 \\ 0 & 0 & U_{C1}-U_{C2} & -U_{C2} \\ 0 & 1 & \frac{U_{C2}}{R}-\frac{U_{Co}}{r_C}+\frac{U_{C1}}{r_C}+\frac{U_{C1}}{R}+\frac{U_{C2}}{r_C}-I_{L1}-I'_{L2} & 0 \\ 0 & 0 & I'_{L2}+\frac{U_{C1}+U_{C2}}{R}+\frac{U_{C1}+U_{C2}-U_{Co}}{r_C} & I'_{L2} \\ 0 & 0 & \frac{U_{Co}}{r_C}-\frac{U_{C1}}{r_C}-\frac{U_{Co}}{r_C+R}-\frac{U_{C2}}{r_C} & 0 \\ 0 & 0 & -(U_{C1}-U_{C2}) & 0 \end{bmatrix} \begin{bmatrix} \hat{u}_B(s) \\ \hat{i}_{pv}(s) \\ \hat{d}(s) \\ \hat{d}_1(s) \end{bmatrix} \tag{36}$$

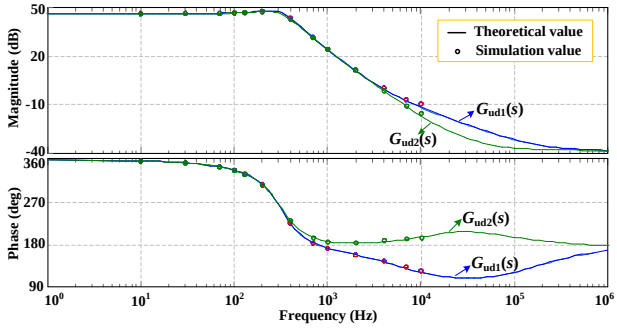

Fig. 11. Bode diagrams of $G_{ud1}(s)$ and $G_{ud2}(s)$.

TABLE III
SPECIFICATIONS OF PROPOSED TPC

Port	Parameters	Value
PV	PV voltage U_{pv}	160-170 V
	PV current I_{pv}	0-2 A
Battery	Nominal battery voltage U_B	48V
Load	Load voltage U_o	300 V
	Maximum load power $P_{o,max}$	300 W

B. Design of Inductors L_1 and L_2

The design method and selection of capacitors C_B, C_1, C_2 and C_o are similar to a conventional boost converter; therefore, it is not described in this paper. However, the design of inductors of the proposed TPC under PWM+PFM control is different from the conventional PWM control and hence explained in detail.

By substituting the parameters listed in Table III into (9) and (28), the relation curves of switching frequency f_s versus load power P_o under different L_2 and U_{pv} are plotted in Fig. 12. As can be seen, when L_2 and U_{pv} are given, f_s automatically decreases gradually with the increase of P_o to ensure that L_2 works under DCM; under the same U_{pv}, both the upper and lower limits of f_s increase with the decrease of L_2. Consequently, the volume and weight of L_1 and L_2 can be reduced, but the switching loss increase accordingly. For compromise, L_2 is designed as 100μH and ranging from 56kHz$\leq f_s \leq$168kHz.

The decrease of inductance can optimize the volume and weight of the inductor with the converter dynamic response. However, the current ripple increases, leading to high power loss in the inductor and switching devices. Due to the small internal resistance of the battery, a larger capacitor is required. In general, an input inductor of the boost converter is designed to ensure the maximum peak to peak value of inductor current does not exceed 20%-30% of the maximum average current. Weighing the constraints of dynamic characteristics, capacitance C_B, power loss and other factors, the ripple rate

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$$G_{\mathrm{ud}}(s)=\left.\frac{\hat{u}_{\mathrm{o}}(s)}{\hat{d}(s)}\right|_{\hat{u}_{\mathrm{B}}(s)=0,\hat{i}_{\mathrm{pv}}(s)=0}=\frac{(1+sr_{\mathrm{C}}C_{\mathrm{o}})\left[Xs^3+(AX+Y+TZ)s^2+(X\varphi+AY+\iota Z+TP)s+\varphi Y+\iota P\right]}{Ms^4+(MA+Q-VZ)s^3+(M\varphi+AQ+K-ZW-VP)s^2+(\varphi Q+AK-PW)s+\varphi K} \tag{38}$$

$$\begin{cases}
X=BH-\frac{G}{2f_s},Y=CH+G+\theta,Z=BF-E,P=CF+N,\\
T=\eta-\phi H,W=\phi O+\gamma,M=BJ,Q=BO+CJ,K=CO-\varpi,V=\phi J\\
A=\varepsilon+\frac{\phi\omega}{\psi},B=1-\frac{\chi\rho}{\beta},C=\mu+\frac{\delta\rho}{\beta},O=\frac{\sigma}{\psi},J=\frac{1}{\psi},E=\frac{\chi\rho}{\beta},F=\frac{\omega}{\psi},G=\frac{\alpha\rho}{\beta},H=\frac{\tau}{\psi},N=\nu+\frac{\zeta\rho}{\beta}\\
\alpha=\frac{U_{\mathrm{C1}}-U_{\mathrm{C2}}}{L_2},\beta=\frac{U_{\mathrm{C2}}}{L_2},\chi=\frac{D}{2f_sL_2},\delta=\frac{D+D_1}{L_2},\zeta=\frac{D}{L_2}\\
\varepsilon=\frac{D}{C_1}\frac{D}{2f_sL_2}-\frac{D-1}{C_1r_{\mathrm{C}}}-\frac{D-1}{C_1R}+\frac{1}{C_1R_{\mathrm{pv}}},\varphi=\frac{1-D}{C_1}\frac{1-D}{L_1},\phi=\frac{D-1}{C_1r_{\mathrm{C}}}+\frac{D-1}{C_1R}+\frac{D}{C_1}\frac{D}{2f_sL_2},\gamma=\frac{1-D}{C_1r_{\mathrm{C}}}\\
\eta=\frac{U_{\mathrm{C1}}+U_{\mathrm{C2}}}{C_1R}+\frac{U_{\mathrm{C1}}+U_{\mathrm{C2}}-U_{\mathrm{Co}}}{C_1r_{\mathrm{C}}}-\frac{I_{\mathrm{L1}}}{C_1}-\frac{I'_{\mathrm{L2}}}{C_1}-\frac{D}{C_1}\frac{U_{\mathrm{C1}}-U_{\mathrm{C2}}}{2f_sL_2},\iota=\frac{1-D}{C_1}\frac{U_{\mathrm{C1}}}{L_1},\kappa=\frac{1-D}{C_1}\frac{1}{L_1},\lambda=\frac{1}{C_1}\\
\mu=\frac{D+D_1}{C_2}\frac{D}{2f_sL_2}-\frac{D-1}{C_2r_{\mathrm{C}}}-\frac{D-1}{C_2R},\nu=\frac{D-1}{C_2r_{\mathrm{C}}}+\frac{D-1}{C_2R}+\frac{D+D_1}{C_2}\frac{D}{2f_sL_2},\varpi=\frac{1-D}{C_2r_{\mathrm{C}}}\\
\theta=\frac{I'_{\mathrm{L2}}}{C_2}+\frac{U_{\mathrm{C1}}+U_{\mathrm{C2}}}{C_2R}+\frac{U_{\mathrm{C1}}+U_{\mathrm{C2}}-U_{\mathrm{Co}}}{C_2r_{\mathrm{C}}}+\frac{D+D_1}{C_2}\frac{U_{\mathrm{C1}}-U_{\mathrm{C2}}}{2f_sL_2},\rho=\frac{I'_{\mathrm{L2}}}{C_2}\\
\sigma=\frac{1-D}{C_{\mathrm{o}}r_{\mathrm{C}}}+\frac{D}{C_{\mathrm{o}}(r_{\mathrm{C}}+R)},\tau=\frac{U_{\mathrm{Co}}}{C_{\mathrm{o}}r_{\mathrm{C}}}-\frac{U_{\mathrm{C1}}}{C_{\mathrm{o}}r_{\mathrm{C}}}-\frac{U_{\mathrm{Co}}}{C_{\mathrm{o}}(r_{\mathrm{C}}+R)}-\frac{U_{\mathrm{C2}}}{C_{\mathrm{o}}r_{\mathrm{C}}},\omega=\frac{1-D}{C_{\mathrm{o}}r_{\mathrm{C}}},\psi=\frac{1-D}{C_{\mathrm{o}}r_{\mathrm{C}}}
\end{cases} \tag{39}$$

of no more than 30% under the lowest switching frequency $f_{\mathrm{s,min}}$ and the maximum battery current $I_{\mathrm{B,max}}$ is selected.

In order to satisfy the above current ripple requirements, the inductance L_1 can be calculated as

$$L_1=\frac{U_{\mathrm{B}}dT_{\mathrm{s}}}{\Delta I_{\mathrm{L1}}}\geq\frac{U_{\mathrm{B}}dT_{\mathrm{s,max}}}{0.3I_{\mathrm{B,max}}}=\frac{U_{\mathrm{B}}^2\left(U_{\mathrm{pv}}-U_{\mathrm{B}}\right)}{0.3U_{\mathrm{o}}I_{\mathrm{o,max}}f_{\mathrm{s,min}}U_{\mathrm{pv}}} \tag{40}$$

According to Table III and the minimum switching frequency $f_{\mathrm{s,min}}$=56kHz, it can be obtained that $L_1\geq320\mu$H, and L_1 is designed as 320μH.

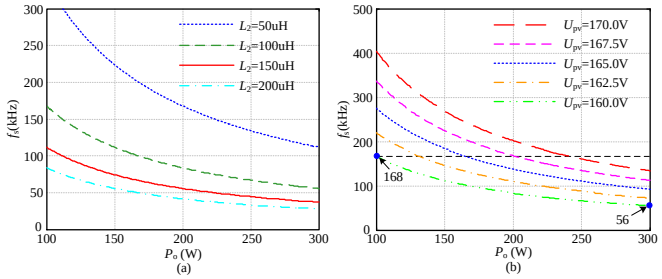

Fig. 12. Relation curves of f_{s} versus P_{o} under different inductance L_2 and PV port voltage U_{pv}. (a) U_{pv}=160V. (b) L_2=100μH.

C. Design of Load Port Voltage Controller Parameters

Fig. 13 shows the simplified closed-loop control based on voltage regulation, where H is the load port voltage feedback coefficient, $G_{\mathrm{c}}(s)=k_{\mathrm{p2}}+k_{\mathrm{i2}}/s$ is the transfer function of PI controller 2, and F_{m} is the PWM gain. The closed-loop transfer function can be obtained as

$$\frac{\hat{u}_{\mathrm{o}}(s)}{\hat{u}_{\mathrm{o,ref}}(s)}=\frac{G_{\mathrm{c}}(s)G_{\mathrm{ud}}(s)F_{\mathrm{m}}}{1+G_{\mathrm{c}}(s)G_{\mathrm{ud}}(s)HF_{\mathrm{m}}} \tag{41}$$

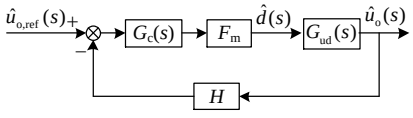

Fig. 13. Load port voltage closed-loop control diagram.

According to the Routh stability criterion and (41), the stability regions of the proposed TPC with PWM control in four working modes is obtained and shown in Fig. 14, where F_{m}=1/2.4, and H=0.01. As can be seen, the optimized control parameter are chosen based on the blue shaded area to ensure the proposed TPC can be stablized for all the operation modes.

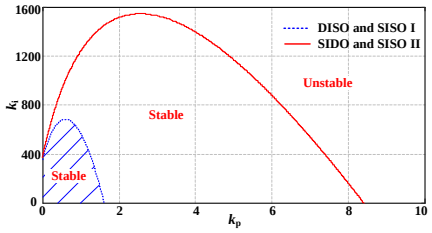

Fig. 14. Stable regions of the proposed TPC with PWM control.

Due to the strong coupling between the two control loops, in order to make the proposed TPC operates robustly under diverse working modes and strict conditions, the parameters of load port voltage control loop are selected as (k_{p2}=0.01, k_{i2}=20), which are far away from the boundary line in the stability zone shown in Fig. 14. Fig. 15 shows the bode diagrams of open-loop transfer function $T_1(s)=F_{\mathrm{m}}HG_{\mathrm{c}}(s)G_{\mathrm{ud1}}(s)$ and $T_2(s)=F_{\mathrm{m}}HG_{\mathrm{c}}(s)G_{\mathrm{ud2}}(s)$, respectively. The gain margin G_{m} and phase margin P_{m} are far greater than zero, indicating that the selected controller parameters ensure the robustness of the proposed TPC.

TABLE IV
POWER STAGE PARAMETERS OF PROTOTYPE

Device	Chip model or parameter
S_1,S_2	IXFP72N30X3M, 300V/19mΩ
D_{o}	STTH803, 300V/0.8V/30ns
D_1	VS-8ETU04S-M3, 400V/0.94V/35ns
C_{B}, C_1, C_2, C_{o}	20μF/100V, 20μF/250V, 20μF/250V, 20μF/400V
L_1	320μH, EE55/28/25, R_{L1}=9mΩ
L_2	100μH, EE28/10/11, R_{L2}=65mΩ

VIII. EXPERIMENTAL VERIFICATION

An experimental prototype for the proposed TPC was built and tested to verify its feasibility. The design parameters of

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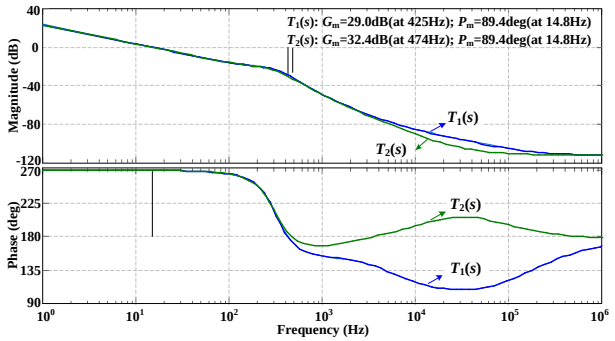

Fig. 15. Bode diagrams of $T_1(s)$ and $T_2(s)$.

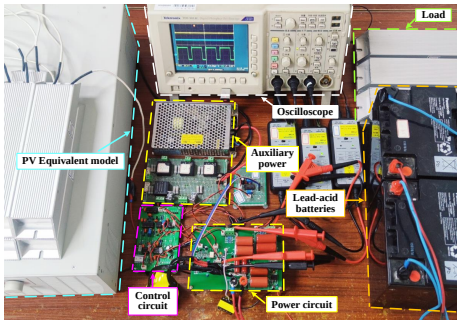

Fig. 16. Detailed schematic diagram of the setup.

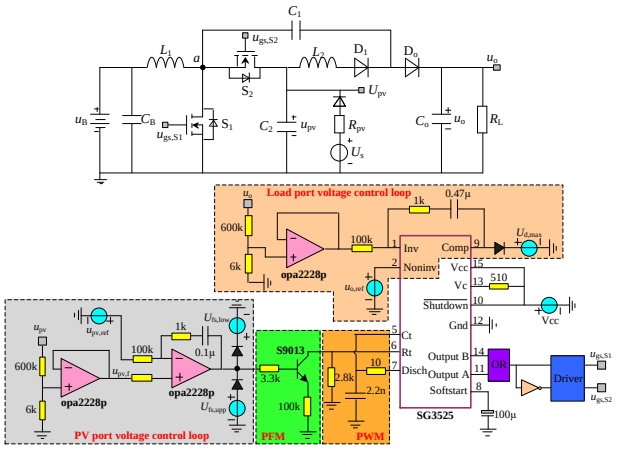

Fig. 17. Detailed schematic diagram for the setup.

the power stage are shown in Table IV. The polypropylene film capacitors with low ESR are leveraged for C_B, C_1, C_2 and C_o. The power stage attains a power density of 380W/Lit without mounting any heat sink. The laboratory setup is shown in Fig. 16. The detailed schematic diagram for the analog control is shown in Fig. 17. The DC voltage source U_s is connected in series with resistor R_{pv} is used to emulate the PV cells with the maximum power point voltage $0.5U_s$. The variation of temperature and irradiance can be emulated by adjusting the U_s and R_{pv}. The battery stack contains four Panasonic lead-acid battery cells of 12V and 28A●h in series. Since this research aims to evaluate the feasibility of the proposed TPC and control method, hence the MPPT calculation part shown in Fig. 9 is ignored in the experiment and the PV port voltage reference value of $u_{pv,ref}$ is given directly. The load port voltage reference value of $u_{o,ref}$ is set as 3V. By increasing the collector current of the triode S9013 in Fig. 17, the frequency of the PWM signal generated by the PWM control chip SG3525 can be decreased. $f_{s,max}$ and $f_{s,min}$ are set with the voltages $U_{fs,upp}$ and $U_{fs,low}$ in Fig. 17, respectively. In addition, the $U_{d,max}$ is used to set the maximum duty cycle d_{max}=0.8.

Figs. 18 and 19 demonstrate the steady-state operation of experimental waveforms in DISO mode (U_{pv}=160V, P_{pv}=80W, P_o=300W) and SIDO mode (U_{pv}=160V, P_{pv}=320W, P_o=200W), respectively. Figs. 18(a) and 19(a) illustrate that the inductor currents i_{L1} and i_{L2} are in continuous and discontinuous states, respectively. The inductor current i_{L1} flows in positive direction in DISO mode, indicating the discharging state of the battery. The negative current direction in SIDO mode reveals the charging state of the battery. The duty cycles are d=0.71 and d_1=0.11 and the voltage gain is measured as u_o/u_B=300V/48V≈6.25. These measured values are consistent with the theoretical analysis and verify the high voltage step-up capability of the TPC. As can be seen from Fig. 18(b), the drain-to-source voltage $u_{ds,S2}$ of S_2 drops to zero before applying the PWM driving signal $u_{gs,S2}$ and begins to rise after 250ns dead time, which indicates that switch S_2 realizes ZVS turn-on and turn-off. However, switch S_1 is operated in hard-switching. The switching states of S_1 and S_2 in SIDO are opposite to that in DISO, as demonstrated in Fig. 19(b). From Figs. 18(c) and 19(c), it can be observed that before the diode D_1 is reverse biased, its current i_{D1} is dropped to zero, hence D_1 is ZCS turned off. The voltage stresses across S_1, S_2 and D_o are 160V, which are consistent with the theoretical analysis. The transient voltage ringing across the diode D_1 can also be observed. This phenomenon is caused by the resonance between the junction capacitance of D_1 and the inductor L_2 when D_1 is turned off, and is an inherent issue of the method using blocking diode to achieve discontinuous inductor current (DCM) [29]. Although S_1 (DISO mode), S_2 (SIDO mode) and D_o working under hard switching, their voltage stresses are reduced to half of the load voltage. Therefore, MOS transistor with low on-state resistance, ultrafast recovery diode with short reverse recovery time, and even Schottky diode can be employed in this prototype, thus switching loss and conduction can be reduced further.

The dynamic responses of source voltage variation of battery and PV are shown in Fig. 20. In Fig. 20(a), the voltage u_B is changed gradually in the range of 56V to 40V over several hundreds of milliseconds, when U_s=320V, R_{pv}=320Ω, $u_{pv,ref}$=1.6V and P_o=200W. It is observed that the load voltage and the PV voltage approximately at 300 V and 160V, respectively, due to the adjustment of the voltage loop PI controllers. In Fig. 20(b), the PV reference voltage $u_{pv,ref}$ is directly changed from 1.6V to 1.4V, representing the variation of U_{mpp} from 160V to 140V. As can be seen, when P_o=200W and $u_{pv,ref}$=1.6V, the operating point is dot A, located in the PWM+PFM region shown in Fig. 10. When $u_{pv,ref}$ changes to 1.4V, i_{L2} remains in DCM, the switching frequency is clamped at $f_{s,min}$ and u_{pv} is controlled at 156V. This indicates the

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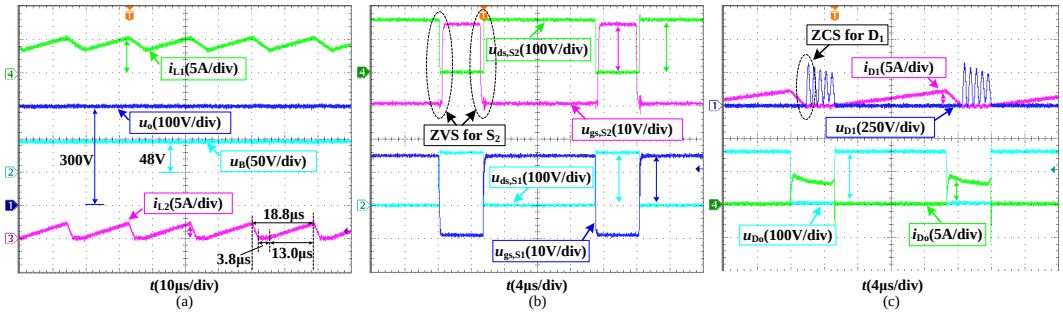

Fig. 18. Steady-state operation of the proposed TPC in DISO mode. (a) u_B, u_o, i_{L1} and i_{L2}. (b) $u_{ds,S1}$, $u_{gs,S1}$, $u_{ds,S2}$ and $u_{gs,S2}$. (c) u_{Do}, i_{Do}, u_{D1} and i_{D1}.

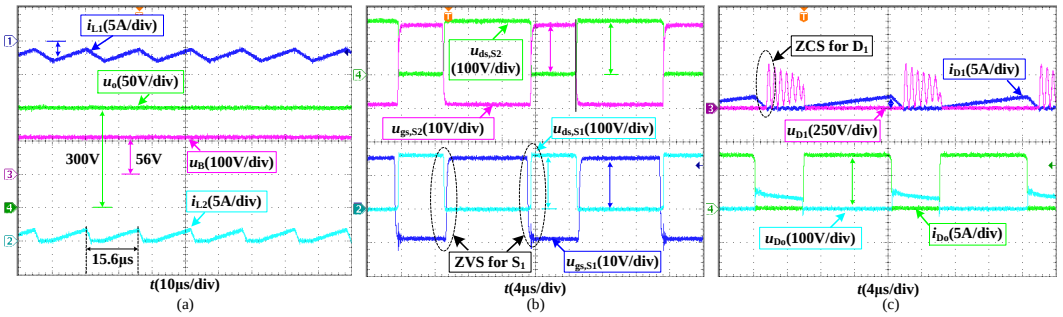

Fig. 19. Steady-state operation of the proposed TPC in SIDO mode. (a) u_B, u_o, i_{L1} and i_{L2}. (b) $u_{ds,S1}$, $u_{gs,S1}$, $u_{ds,S2}$ and $u_{gs,S2}$. (c) u_{Do}, i_{Do}, u_{D1} and i_{D1}.

operating point changes from dot A to C, as shown in Fig. 10. However, the load port voltage u_o is regulated at 300V. Fig. 20(c) shows the PV reference voltage $u_{pv,ref}$ is directly changed from 1.6V to 1.8V, representing the variation of U_{mpp} from 160V to 180V. When $u_{pv,ref}$ changes to 1.8V, i_{L2} remains in DCM, the switching frequency is clamped at $f_{s,max}$, u_{pv} is controlled at 167V, indicating the operating point is dot B at the upper boundary, as shown in Fig. 10. The feedback control of the proposed TPC is capable of regulating the load port voltage at 300V.

Fig. 21(a) shows the dynamic responses of load changing from 0 to 200W step, where U_s=320V, R_{pv}=80Ω, and $u_{pv,ref}$=1.6V. It can be seen that when the proposed TPC is under no load, u_o is maintained at 300V and u_{pv} at 150V. The operating point corresponds to dot E in Fig.10. i_o and i_B are 0 and -1.5A, respectively, indicating that it works in SISO II mode, as shown in Fig. 2(d). After the load step change, u_{pv} and u_o are controlled at 160V and 300V, respectively. The settling time is t_s=44ms, the undershoot of u_o is about 13.3%, and i_o and i_B become 0.62A and 2.5A, respectively. These results indicate that the proposed TPC enters DISO mode and realizes voltage regulation of load port and PV port simultaneously.

Fig. 21(b) shows the load transient response of the proposed TPC, where the load power step changes from 300W to 100W while U_s=320V, R_{pv}=120Ω and $u_{pv,ref}$=1.6V. It can be seen that after the load is suddenly decreased, u_{pv} and u_o are able to maintain at 160V and 300V within at t_s=26ms; the overshoot of u_o and undershoot of u_{pv} are about 4.3% and 5%, respectively; i_o changes from 1A to 0.4A, i_B changes from positive to negative, and the proposed TPC switches the operation mode from DISO to SIDO.

Fig. 21(c) shows the transient response of irradiance step change which can be emulated by switching R_{pv} from 80Ω to 320Ω and $u_{pv,ref}$=1.6V, U_s=320V, P_o=200W. The output voltages of load port and PV port are stabilized at 300V and 160V with stable operation. i_{pv} changes from 2A to 0.5A, i_B changes from negative to positive, indicating the the proposed TPC is switched the operation mode from SIDO to DISO.

Fig. 21(d) shows the response of R_{pv} switching from 320Ω to infinity and $u_{pv,ref}$ changing from 1.6V to 1.5V (as emulated transition from daylight to night time) at P_o≈200W. Before R_{pv} switching, I_{pv}≈0.42A and I_B≈3A, u_{pv} and u_o are 160V and 300V, respectively, showing the proposed TPC operates in DISO mode. After R_{pv} is step changed, u_o and u_{pv} stabilize at 156V and 300V, respectively. At this time, I_{pv}=0 and I_B≈5A, indicating that the TPC enters SISO I mode.

Fig. 22 shows the theoretical power losses distributions of the proposed TPC under the four main operation modes, where $P_{con,S}$ and $P_{sw,S}$ denote the conduction loss and switching loss of the active switches, respectively; $P_{con,D}$ and $P_{rr,D}$ are the conduction loss and reverse recovery loss of the diodes, respectively. In addition, P_{cop} and P_{core} are the total copper loss and total core loss of the inductors, respectively. The operation conditions are described as follows, respectively. (a) DISO mode: U_B=48V, U_o=300V, U_{pv}=160V, P_{pv}=300W, P_o=300W; (b) SIDO mode: U_B=48V, U_o=300V, U_{pv}=160V, P_{pv}=300W, P_o=250W; (c) SISO I mode: U_B=48V, U_o=300V, U_{pv}=160V, P_{pv}=0, P_o=300W; (d) SISO II mode: U_B=48V, U_o=300V, U_{pv}150V, P_{pv}=300W, P_o=0. The ESRs of C_B, C_1, C_2 and C_o are very small and the gate driver and control circuit are powered by the auxiliary switching power supply, hence their losses are not included in calculating system efficiency.

Under the working conditions of DISO mode and SIDO

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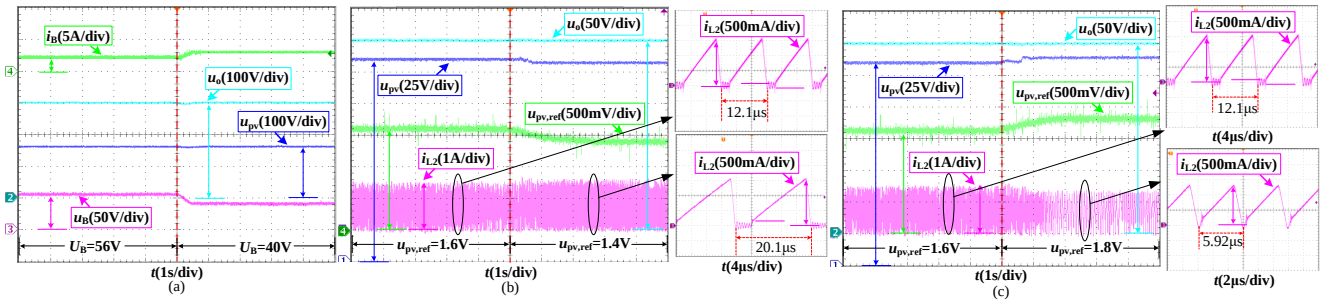

Fig. 20. Dynamic response of the proposed TPC. (a) Step change of battery voltage from 56V to 40V. (b) Step change of PV voltage from 160V to 140V. (c) Step change of PV voltage from 160V to 180V.

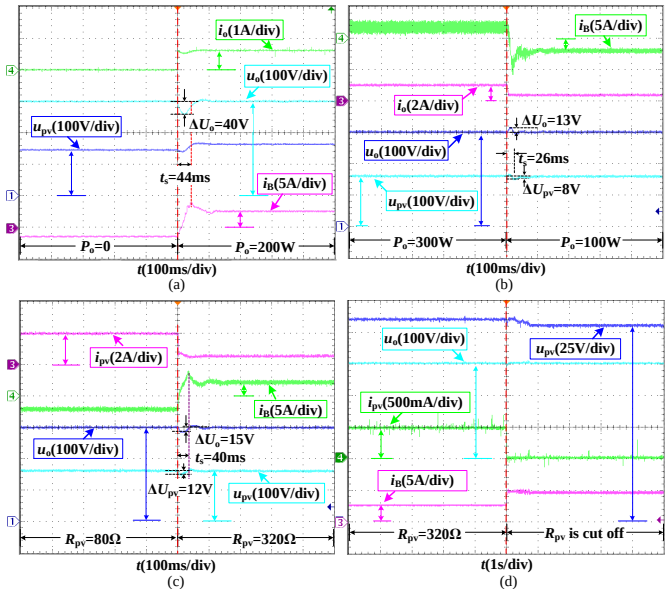

Fig. 21. Dynamic response of the TPC operation modes under step change of load power and PV irradiance. (a) Load power step from 0 (SISO II) to 200W (DISO). (b) Load power step from 300W (DISO) to 100W (SIDO). (c) Emulated step change of the PV irradiance by adjusting the R_{pv} from 80Ω (SIDO) to 320Ω (DISO). (d) Emulated transition from day to night by adjusting R_{pv} from 320Ω (DISO) to infinity (SISO I).

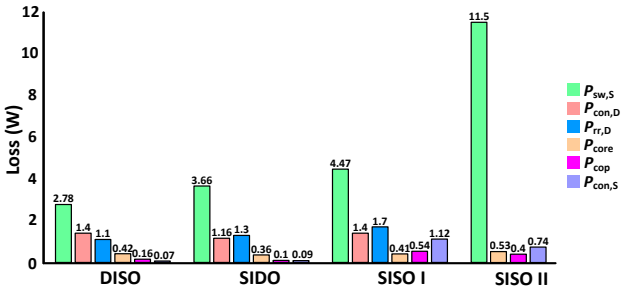

Fig. 22. The power losses distributions of the proposed TPC under the four main operation modes.

mode, the switching frequency and the battery port current are relatively low; therefore, the losses of switches are reduced, resulting in the high theoretical efficiencies, which are 79.06% and 98.06%, respectively. Under the operating condition of SISO I mode, the PV power P_{pv}=0, the load power is completely provided by the battery. Therefore, the current I_B is larger, and consequently, the conduction loss and switching loss of the switches are higher, resulting in slightly low theoretical efficiency (about 96.88%). Under the operation condition of SISO II mode, although the load power P_o=0 and the losses of diodes are approximately zero, the maximum switching frequency and the large battery port current I_B will cause higher switching losses of switches than those in SISO I mode. Hence, the theoretical efficiency is reduced to 95.61%.

Fig. 23 shows the efficiency curves of the proposed TPC under different operation modes. The efficiency calculation formulas are expressed in Table V.

TABLE V
POWER STAGE PARAMETERS OF PROTOTYPE

Operation mode	State of battery	Efficiency formula
DISO	discharging	$\eta_1 = U_o I_o/(U_{pv} I_{pv}+U_B I_B)$
SIDO	charging	$\eta_2 = [U_o I_o+(-I_B)U_B]\ /(U_{pv} I_{pv})$
SISO I	discharging	$\eta_3 = (U_o I_o)/(U_B I_B)$
SISO II	charging	$\eta_4 = (-I_B U_B)/(U_{pv} I_{pv})$

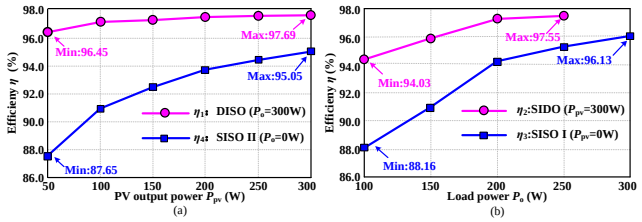

Fig. 23. Efficiency curves of proposed TPC. (a) DISO mode (P_o=300W). (b) SIDO mode (P_{pv}=300W).

In DISO and SISO II modes, U_o=300V, the load power is P_o=300W and P_o=0, respectively, and the PV power P_{pv} varies from 50W to 300W by keeping U_s constant at 320V and changing the value of R_{pv}. From Fig. 23(a), it can be seen that the maximum measured efficiencies in DISO mode and SISO II modes are 97.69% and 95.05%, respectively, which finds good agreement with the predicted efficiency results.

In SIDO and SISO I modes, the PV power is P_{pv}≈300W by keeping U_s=320V and R_{pv}≈85Ω, respectively, U_o=300V, and the load power P_o varies from 50W to 250W (SIDO mode) and 300W (SISO I mode), respectively. From Fig. 23(b), it can be seen that the maximum efficiencies in SIDO mode and SISO I modes are measured as 97.55% and 96.13%, respectively, which are consistent with the prediction efficiencies.

The results demonstrate that the proposed TPC realizes high conversion efficiency.

IX. Conclusion

This paper uses a simple construction method to develop a ZVS transformer-less high gain TPC from a single-switch dual-inductor high gain boost converter. The proposed TPC is comprehensively analyzed and tested under different operation modes to verify the theoretical analysis and practical feasibility. The research results demonstrate that compared to existing TPCs, the proposed TPC has the advantages of high voltage conversion gain, equal to almost twice the conventional boost converter, continuous and bidirectional battery current, fewer power switches (only two) and reduced voltage stress. In addition, the proposed TPC port shares a common ground for all three ports, and two complementary switches, forming a phase-leg, can be deriven by any off-the-shelve bootstrap gate driver. The proposed TPC shows a stable output voltage with the source voltage variation of battery and PV, as well as step load change. The dynamic results are consistent with the small-signal model. Further, the proposed TPC simultaneously realizes MPPT control at the PV port and constant voltage control at the load port using the hybrid PWM+PFM modulation strategy. The proposed TPC can realize constant load voltage control throughout the entire operating range. However, if the operating conditions are outside of the PWM+PFM region, the practical operating point is limited to the boundary, and the switching frequency is clamped at $f_{s,max}$ or $f_{s,min}$, thus entering PWM mode. With the application of the third-generation power electronic devices, the maximum switching frequency of the proposed TPC can be lifted while maintaining high conversion efficiency to obtain a wider PWM+PFM controllable region. The voltage stress on power devices is curtailed to almost half of the load port voltage. Besides, the synchronous switch and diode D_1 can realize the soft-switching operation. Therefore, the power losses are significantly reduced, resulting in higher conversion efficiency. The prototype shows a peak efficiency of 97.7% in the laboratory. Therefore, the proposed TPC is suitable for standalone PV power generation systems with low cost, high efficiency, and high power density requirements.

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Ling Qin (Member, IEEE) received the B.S. degree in electrical engineering from Southeast University, Nanjing, China, in 1999, and the M.S. and Ph.D. degrees in electrical engineering from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2007 and 2017, respectively.

From January 2016 to January 2017, he was a Visiting Scholar at the Centre for Future Energy Networks, University of Sydney, Sydney, NSW, Australia. He is currently a Professor in the Department of Electrical Engineering, Nantong University, Nantong, China. His research interests include high-efficiency power conversion technology, renewable energy grid-connected power generation technology, modeling and control of power electronic systems. His work has resulted in more than 60 technical publications and mare than 30 China patents.

Tianhong Qian was born in Jiangsu, China, in 2000. She received the B.S. degree in Electrical engineering and automation from Nantong University, Nantong, China, in 2022. She is currently working toward the M.S. degree in control science and engineering from Nantong University, Nantong, China.

Her current research interest focuses on the three-port soft-switching dc converters.

John Long Soon (Member, IEEE) received the Master's and Ph.D. degrees in electrical engineering from The University of Sydney, Sydney, NSW, Australia, in 2015 and 2019, respectively.

From 2018 to 2019, he was a laboratory instructor to supervise various of lab courses and R&D designs for the STEM educational learning kits including internet of things (IoT), power converter and audio amplifier, at the School of EIE in the University of Sydney, NSW, Australia. From 2019 to 2020, he was a Postdoctoral Researcher under the microgrid lab at the National University of Singapore (NUS). In 2021, he joined the ION Mobility Pte. Ltd. as a Lead Power Electronics Engineer, Singapore, where he was mainly responsible for the high-power PCB and firmware integration for the EV motorbike, including battery management system (BMS), On-Board charger (OBC), 3-phase PMSM motor controller. His current research interests include EV powertrain, power converter topologies, fault-tolerant and reliability of power electronics.

Dr. Soon was the recipient of the Best Paper Award in the category of Emerging Power Electronic Technique at the IEEE PEDS 2015 in Sydney conference.

Waqas Hassan (Member, IEEE) received the bachelor's (hons.) and master's degrees in electrical engineering from the University of Engineering and Technology, Taxila, Pakistan, in 2010 and 2014, respectively, and the Ph.D. degree in electrical engineering from The University of Sydney, NSW, Australia, in 2020.

He is currently a Lecturer at the School of Engineering, University of Tasmania. He has over ten (10) years of experience in academic, research and industry in the power and energy sector. Prior to joining the University of Tasmania, he was a senior R&D engineer at Regal Rexnord Corporation, Australia, where he worked on next-generation motor drives. His research interests include designing and developing power electronics technologies and products, solar photovoltaic (PV) power systems, renewable energy systems, DC microgrids, and electric vehicle systems. His recent work has been featured by the IEEE Industrial Electronics Society and IET Renewable Power Generation.

Min Tian was born in Anhui, China, in 1997. He received the B.S. degree in Electrical engineering and automation from Nantong University, Nantong, China, in 2019. He is currently working toward the M.S. degree in control science and engineering from Nantong University, Nantong, China.

His current research interest focuses on the topology and control of three-port soft-switching dc converter.

Lei Zhou was born in Jiangsu, China, in 1996. He received the B.S. degree in automation from Nantong University, Nantong, China, in 2020. He is currently working toward the M.S. degree in control science and engineering from Nantong University, Nantong, China.

His current research interest focuses on the high-gain dc/dc converters.

Lei Ren was born in Nantong, China, in 1991. He received the B.Eng. and Ph.D. degrees in Electrical Engineering from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2013 and 2019 respectively.

He has been a Lecturer since 2019 in the College of Electrical Engineering, Nantong University, Nantong, China. His current research interests include static inverters and condition monitoring of power electronic converters.