Low Voltage Ride-Through Enhancement of DFIG-Based Wind Turbine Using DC link Switchable Resistive Type Fault Current Limiter

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***Abstract*—Doubly-fed induction generator (DFIG)-based wind turbines utilise small-scale voltage sourced converters with a limited overcurrent withstand capability, which makes the DFIG-based wind turbines very vulnerable to grid faults. Often, modern DFIG systems employ a crowbar protection at the rotor circuit to protect the rotor side converter (RSC) during grid faults. This method converts the DFIG to a squirrel cage induction generator, which does not comply with the new grid codes. The recent grid codes need wind turbines to stay connected to the utility grid during and after power system faults, especially in high penetration level of wind power. Furthermore, the crowbar switch is expensive. This paper proposes a novel DC-link switchable resistive-type fault current limiter (SRFCL) to improve the LVRT capability of the DFIG. The proposed SRFCL is employed in the DC side of the RSC. The SRFCL solves crowbar protection activation problems and eliminates subsequent complications in the DFIG system. The proposed SRFCL does not have any significant impact on the overall performance of the DFIG during normal operation. Whenever the fault, whether symmetrical or asymmetrical, occurs, the SRFCL not only limits rotor over-currents but also prevents rotor speed acceleration and restricts high torque oscillations even during zero grid voltage, as recommended by some grid codes. To prove the effective operation of the SRFCL on the RSC fault current limitation, analytical analysis is performed in each switching interval. The proposed approach is compared with the crowbar-based protection method. Simulation studies are carried out in PSCAD/EMTDC software. In addition, a prototype is provided to demonstrate the main concept of the proposed approach.**

***Keywords*—doubly-fed induction generator; low voltage ride-through; grid faults; DC link; switchable resistive type fault current limiter.**

1. Introduction

By increasing the penetration level of wind energy conversion systems (WECS) in power grids in recent years, the grid operators are faced with new operational challenges in order to avoid grid instability and to ensure the secure and reliable operation of the power system. One of these challenges is that wind turbines, similar to conventional power plants, must be able to stay connected with the utility grid during voltage sag when a grid fault happens. This operational behaviour is known as low voltage ride-through (LVRT) capability [1].

Currently, the doubly fed induction generator (DFIG)-based wind turbines are widely used because of many salient features [2]. The stator of DFIG is usually directly connected to the utility grid and a partially scaled back-to-back connected voltage source converter (VSCs) links the rotor circuit to the power grid. In the case of a low voltage at the grid side of the DFIG, transient over-currents flow from the rotor circuit towards the rotor side converter (RSC). These over-currents can either trip the DFIG system out or damage its power electronic components [3, 4]. Therefore, the great challenge is to keep the DFIG wind turbine connected with the utility grid during the low voltage conditions and, at the same time, prevent the equipment from damage.

In the literature, several LVRT approaches have been introduced to improve the LVRT capability of the DFIG. The most common method is to employ crowbar protection and protect the back-to-back converters during low voltage [5, 6]. This method changes the DFIG to a squirrel cage induction generator. In this situation, due to absorption of the reactive power from the grid, the DFIG does not comply with the grid requirements, as mentioned in grid codes [7, 8].

Changing the DFIG configuration is one of the solutions to improve the LVRT behaviour of the DFIG based wind turbines. In [9] and [10], nine switch grid side converter has been proposed to overcome the fault situation in the power system. Meanwhile, in [11] and [12], a series gird side converter connected to a star point terminal of the stator including parallel gird side rectifier and three winding transformer have been utilized to make adequate power processing capability and ride though the low voltage. As it is clear, these approaches make fundamental changes in the conventional DFIG configuration and it may not be a simple process for industry to carry out. So, practical implementation of these methods will probably not be economical.

Some studies in the literature [13-16] have discussed advanced control strategies for the LVRT solutions of the DFIG. In [13], an efficient method with active and passive FRT compensators has been proposed that more measurements and two control strategy are required to the LVRT of the DFIG. Novel hybrid controllers in the (dq)+ and rotor reference frames have been studied in [14], which only considered the asymmetrical grid faults. An optimisation theory considering practical constraints of the RSC and a reactive power support method have been discussed in [15] and [16], respectively. The LVRT improvement of the DFIG based on damping flux linkage has been proposed in [17], which helps to decrease the RSC current and smooths the electromagnetic torque oscillations. The nonlinearity characteristic of the flux linkage alleviates the efficiency of the control method. In [18], a flux leakage tracking has been discussed, which makes the rotor flux a reduced fraction of the stator flux during the fault condition. In this way, the rotor current can be suppressed to a lower value. However, in this method, a quick changing of the control method is essential after detection of the fault. Meanwhile, different control methods should be utilized during the normal and the fault situations. Due to the complexity of most of these approaches, they may not be practical for the DFIG manufacture companies [16]. Moreover, the DFIG could not ride through the network low voltage just by controlling the converters during the zero grid voltage [6].

Utilising additional hardware in the terminal of the DFIG [19-21] is another way to facilitate the low voltage ride-through. In these methods, voltage sag compensation and reactive power support have been done by a dynamic voltage restorer (DVR) [19, 20] and a static synchronous compensator (STATCOM) [21], respectively. These solutions need huge amount of storage component.

Another additional hardware, which is very well-known in limiting the fault current and compensating the voltage sag in the power system, is fault current limiter (FCLs). Some configuration of the FCLs are employed to increase the LVRT capability of the DFIG based wind turbine in the power network [22-25]. A three phase FCL including an isolation transformer and a large DC inductance with a bypass resistance located in the stator side of the DFIG is used to restrict the fault current level [22, 23]. A single phase bridge type FCL is utilized in the terminal of the DFIG to improve the LVRT capability of the DFIG during all gird faults [24]. Superconducting FCL is also interesting in limiting the fault current in the DFIG [25]. Despite of the mentioned FCLs for the LVRT improvement of the DFIG, various types of FCLs are also employed to improve power system operation during power system faults (PSFs) in the literature [26]-[30]. In section IV, a comprehensives comparison of the previous studied FCLs with the proposed method will be done in details.

In this paper, the DC-link switchable resistive type FCL (SRFCL) is proposed to limit the rotor transient over-currents and, consequently, to improve the LVRT capability of the DFIG during symmetrical and asymmetrical grid faults. The operation of the proposed method is compared to the crowbar protection. By means of the proposed scheme, continuous operation can be also ensured for the DFIG even during zero grid voltage. In addition, due to the use of non-superconducting inductance in the SRFCL, the proposed LVRT approach has low initial cost and simple configuration. Simulation results are carried out in PSCAD/EMTDC software for different types of grid faults. Furthermore, an experimental setup is provided to show the effectiveness of the proposed SRFCL in the LVRT improvement of the back-to-back converters.

1. Brief Review of Fault Ride-Through Behaviour of the DFIG

In the case of PSFs, the low voltage appears at the stator terminal of the DFIG; its depth depends on the fault characteristics. In this condition, severe over-voltages caused by the natural flux of the stator are induced in the rotor windings [3]-[4]. These over-voltages generate transient over-currents passing through the rotor towards the RSC. Because the maximum permissible current of the RSC’s semiconductor devices is approximately twice that of their nominal current [31], these over-currents can damage the RSC’s semiconductor devices. Therefore, the RSC cannot continuously operate during low voltage in the terminal of the DFIG without any special protective measures.

Meanwhile, as the grid voltage drops during the fault condition, considering the limited capacity of back-to-back connected VSCs, the GSC cannot transfer power imported from the RSC to the DC-link further to the grid. This excess active power charges the DC-link capacitor voltage and rapidly increases its voltage from the nominal value. This over-voltage must be restrained by special protective measures to avoid damage to the DFIG power converters.

In a modern DFIG-based wind turbine, the application of a crowbar is a common practice to protect the RSC against high over-currents [5, 6]. The crowbar is a protection device, which is installed between the rotor windings and the RSC. Following a grid fault, the crowbar is triggered, thus providing a safe route for rotor over-currents. In general, the crowbar activation converts the DFIG to a squirrel cage induction generator, which cannot meet the LVRT requirements imposed by the new grid codes.

1. Proposed Low Voltage Ride Through Scheme For the DFIG and its Control Circuit

The schematic diagram of the proposed LVRT configuration to provide continuous operation during the PSFs for the DFIG is shown in Fig. 1. To improve the ride-through capability of the DFIG during the PSFs, the SRFCL is connected in series with the RSC (between the RSC and the DC link capacitor), as shown in Fig. 1.The suggested SRFCL is composed of three main parts, which are described as follows:

1. A diode bridge rectifier that consists of *D1* to *D4* diodes.
2. A non-super-conductor magnet (copper coil) that is represented by a resistor *rd*and an inductance *Ld*.
3. A parallel connection of a fully controllable semiconductor switch (SS), such as *IGBT*, *IGCT etc.*, and a discharging resistor (*rp*) that are connected in series with the DC inductance.

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| G:\Research Paper  22 December\DFIG\DFIG revised by Kashem and Mehrdad\Elsevier\figures\1-1-1.png |
| Fig. 1. The proposed fault ride through configuration for the DFIG-based wind turbine during various power system faults. |

With this arrangement, the rotor transient over-currents are effectively limited at the time of the occurrence of the fault and its clearance, thanks to the SRFCL. In Fig. 1, the DC inductance does not have a significant impact on the normal operation of the DFIG. But, when a fault occurs, the DC inductance effectively suppresses *di/dt* initiated in the first moments of the fault (which is significantly higher in the first cycle) and also limits the rotor over-current successfully during the fault period. It should be noted that the DC link current (*idc*), is a periodic DC current and its value depends on the switching pulses of the RSC and the rotor currents. So, in Fig. 1, utilising just an inductance without a rectifier diode-bridge in series with the RSC causes a voltage drop due to across the inductance in the DC link and, as a result, disturbs the normal operation of the back-to-back connected VSCs, as well as the DFIG. To solve this problem and to provide the DC route for the DC inductance current (*id*), the rectifier diode-bridge is utilised in the proposed SRFCL as shown in Fig. 1. Overall, by applying the proposed SRFCL, the DFIG can ride through the voltage sag during the fault.

In the proposed LVRT configuration, the resistor in parallel connection with the SS is employed to consume the excess active power of the generator during the fault. Therefore, the *rp* can provide a balance between input active power to the turbine and output power from the generator during the fault.

The DFIG-based wind turbine may have a DC-chopper installed at the DC-link [32]. This module not only protects the DC-link from over-voltage during the fault but it can also enhance overall system performance during the normal operation, especially when there is an imbalance between the active power of the RSC and the GSC [32]. Meanwhile, the limited rotor fault current by the SRFCL reduces the charging current to the DC-link capacitor. The overall structure of the control circuits for the rotor side and the gird side converters are shown in Fig. 2. In the rotor side converter, the active power control *Pactual* is based on the wind conditions during the normal operation. *Pref*is calculated with regard to maximum power point tracking (MPPT) and as a result, the *d*-axis reference current of rotor *idr* is obtained. In the gird side converter, the DC link voltage *Edc,actual*is compared to the reference value *Edc,ref*. In the DC-link voltage control and the grid side current control, PI controllers are utilized for regulation. In addition, the reactive power *Qactual* in both the rotor side and the grid side converters is directly regulated by reference value, *Qref*.

The control circuit of the proposed SRFCL is shown in Fig. 3. In the normal operation of the power system, the SS is closed and bypasses the *rp*. Therefore, the SRFCL does not have any effect on the normal operation of the DFIG. Furthermore, in this condition, by selecting the proper value for the *Ld*, it is possible to achieve a nearly constant DC current through the DC inductance. It is evident that increasing the inductance of the *Ld*decreases the ripple of *id*. This leads to a short circuit of the *Ld*during the steady state operation. In the meantime, when the fault occurs in the power system, the DC inductance prevents *di/dt* at the first moment of the fault. If the fault lasts for a long time, the current through the DC inductance will increase. When the DC inductance current reaches to a threshold value, *IC*, the SS is switched off and the *rp*, evacuates the *Ld*. In addition, when the DC inductance current decreases below the value of *IC*, the control circuit turns on the SS. Consequently, by turning on and turning off the SS, the *idc* remains limited during the fault period. By using a suitable value for the *rp*, it can be ensured that the *id* is limited to the *IC*. In this condition, the excess active power of the generator will be absorbed in the DC inductance. As a result, the SRFCL prevents rotor speed acceleration. Moreover, by consuming the active power during the fault, the *rp* mitigates severe electrical torque oscillations at the time of the occurrence and the clearance of the fault. It is clear that the proposed SRFCL can increase the life of the turbine shaft and the gearbox.

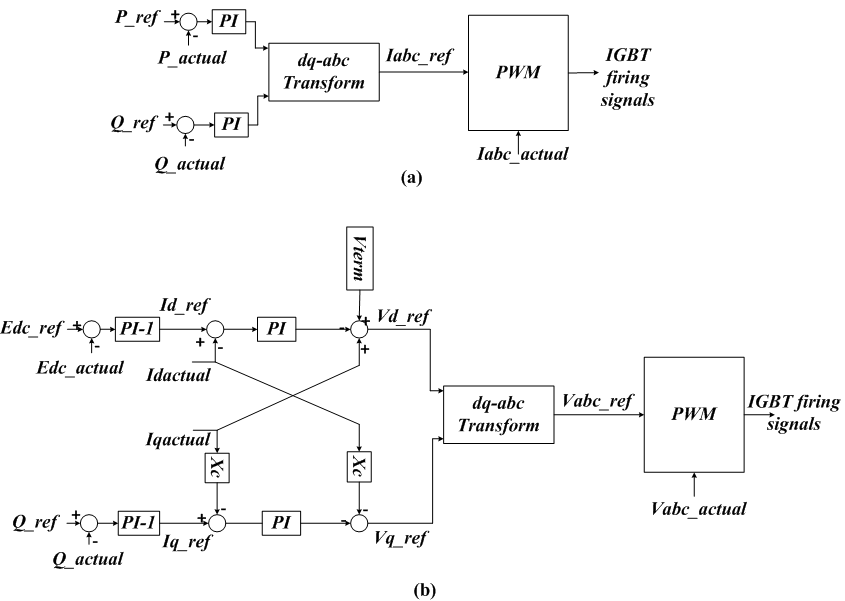


Fig. 2 The overall structure of the control circuits of the DFIG, (a): rotor side controller, (b): grid side controller.

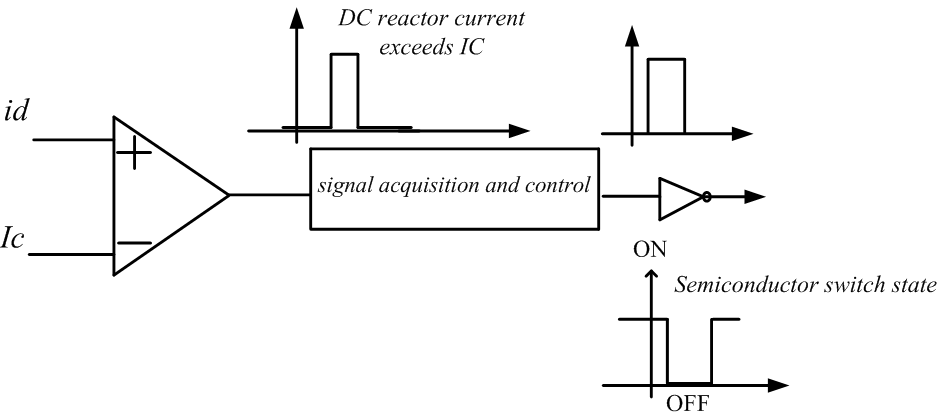


Fig. 3. Control circuit of the proposed SRFCL

1. Advantages of the DC Link SRFCL as the Proposed LVRT Scheme   
   and its Comparison with Other FCLs

This section deals with the comparison of the performance of the proposed LVRT scheme from the power circuit topology point of view, with other previously introduced FCL-based LVRT methods for DFIG.

In [22], the authors introduced switch-type FCL (STFCL) connected in series with the stator circuit of the DFIG as a dedicated topology to improve its LVRT capability. The STFCL topology includes three fault limiting inductors, three isolation transformers, a three phase diode bridge, a snubber capacitor, one SS, and a series connection of a resistance and a very large capacitor to absorb excess energy of the DFIG during the fault condition. As it can be realized, the STFCL employed many power components in its structure, which limit the possibility of its practical implementation.

The performance of the three types of bridge types FCL (BTFCL) is evaluated in [23] to enhance the LVRT capability of the DFIG. The first type of the BTFCL is introduced a basic topology. However, when the diode bridge in the basic topology of the BTFCL conducts, high stator voltage spikes are induced. Moreover, this situation increases the rotor currents and electromagnetic torque oscillations during the normal operation. The basic BTFCL topology adversely affects the steady state operation of the DFIG. To tackle this problem, authors in [24] proposed to add a current regulator circuit (CRC) to the basic BTFCL topology and called the created new topology as BTFCL-CRC. However, due to adding two SS and power diodes in the BTFCL structure, the increased number of SS leads to a reduction in the reliability of the whole system. On the other hand, this situation increases the steady state power losses of the BTFCL-CRC. Finally, as another solution to solve the previous problems associated with the BTFCL topology, the authors proposed to replace the diode-bridge with a thyristor-bridge and insert a bypass resistor (BR) in parallel with the primary side of the isolation transformer. This topology is called BTFCL-BR. The BTFCL-BR eliminates two excess SS in comparison with the BTFCL-CRC but, in this structure, the thyristor bridge must be fully conducting (ON state) during the normal operation, which increases the power losses.

During the normal operation of the DFIG, about %70 of the rated power of the DFIG is passed through the stator. Also during the fault condition, a high percentage of the DFIG fault current (about %90) is injected through the stator. Considering these facts, and the research in [22]-[23], three similar sets of the STFCL must be connected in series with the stator of the DFIG. The rating of the STFCL devices must be selected carefully to withstand the rated voltage and current of the stator during the normal condition, as well as the fault condition. As a result, in this situation, power losses of the whole system will be increased during the normal operation.

Another LVRT scheme based on the BTFCL is proposed in [24] to improve the LVRT capability of the DFIG. The authors of [24] employed the BTFCL at the terminal of the DFIG to improve its LVRT capability. However, this approach requires connecting three similar sets of the BTFCL in series with the individual phases. From the power circuit topology point of the view, this approach employs twelve power diodes, three high speed semiconductor switches, three DC inductances, and three series R-L branches that are connected in parallel with a diode-bridge. Moreover, from the control circuit point of view, the method in [24] requires the measurement of *id*, the AC side currents, and the terminal voltage of the DFIG to control the SS. In addition, in [25], the authors introduced the application of the bridge-type superconducting FCL (SFCL) at the terminal side of the DFIG to improve the LVRT capability. However, this method, similar to the approach presented in [24], needs to connect three similar sets of the SFCL in series with the individual phases of the DFIG. Generally, the SFCL cannot be justified from a practical point of view, especially due to high installation and maintenance costs of the superconductors.

However, the proposed LVRT scheme in this paper uses just one single set of the FCL incorporated in the DC side of the RSC to ensure the LVRT capability of the DFIG during the PSFs. Meanwhile, from the power circuit topology point of view, in comparison with other previously introduced LVRT methods for the DFIG, the proposed scheme employs minimum additional components. Moreover, from the control circuit point of view, in the proposed LVRT approach, unlike methods present in [24], the *id* is employed to control operations of the SS. As a result, in comparison with other LVRT methods, this method has a high level of reliability.

Other types of the FCLs are also applied to the power system to limit the fault current level. Well-known applications and configurations of the FCLs in the power grid have been presented in many previous works [26]-[30]. In all of the mentioned studies, for current limiting in the AC side of DFIG system, three similar sets of the FCL must be connected in series with the individual phases. But in the proposed scheme, just one single set of the SRFCL is required to limit the RSC fault current in all three phases. Accordingly, the present approachwould result in considerable cost reduction in the present approach for the FCLs. Additionally, from the power circuit topology point of view, the proposed SRFCL uses one diode bridge rectifier and one fully controllable SS as a high speed switch. Utilising the proposed SRFCL in the DC side of the RSC, in comparison with previously introduced FCL structures in the AC side, has the following advantages:

* In [26], in order to provide a DC route for the inductance current, three sets of single phase transformers and a three phase diode-bridge rectifier are used. However, in the proposed approach, not only are three isolation transformers eliminated but also one single phase diode-bridge rectifier is employed to rectify the *id*. Therefore, the number of employed power components for three phase applications is reduced.
* From the power circuit topology point of view, instead of a three phase diode-bridge rectifier and a fully controllable power electronic switch or two thyristor switches in the crowbar-based protection scheme, the proposed approach uses only one single phase diode-bridge rectifier and a non-superconducting inductor to limit the high rotor over-currents.Unlike the crowbar-based protection approach, which bypasses the RSC during the fault, in the proposed scheme, the RSC continuously operates during various grid faults.
* The power circuit topology of the FCL introduced in [27, 28] utilises three similar sets of the FCL in series with individual phases to limit the fault currents. This approach requires three single phase diode-bridge rectifiers, three SSs, three DC inductances, and three series R-L branches, which are connected in parallel with the diode-bridge rectifier to compensate the voltage sag caused during the fault. Therefore, from the power circuit topology point of view, in the proposed method, since the SRFCL is placed in the DC side of the RSC, and there is no requirement to compensate for the voltage sag in the fault condition, the parallel branch is eliminated. Additionally the number of the semiconductors in the proposed approach has been reduced to one third. From the control circuit point of view, the method in [27, 28] requires both the DC inductance and AC side currents to controls the SS, while in the proposed approach only the *id* is employed for control aspects.
* The FCLs are commonly installed at high voltage substations to improve the LVRT capability of the DFIG [25] but in the proposed method, the proposed SRFCL is placed in the DC side of the RSC with a lower voltage level in comparison with AC side applications. As a result, from the insulation point of view, the present approach is more economical than other methods that employ the FCLs at the AC side.
* The proposed SRFCL uses only one fully controllable SS (such as *IGBT* …) which operates at the DC side unlike the method in [29], which employs two SSs that operate at the AC side. Because of eliminating ON/OFF switching signals in the steady state operation, the control of the proposed circuit is simpler.

1. Analytical Technique for Analysis of the Proposed LVRT scheme
   1. *System Description*

When a short-circuit fault occurs in the utility grid, the high rotor over-currents flow toward the RSC. During the fault, the switching pulses of the RSC are continuously issued by the control system. These over-currents pass through the SDs of the RSC and enter into the DC-link. The rotor over-currents are forced to pass through the SRFCL, which is connected between the RSC and the DC-link capacitor. In this way, the proposed SRFCL limits the rotor over-currents to the maximum permissible current of the SDs, *IC*.

Under low voltage conditions at the grid side of the DFIG, the magnitude of the fault current depends on the fault type, depth of the voltage dip and the fault inception [3]-[4]. Also, additional energy, which cannot be delivered to the grid by the GSC, charges the DC-link capacitor and rapidly increases its voltage from its nominal value. Therefore, the DC-chopper is triggered to keep the DC-link voltage at an acceptable limit. The system response, due to operation of the DC-chopper and the induced rotor voltages during the fault, is non-linear. So, some approximations are required to perform an analysis of the proposed scheme.

The DC-link voltage is approximately constant during the fault period due to the DC-chopper operation. In the analysis of the proposed approach, similar to the research conducted in [33], the middle part of the DC-link, including the DC-chopper and the DC-link capacitor are modelled on a constant DC voltage source. Furthermore, to simplify the analysis during the voltage sag, the rotor circuit is modelled on a sinusoidal three-phase AC voltage source (*Van*, *Vbn* and *Vcn* as given in Fig. 4) with a constant frequency. The three-phase AC voltage source is connected in series with the transient inductance, *σLr*, and the rotor resistance, *Rr*, where *ω* and *Vϕ* stand for its angular frequency and effective voltage value in each phase, respectively. In Fig. 4, the rotor currents (*ia*, *ib* and *ic*) are purely sinusoidal and switching signals of the VSC are generated using a sinusoidal PWM strategy. The *idc* of 2-level VSC can be expressed based on the AC side currents and switching states as follows [34]:

(1)

where *Sa*, *Sb* and *Sc*are switching states of the phases *a*, *b* and *c*, respectively.

In the carrier-based sinusoidal PWM (SPWM) converters, the carrier frequency is high compared to the fundamental output frequency. In this section, the performance of the proposed scheme is explained during one carrier period [35].



Fig. 4. Schematic diagram of the simplified DFIG system for analytical analysis.

* 1. *Analytical Approach for the Simplified DFIG System*

In this section, in order to better understand the performance of the proposed LVRT scheme, the charging and discharging operating condition of *id* is analysed. It should be noted that each semiconductor device of the RSC and the diode bridge rectifier is modelled on a series connection of its voltage drop (*Vd*) and resistance (*ron*) in ON state. Also the SS is modelled by its voltage drop (*Vss*) and resistance (*ron*) in ON state. Fig. 5 shows the *idc*, the *id* and the switching sequence of the 2-level VSC during one carrier period. As evident, during a change in the switching state, the *idc* instantaneously changes. However, due to the single phase diode-bridge rectifier, the *id* is a smooth current in one carrier period. During *T0*, the switching state is (000) and the *id* is more than the *idc*. Fig. 6(a) shows the equivalent circuit in interval *T0*. According to the equivalent circuit, in the time interval of *T0*, the DC inductance is in the discharging mode. As a result, all diodes of the SRFCL are in on-state and the *id* **freewheels** through *D1-D3* and *D2-D4*. The *id* can be expressed as follow:

(2)

Solving (2) leads to (3), which represents *id* expression during the discharging mode in the normal operation.

(3)

where *i'1=id*(*t0*), *Re1*=*rd*+2*ron*, *Ve1*=*Vss*+2*Vd*.

At *t=t1*, the switching state changes to (100). Fig. 6(b) shows the equivalent circuit in this condition. As the equivalent circuit reveals, the *id* is equal with the *idc* and the DC inductance is in charging mode. Therefore, the *id* can be expressed as follows:

(4)

where *Le*=3/2*σLr*+*Ld*, *Re2*=*rd*+9/2*ron*+3/2*Rr*, *Ve2*=*VDC*-*VSS*-4*Vd*.

As a result:

(5)

where:

At *t=t2*, the switching state changes to (101) and the *id* instantaneously decreases. As a result, in the time interval of *t2* until *t3*, the *id* is more than the *idc* and the DC inductance is in discharging mode (Fig. 6(c)). At *t=t3*, the switching state is not changed but the *idc* is reached to the *id* and the charging mode begins and continues to *t4*, (Fig. 6(d)). At *t=t4*, the switching state changes to (111) and the *idc* instantly decreases to zero. The DC inductance is in discharging mode up to *t5* (Fig. 6(e)). It should be noted that the time interval between *t0* till *t5* is half of the carrier period and the same analysis can be implemented in the next half of the carrier period by *t10*.

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| G:\Research Paper  22 December\DFIG\DFIG revised by Kashem and Mehrdad\Elsevier\figures\4-4.png |
| Fig. 5. SPWM output sequence of the VSC with the measured DC link (*idc*) and the DC inductance (*id*) currents of the simplified DFIG system. |

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| J:\Research Paper 11 April\DFIG\DFIG revised by Kashem and Mehrdad\Elsevier\revise\Fig 6.png |
| Fig. 6. Equivalent circuits of the operating intervals. (a) Switching state (000). (b) Switching state (100). (c)-(d) Switching state (101). (e) Switching state (111). (f) Single line diagram of the test system under study. |

* 1. *Generalisation of the Simplified Analytical Approach for the Real DFIG System*

The simplified analytical approach stated in the section V-B was performed using the fact that the rotor circuit is modelled on the three phase AC voltage source with the fixed frequency and amplitude. However, in the real DFIG system, the induced voltages in the rotor during the fault are composed of various components with different amplitudes and frequencies. Therefore, to extend the analytical analysis performed above to the real DFIG case, the magnitude and frequency of the three phase AC voltage source shown in Fig. 4 must be substituted with the corresponding values of the real DFIG during the grid fault. In the following sections, various grid fault situations are considered for real case study. The rotor-induced voltage expressions during the fault are derived from [3]-[4] and expressed in the rotor reference frame.

### Symmetrical LLLG Fault:

An LLLG fault causes a symmetrical voltage disturbance with the voltage sag depth of *р* at the stator side of the DFIG. In this condition, the rotor voltage has two components, as given in [3]:

(6)

where *Vs* is the amplitude of the stator voltage, *Lm* is the magnetising inductance, *Ls* is the stator self-inductance, *s* is the slip, *р* is the depth of voltage sag, *τs* is the stator time constant; *ωs*, *ωr* and *sωs* are synchronous, rotor and slip angular frequencies, respectively. During the symmetrical fault, the amplitude and frequency of each component of voltage in (6) should be applied in the mathematical expression obtained in section V-B, instead of the three phase AC voltage sources given in Fig. 4. Hence, the new expressions for three phase AC voltage sources will be expressed as follows:

(7)

(8)

In this way, the existing amplitudes and frequencies in the *id* in each time interval are replaced with the corresponding values for the real DFIG system during the symmetrical fault.

### Asymmetrical Faults:

In the case of an asymmetrical fault, the induced voltages in the rotor consist of three terms including positive, negative, and zero sequences. The amplitude and the frequency of each of these components are related to the type of asymmetrical fault. In the following sections, a single phase fault and a phase-to-phase fault are studied to obtain the amplitude and the frequency of each sequence.

#### Single-Phase Fault:

For an LG fault in *a* phase, the induced voltage in the rotor is as follows [4]:

(9)

To obtain the amplitude and frequency of each component presented in (9) during the single phase fault, the following equations are considered:

(10)

(11)

(12)

#### Phase-to-Phase Fault:

The induced voltages in the rotor during a phase-to-phase fault, in *b* and *c* phases, are as follows [4]:

(13)

In this case, similar to the mentioned cases, the following expressions should be replaced with the three phase AC voltage sources:

(14)

(15)

(16)

1. Design considerations

## Power Loss Calculation of the Proposed SRFCL

During one carrier period, as shown in Fig. 5, the *id* is a DC periodic current. In addition, during the charging mode, there are power losses and voltage drops across the DC inductance, the SS, and the diode-bridge rectifier. However, during the normal operation, the DC inductance current is almost ripple-free, with the amplitude equal to the peak of the *idc*. Therefore, (17) can be written as follows:

 (17)

where, *Ir*, *IDC* and *Imax* stand for ripple-current in the DC inductance, the average current in the DC inductance, and the peak value of the *idc* in the steady state, respectively. The total power loss of the SRFCL (*PTotal-loss*) is the sum of the DC inductance power loss (*PDC*), power losses of the diode-bridge rectifier (*PBridge*) and the SS, as calculated in (18).

(18)

For the present DFIG simulated in this paper with total rated capacity of 2 MW, the *idc* is approximately *id\_rms*=600 A. By utilising the proposed SRFCL in series with the DC link of the RSC, with parameters of *rd*=*0.001* Ohm, *Vd*=3 V, the *PTotal-loss* is equal with 5760 W. The ratio of total power loss to the generated active power by the DFIG (*PDFIG*) is defined by *K* and can be derived as follows:

(19)

Equation (19) shows that in the presence of the SRFCL, the total power dissipation is a very small percentage of the overall rated power of the DFIG. The small value of *K* can be acceptable for most practical applications. However, it should be mentioned that by using a superconducting inductor instead of non-superconducting DC inductance in the diode-bridge rectifier of the SRFCL, it is possible to cancel out the power loss of the non-superconducting DC inductance, at the expense of higher initial cost of the super-conducting inductor and the larger weight and volume of the cryogenic system.

## Determining the Value of rp:

The value of *rp* is linked to two main issues. Firstly, the large or small value of *rp* changes the switching frequency of the SS. In other words, if large value of the *rp* is selected, the discharging time constant of the *id* decreases; consequently, the DC inductance quickly discharges in the *rp*. So, the frequency of the SS during the fault current should be considered.

Secondly, the generated heat in the *rp* must be taken into account. To achieve continuous operation of the RSC during the fault, the SRFCL should consume the excess active power of the DFIG. As aforementioned, the fault duration is short in most cases. Therefore, the amount of heat generated in the fault duration can be dispatched after the fault removal. The same operation principle of consuming the output active power of the wind farm by resistance has been utilised on King Island, Tasmania, Australia*,* but this resistance controls the frequency of the power network by consuming the excess active power output of the wind farm. In fact, the wind turbines produce as much power as possible and if generation exceeds consumption, the excess active power output is absorbed by the resistance [36].

## Determining Rating of the SS:

The SS should be able to switch during the high current level of the *id*. It is clear that the switching interval depends on the fault duration being a short time. During this interval, to satisfy the rated voltage and the rated current of the SS, parallel and series connections of the self-turnoff switch can be employed. Up until now, high rating press-pack self-turnoff switches have been introduced for high power applications [37]. Therefore, the SRFCL can be applicable for the high power rating of the DFIG systems.

## Determining the Value of the Ld and the Ic Considering Rating of the Semiconductor Switches:

As mentioned previously, the *Ld* is placed in series with the SS to protect it against severe *di/dt* at the beginning of a fault. So its value can be chosen considering the current characteristic of the SS. Meanwhile, the inherent resistance of the DC inductance, the semiconductor switch, and the diode of the single phase bridge rectifier have small voltage drops. But these voltage drops are almost negligible compared to the DC link voltage. So, the proposed SRFCL has about no impact on the steady state operation of the inverter. The design criterion of the *Ld*and its corresponding equations are studied completely in [30].

According to the analysis carried out in section V, during the normal operation, the *id* equals to the peak of the *idc* and it is employed to control ON /OFF situations of the SS considering the value of the *Ic*. Therefore, in the proposed LVRT method, the current characteristics of the RSC’s SDs must be considered to determine the value of the *Ic*.

1. Simulation Results

A single line diagram of the test system is shown in Fig. 6(f). The DFIG system is connected to the grid through a double-circuit transmission line. The utility grid is represented by a three phase AC voltage source with equivalent impedance of *Zg*. The complete model of DFIG, including mechanical and electrical parts, has been simulated in a PSCAD/EMTDC environment. More details about DFIG modelling can be found in [38]-[39]. The DFIG system specifications are listed in Table I, and the network parameters are given in [40]. To demonstrate the effectiveness of the proposed LVRT scheme, its performance is compared with a conventional crowbar-based protection method. Extensive simulation studies are carried out under different fault conditions, including symmetrical and asymmetrical faults. In the simulation results, whenever the crowbar protection activates, the switching pulses of the RSC simultaneously cease and the rotor over-currents flow toward the DC link through the freewheel diodes of the RSC. Furthermore, for activation of the crowbar and the DC chopper, the threshold is adjusted at 1.05 (*p.u.*) of the DC capacitor voltage level.

Among the different grid codes, “*E.ON*” grid code has strong LVRT requirements [8]. According to the “*E.ON*”, as the voltage at the point of common coupling (PCC) drops to zero for a timeframe 0.15 *s* or less, the wind turbine must not be disconnected from the grid. In all cases, the fault interval is considered 0.15 *s*.

## Symmetrical LLLG Fault

In this scenario, a temporary LLLG fault is applied to the PCC, as shown in Fig. 6(f), at *t=4 s*. The LLLG fault causes severe voltage dip (*p*=100%) at the stator terminal. Fig. 7(a) shows the transient responses of the stator currents of the DFIG during the LLLG fault when the crowbar protection is employed. The stator current increases due to zero voltage at the stator terminal. Furthermore, the severe over-voltage induced in the rotor windings increases the rotor current abruptly. These over-currents reach about 4 (*p.u.*), as shown in Fig. 7(c), and tend to damage the RSC in practical cases. In fact, the active power cannot transfer to the grid due to drops of three phase voltages at the DFIG terminal. Accordingly, the DC-link voltage increases until the fault is cleared (Fig. 7(e)). There are large electrical torque spikes at the moment of fault when the crowbar protection is employed (Fig. 7(g)). In addition, dynamic response of the rotor currents in-quadrature axis, *q*, *iqr*. and in the *d*-axis, *idr* are shonw in Fig. 7(i) and 7(j), respectively. As it is expected, the high spikes and oscilations happen during the LLLG fault.

Fig. 7(b) shows the transient response of the stator current of the DFIG when the proposed LVRT scheme is employed. As Fig. 7(d) reveals, the SRFCL effectively limits the peak of the rotor current to lower than 2 (*p.u.*) and makes the RSC operate continuously during a worst fault scenario. The DC-chopper triggers and regulates the DC link voltage around the nominal value as shown in Fig. 7(e). As Fig. 7(f) shows, the *id* is effectively limited upon the fault occurrence and discharges to its pre-fault value after fault removal. Crowbar triggering in modern DFIG-based wind turbines causes high stress to the mechanical parts of the system, such as the shaft and gear, as shown in Fig. 7(g). In addition considering Fig. 7(g), from the proposed approach, the first peak point of the electrical torque in comparison with the crowbar protection scheme, which would damage the mechanical parts of the DFIG, has been restricted during the initial moments of the fault. Therefore, the proposed approach can increase the life of the turbine shaft and gear box. The SRFCL effectively restrains the rotor speed as is shown in Fig. 7(h). Fig. 7(i) and (j) present the rotor currents in-quadrature axis, *q*, *iqr*. and in the *d*-axis, *idr*, which prove the dynamic response of the rotor current have been improved by the proposed LVRT scheme compared to the crowbar protection. Generally, with the proposed LVRT scheme, the DFIG stays connected to the grid in good operational conditions without the use of the crowbar protection scheme during the LLLG fault at PCC.

## Asymmetrical LLG Fault

As discussed, the DFIG is very sensitive to the asymmetrical gird faults. So to analyse the operation of the proposed approach on the LVRT of the DFIG, the LLG fault (B and C phases to ground) is applied in point F, at *t*=*4* *s*. Fig 7(a) and 7(c) show the stator and rotor currents with the crowbar protection. Like the LLLG fault, the current level increase up to 4 *p.u*. By using the SRFCL, the current level is limited to 2 p.u. both in the stator and the rotor side as shown in Fig. 8(b) and 7(d), respectively. Fig. 8(e) presents the DC link voltage, which is fixed by the operation of the DC chopper. Furthermore, in Fig. 8(f), the DC inductance current is shown. As it is clear, the DC inductance is restricted to the maximum permissible current in fault condition. After fault removal, the DC inductance is discharged to the pre-fault current by its inherent resistance and the voltage drops on the semiconductor switches. The electrical torque variation is presented in Fig. 8(g). By proposed approach, its oscillation is lower than the crowbar protection. Fig. 8(h) shows the rotor speed variation, which proves the effectiveness of the proposed LVRT scheme. Finally, the rotor currents in-quadrature axis, *q*, *iqr*, and in the *d*-axis, *idr*, are shown in Fig. 8(i) and (j) that prove the rotor current components have lower oscillations during the fault especially in *idr* by using the proposed scheme.

## Asymmetrical LG Fault

In this section, the performance of the proposed approach is evaluated during the LG (A phase to ground) fault at the PCC in Fig. 6(f), at *t*=*4* *s*. The transient response of the key variables of the DFIG, when the proposed LVRT scheme is employed during the LG fault, is shown in Fig. 9. It can be seen that, during the voltage sag, the stator current, the rotor current, and its components *iqr*, *idr*, are limited to the maximum permissible current (2 p.u). In addition, the transient response of other variables is controlled during the LG fault. It should be better to mention that, considering Fig. 9(h), with the crowbar protection, there is under-speed condition for the rotor due to supplying the active power to the grid. However, because with the proposed LVRT approach, the RSC operates continuously, the rotor speed increases.



Fig. 7. Simulation results for the LLLG fault at the PCC. The stator current: (a) with crowbar protection, (b) with the proposed LVRT scheme. The rotor current: (c) with crowbar protection, (d) with the proposed LVRT scheme. (e) the DC-link voltage. (f) The *id*. (g) The electrical torque. (h) The rotor speed. (i) The rotor current in-quadrature axis, *q*, *iqr*. (j) The rotor current in the *d*-axis, *idr*.



Fig. 8. Simulation results for the LLG fault at the PCC. The stator current: (a) with crowbar protection, (b) with the proposed LVRT scheme. The stator current: (c) with crowbar protection, (d) the proposed LVRT scheme. (e) the DC-link voltage. (f) The *id*. (g) The electrical torque. (h) The rotor speed. (i) The rotor current in-quadrature axis, *q*, *iqr*. (j) The rotor current in the *d*-axis, *idr*.



Fig. 9. Simulation results for the LG fault at the PCC. The stator current: (a) with crowbar protection, (b) with the proposed LVRT scheme. The stator current: (c) with crowbar protection, (d) the proposed LVRT scheme. (e) the DC-link voltage. (f) The *id*. (g) The electrical torque. (h) The rotor speed. (i) The rotor current in-quadrature axis, *q*, *iqr*. (j) The rotor current in the *d*-axis, *idr*.

## Performance of the Proposed LVRT Scheme at Super-Synchronous and Sub-Synchronous Speed

In super-synchronous speed, active power is delivered to the utility grid through both the rotor and the stator of the DFIG. But, in sub-synchronous speed, the stator only injects active power to the utility grid. Simultaneously, the rotor circuit absorbs active power from the grid through the RSC.The amount of the output power generated by the DFIG is a function of the wind speed. Accordingly, variations in wind speed change the DFIG’s operating mode from super-synchronous speed (for high wind speed) to sub-synchronous speed (for low wind speed), and vice versa [39]. For this purpose, in this section, the performance of the proposed LVRT scheme is evaluated during the LLLG fault at the PCC for two typical wind speeds: 15 *m/s* and 8 *m/s*, which are relevant to the super-synchronous and the sub-synchronous speeds, respectively. Fig. 10 and Fig. 11 show the LVRT behaviour of the DFIG’s important variables for two modes of operation. As these figures reveal, in comparison with the crowbar protection method, by means of the proposed SRFCL-based LVRT scheme, transient and dynamic responses of the key variables of the DFIG system are improved.



Fig. 10. The super-synchronous speed of operation during the LLLG fault at the PCC. The stator current: (a) with crowbar protection, (b) with the proposed LVRT scheme. The rotor current: (c) with crowbar protection, (d) with the proposed LVRT scheme. (e) The DC-link voltage. (f) The *id*. (g) The electrical torque. (h) The rotor speed. (i) The rotor current in-quadrature axis, *q*, *iqr*. (j) The rotor current in the *d*-axis, *idr*.



Fig. 11. The sub-synchronous speed of operation and the LLLG fault at the PCC. The stator current: (a) with crowbar protection, (b) with the proposed LVRT scheme. The rotor current: (c) with crowbar protection, (d) with the proposed LVRT scheme. (e) The DC-link voltage. (f) The *id*. (g) The electrical torque. (h) The rotor speed. (i) The rotor current in-quadrature axis, *q*, *iqr*. (j) The rotor current in the *d*-axis, *idr*.

1. Experimental Results

Fig. 12 shows the single line diagram of the experimental set-up. As mentioned in section V-A, the *Vdc* is almost constant during the fault due to activation of the DC-chopper. So, the DC link capacitor and the DC-chopper are represented by a fixed DC source, which is connected in series with the SRFCL and a three phase voltage source inverter. The aim of the experimental set-up is to prove the effectiveness of the proposed FRT approach in limiting the fault current level in the DC link of a typical inverter as well as in the AC side.

It should be better to mention that, since the fixed DC source has limited rating power, a parallel capacitor is used to prevent voltage drop at input of the inverter, when the current of the DC source increases during fault condition. The capacitor consists of two parallel 470 µF capacitor by itself. The three phase inverter is a superfast NPT-IGBT modules, 50 A, 600 V and 60 Hz. The carrier frequency is 1080 Hz. To generate the switching pulses of the inverter’s IGBTs using SPWM, dSPACE (DS1104) as a real time simulator is employed. The real time simulator can link the simulation model of SPWM developed in MATLAB to the experimental set-up.

Considering “*E.ON*” grid code, the fault duration of 0.15 s is applied to the point F at Fig. 12. To control the fault interval, a three phase TTL controlled switch, 415 V and 16 A, is utilised, which is also trigged through the control signal implemented in MATLAB and dSPACE software tools. The SRFCL includes a single phase diode bridge rectifier, model BR354 400 V and 35 A, and an IGBT switch as the SS, model IKW75N60T, 600 V and 75 A. The *Ld* is 50 mH and its resistance is 0.3 Ω. In addition, the discharging resistance value of the SRFCL is 15 Ω. The waveforms are captured using two four channels Tektronix TDS2024C oscilloscopes. All information about time per division, volt per division and ampere per division are illustrated on the screen of the oscilloscope. The experiment is carried out in three case studies, the LLLG, the LLG, and the LG faults. Fig. 13 shows the experimental results without and with application of the proposed SRFCL for the LLLG. After the LLLG fault happens, without implementing the proposed scheme, the current level in both the DC side and the AC side of the inverter increases up to 7.5 A, as shown in Fig. 13(a) and Fig. 13(b), respectively. The fault current level is 10 times more than the normal current value, which can trip out the inverter in practical cases. Considering Fig. 13(c) and 13(d), the SRFCL ensures that the fault current level of the inverter is restricted to less than 1.5 A during the LLLG. In addition, the *VDC* is shown in Fig. 13(c) together with *idc*.

To evaluate the operational behaviour of the proposed LVRT during the asymmetrical grid faults, the LLG fault is applied to point F for 0.15 s. It is clear from Fig. 14(a) and 14(b), in the DC side and the AC side, the fault current level increases up to 7.5 *A* like the LLLG fault. As shown in Fig. 14(c) and 14(d), by employing the SRFCL, the current level is restricted to 1.5 *A*, and the safe area of operation is achieved for the inverter. Finally, Fig. 15 shows the experimental results for the LG fault. Considering the fault current level, it is obvious that the SRFCL has effective operation during the LG fault.

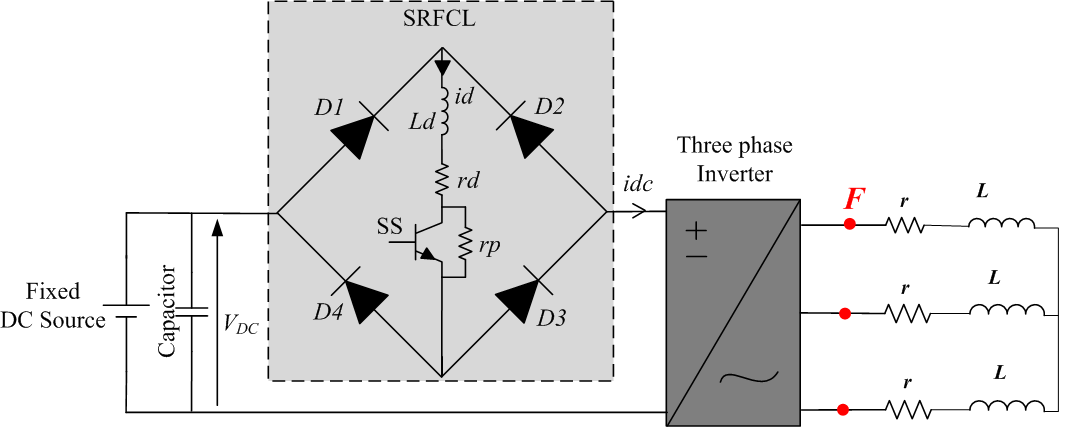


Fig. 12. Single line diagram of the experimental set-up.

|  |  |
| --- | --- |
| J:\Research Paper  22 December\exp\27 April\new pic 27 April\LLLG\F0028TEK.BMP  The DC voltage  The DC-link current  (a) | J:\Research Paper  22 December\exp\27 April\new pic 27 April\LLLG\F0022TEK.BMP  The DC voltage  The DC inductance current  The DC-link current  (c) |
| J:\Research Paper  22 December\exp\27 April\new pic 27 April\LLLG\F0029TEK.BMP  (b) | J:\Research Paper  22 December\exp\27 April\new pic 27 April\LLLG\F0023TEK.BMP  (d) |

Fig. 13. Experimental results for the LLLG fault at point F: without utilizing the SRFCL (a) The *VDC* and *idc*, (b) the output AC currents of the inverter. By employing the proposed SRFCL: (c) The *VDC*, *idc*, and *id*, (d) the output AC currents of the inverter.

|  |  |
| --- | --- |
| J:\Research Paper  22 December\exp\27 April\new pic 27 April\LLG\F0030TEK.BMP  The DC voltage  The DC-link current  (a) | J:\Research Paper  22 December\exp\27 April\new pic 27 April\LLG\F0024TEK.BMP  The DC voltage  The DC inductance current  The DC-link current  (c) |
| J:\Research Paper  22 December\exp\27 April\new pic 27 April\LLG\F0031TEK.BMP  (b) | J:\Research Paper  22 December\exp\27 April\new pic 27 April\LLG\F0025TEK.BMP  (d) |

Fig. 14. Experimental results for the LLG fault at point F: without utilizing the SRFCL (a) The *VDC* and *idc*, (b) the output AC currents of the inverter. By employing the proposed SRFCL: (c) The *VDC*, *idc*, and *id*, (d) the output AC currents of the inverter.

|  |  |
| --- | --- |
| J:\Research Paper  22 December\exp\27 April\new pic 27 April\LG\F0032TEK.BMP  The DC voltage  The DC-link current  (a) | J:\Research Paper  22 December\exp\27 April\new pic 27 April\LG\F0026TEK.BMP  The DC voltage  The DC inductance current  The DC-link current  (c) |
| J:\Research Paper  22 December\exp\27 April\new pic 27 April\LG\F0033TEK.BMP  (b) | J:\Research Paper  22 December\exp\27 April\new pic 27 April\LG\F0027TEK.BMP  (d) |

Fig. 15. Experimental results for the LG fault at point F: without utilizing the SRFCL (a) The *VDC* and *idc*, (b) the output AC currents of the inverter. By employing the proposed SRFCL: (c) The *VDC*, *idc*, and *id*, (d) the output AC currents of the inverter.

1. Conclusion

This paper proposes a novel concept of the FCL application in the field of the LVRT of the DFIG. The proposed SRFCL employs just one single set of the SRFCL in the DC side of the RSC to limit high rotor over-currents during various grid fault conditions. Therefore, it is more efficient than conventional approaches, which need three similar sets of the FCL at the AC side of the DFIG. In the proposed scheme, thanks to the SRFCL, the LVRT capability is applied to a basic configuration of the RSC, which makes the proposed scheme easy to be implemented by industry. The SRFCL has simple power circuit topology. The proposed approach is not affected by the depth of the voltage dip. With the present method, continuous operation can be achieved for the DFIG even at zero grid voltage during the fault condition. From the extensive simulation studies carried out in PSCAD/EMTDC software, it is proved that the proposed scheme can provide promising performance during the symmetrical and asymmetrical grid faults. Moreover, the main concept of the proposed method has been experimentally studied with a prototype setup. The obtained results show that the proposed LVRT configuration could eliminate the crowbar activation problems and subsequent complications in the DFIG-based wind turbines and enable the DFIG to remain connected to the utility grid during the PSFs.

Table I

Simulated DFIG System Specifications

|  |  |  |
| --- | --- | --- |
| Generator data | | |
| Rated Power | 2 MW | |
| Rated Stator Voltage | 690 V | |
| Rated Frequency | 60 Hz | |
| Stator leakage inductance | 0.12 p.u. | |
| Rotor leakage inductance | 0.12 p.u. | |
| Magnetising Inductance | 3.45 p.u. | |
| Stator to Rotor turns ratio | 0.35 | |
| Stator resistance | 0.011 p.u. | |
| Stator inductance | 0.012 p.u. | |
| Generator inertia constant | 0.85 s | |
| Other data | | |
| Rated DC-link voltage | | 1200 V |
| DC bus capacitor | | 50 mF |
| Resistance of grid side filter | | 0.3 p.u. |
| Reactance of grid side filter | | 0.003 p.u. |
| Nominal wind speed | | 13 m/s |
| DC-chopper resistor | | 0.5 Ω |
| Crowbar resistance | | 0.3 Ω |
| The DC inductance | | 0.01 H |
| Inherent resistance of the DC inductance | | 0.01 Ω |
| Voltage drop across the diode bridge of the SRFCL | | 3 V |

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