I PULSE-CODE MODULATION

II EQUIPMENT INCIDENTAL TO MAIN PROJECT

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THESIS - "PULSE-CODE MODULATION" - by G.V. Dunne

ERRATA

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1. The word "quantized" has been consistently misspelt "quantitized".

2. Page 1/8, last paragraph, line 4 should read:
"... pulses of unit amplitude, width τ and ..."

3. Page 1/9, paragraph 2, lines 8, 9 should read:

$$F_s(j\omega) = \int_{-\infty}^{\infty} F(\lambda).\ S(j\omega - \lambda)\ d\lambda$$

$$= \int_{-\infty}^{\infty} F(\lambda).\ \sum_{n=-\infty}^{\infty} \delta\left(j\omega - j\frac{2\pi n}{T} - \lambda\right)\ d\lambda$$

4. Page 1/10, paragraph 3, lines 7, 8 should read:
"... represents the ratio of the sampling-pulse width to period"

5. Page 1/13, paragraph 2, line 8 should read:
"peak signal to rms noise is $\sqrt{12}$ s, and the ..."

6. Page 1/14, paragraph 2, line 8 should read:
"... when none was sent or of its causing a pulse to be deleted".

7. Page 2/1, paragraph 2, line 4 should read:
"...The type of information which must accompany..."

8. Page 2/1, paragraph 5, line 5 should read:
"...which scanned the mask in..."

9. Page 2/3, paragraph 1, line 1 should read:
"...be compared with the input and used to stop..."

10. Page 2/5, paragraph 2, line 11 should read:
"...every negative difference to no digit..."

11. Page 2/6, paragraph 3, line 2 should read:
"on the accuracy of the weighted voltages..."

12. Page 2/10, paragraph 2, line 1 should read:
"...obeys equation 1"

13. Page 2/13, paragraph 4, line 5 should read:
"...can react to change and on the gain..."

14. Page 3/10, paragraph 2, insert between lines 5 and 6:
"16 possible four-input AND gates to give"

15. Page 3/13, paragraph 5, line 7 omit "by all the stores"

16. Page 3/13, paragraph 5, line 9 should read:
"...voltages to decrease in"

17. Page 3/18, paragraph 2, line 3 should read:
"...clamp capacitor",

18. Page A/2, equation leading to equation 10) should read:

$$g(t) = \frac{1}{2\pi} \int_{-2\pi B}^{2\pi B} f\left(\frac{n}{2B}\right).\ \tau\ .\ e^{j\omega\left(t-(t_0+t_1)\right)}\ d\omega$$

19. Page D/1, paragraph 5, line 1 should read:
"Although the analyses have ....."

CONTENTS

This thesis describes work done on the Electrical Engineering Department of the University of Tasmania from April 1959 until March 1960 under the supervision of Professor G.H. Newstead.

At that time the Department was concerned with providing equipment for telemetry of very low frequency seismic data from remote stations in Tasmania. In support of a proposal that PCM transmission be used due to its claimed high noise-immunity, a theoretical investigation of the characteristics of PCM was carried out, and simple transistorized equipment was developed for this application: a coder and decoder for the data, and regeneration and synchronization equipment for the transmission link.

Other equipment concerned with the instrumentation of geological work was designed and built for the Department during this period. It included a portable unit for measuring borehole temperatures, standard time-signal equipment for the laboratory and high-current regulated power supplies for transistorized equipment.

When this work was undertaken the use of transistors was very restricted and little experience had been gained in the Department in their application. Consequently, this thesis reports some of the early transistor circuit development in the University of Tasmania.

INTRODUCTION:

Pulse-code modulation is an appealing topic. It has interesting theoretical aspects, leading into the fields of information and communication theory, and its practical relization involves a rare combination of analogue and digital techniques in which the circuit designer can exercise his ingenuity. Work on both these facets of PCM is reported here.

In the first Section the history of the development of pulse-code modulation (PCM) is surveyed and its important characteristics are considered theoretically.

The second Section contains descriptions of practical methods for achieving the coding operation, for synchronizing the demodulator with the modulator, and for regenerating distorted pulses.

The equipment which was designed and built for the project is described in Section 3, together with its performance as a synchronized coder and decoder.

In Section 4 an interesting result of the Sampling Theorem is investigated and given experimental illustration by use of the PCM equipment.

Appendices A, B, C and D contain, respectively, a proof of the Sampling Theorem, an analysis of some of the circuits, a graphical construction for waveforms relating to Section 4, and other applications for the synch detector described in Section 2.

1.1 Historical Survey of PCM Development

Pulse-code modulation (PCM) was invented in 1937 by Reeves[1] in the French laboratories of a telephone and telegraph company. He has been seeking to obtain for speech transmission the digital advantages of telegraphy, namely pulses of fixed height which may be regenerated as often as desired along communication links. Another advantage which he realised was the inherent suitability of the method for time-division multiplexing of many signals on one channel.

The first practical work on PCM was done in the Bell Telephone Laboratories in USA, and published in 1947 when Goodall[2] and Black[3] described many of the basic principles of PCM and

outlined the equipment used in their system. The advantages of PCM were also put forward by Black and Edson[4,5] in an early theoretical treatment. Panter et al from the ITT Company were concerned with the effects of coding, and published two papers[6,7] on quantitization noise and distortion of speech.

A major contribution to PCM development came from Meacham and Peterson of Bell Laboratories who announced[8] the first experimental multichannel link technically good enough for use in existing telephone systems, but although they quoted performance data for the link the equipment was not detailed. However, Sears[9] gave a description of an electron-beam coding tube in the same journal, and later Carbrey[10] showed a simple circuit, called the Shannon-Rack decoder, for decoding binary pulses, and it is highly probable that these were the devices used by Meacham.

In 1948 a large amount of material on communication and information theory was being published[11,12,13,14,15] and PCM was receiving a theoretical analysis[16,17,18] when the classic summary of its properties was given by Oliver, Pierce and Shannon[19] in terms of the work of Nyquist and Hartley. They explained the processes of sampling, quantitization and coding, and showed how coding improved the noise threshold and used the needed extra bandwidth to better purpose in signal-to-noise ratio return than FM. Several other authors[20,21,22,23,24], all concerned with speech transmission, turned to methods of reducing coding noise by the use of unequal quantitizing levels. Thus, by the end of 1948 most of the factors required for long-distance speech communication by PCM were well realized. But, after two papers[25,26] dealing with the signal-to-noise ratio improvement of PCM over other modulation methods, the literature on theoretical aspects became suddenly vacant for

about four years until Villars[27] gave further work on coding and Page[28] and Nichols[29] mentioned PCM in comparing different methods of multiplexing and modulation.

Implementation aspects of PCM also showed a pause of about four years after Ostendorf's 1949 description[30] of the principles of a pulse-regenerator for repeater stations. However, an important paper on binary coding, not then related to PCM, was published in 1949 by Barney[31] who described in detail an original analogue-to-digital converter using a tracking up/down counter and analogue feedback. The gap was ended when Oxford[32,33] published the first work done on PCM speech transmission outside a telephone company. He described a novel coding and decoding system in terms of mechanical switches, and claimed that electronic switching had been successfully achieved. The matter of synchronization was also discussed for the first time.

About that time (1952), work was starting on analogue-to-digital conversion, but not in connection with PCM development. This process is identical to the quantitizing and coding needed to produce PCM, although the codes may differ. Lippel[34,35,36] and Burke[37] analysed the fundamental processes involved, but although they listed many methods only one gave promise as a high-speed voltage encoder. Smith[38] contributed a basic paper on the method of coding by feedback(forseen by Barney) which is necessary to obtain high accuracy. The first record of the use of a transistorized circuit in digital conversion came from Follingstad et al[39] in 1952, although their equipment was an optical position encoder and did not have great relevance to PCM coders.

In succeeding years little more appeared in the literature on accurate high-speed analogue-to-digital converters. Presumably vacuum tubes were not sufficiently good electronic switches for analogue signals, and transistors were still being developed, for between 1955 and 1957 low-level switches using transistors were being reported[40,41,42,43]. Only one reference, by Bishop

and Marquand[44], described PCM equipment. Their system employed vacuum tubes, but it was the first to be made for telemetry purposes and, furthermore, the code format was chosen to suit direct data-processing in the ERA 1103A digital computer. Subsequent transistorizing of this equipment led to the first high-speed high-accuracy multiplexed PCM system, described by McMillian[45] and Marquand[46,47] in 1957. These articles were detailed in regard to the multiplexing and coding techniques, but the method of synchronization was not included. Another practical and useful publication was the collection by Susskind[38] of many of the up-to-date methods for analogue-to-digital conversion.

Meanwhile, reports of both theoretical work on coding[48] and redundant codes[49,50,51,52,53], and practical work on systems[54,55,21] re-appeared from telephone companies. One subject which was treated in detail[56,57,58,59,60,61], and which produced some published circuits, was that of regenerative repeaters for long communication links, and another was companding of speech signals[20,62]

The first proposal for improving on PCM's characteristics came from Bedrosian[63] in 1958 when he showed that PCM could yield transmission rates even closer to the theoretical maximum if the code pulses were weighted in amplitude before transmission. This suggestion is simple to put into practice, but it will probably be regarded for some time as an unnecessary refinement.

By the end of 1958 the literature showed that a few large PCM systems had been built by telephone companies and had come up to expectations. The theory of PCM was also well established. However, there was a great lack of practical detail about the equipment, and the little that was published came from sources other than telephone companies. Of the latter contributions, only one demonstrated the successful application of transistors to multiplexing and coding.

It may be said that PCM development was retarded, in view of its fulfilling the need for which it was invented. This

was probably because its concepts were too different from those of telecommunication practice at the time, and because the sampling and coding processes could not be achieved satisfactorily with available components. The demands of World War 2, which spurred technological progress in many other fields, did not seem to produce any useful results on PCM. Perhaps the difficulty until recently has still been that of simple implementation, but it is surprising that the advantages of PCM have not brought more widespread development and application.

1.2 The Characteristics of PCM

Pulse-code modulation is a sophisticated communication technique which alters the nature of the signal to be sent to a receiver in such a way that the effect of noise added by the link is less than for other modulation methods. Basically, it involves sampling the amplitude of the input signal repetitively and converting each sample into a coded group of pulses which are transmitted in the period between samplings. The information is carried in the pattern of the pulses, and at the receiving end of a link the original information can be extracted by decoding the pattern, provided that the code is known there. Since the code will be prearranged, it does not need to be transmitted over the link. The improved signal-to-noise ratio for PCM is achieved at the expense of the bandwidth needed to carry the code pulses.

In the explanation which follows, the coding will be considered binary; that is, the code group consists of pulses which have only two possible levels - present or absent. The original invention used a binary code deliberately for practical reasons, and it will be shown in Section 1.7 that even though codes with other bases may be used the binary code yields the greatest advantage in most communications systems.

Since only a finite number of code pulses can be transmitted between samplings, the sample must be represented to a limited accuracy. The smallest possible change to one pulse group is a change in one pulse - an extra pulse where there was

none, or one less pulse. Therefore, the coded representation of the sample must change discretely, and the decoded version will at best be a quantitized, or stepped, approximation to the input sample. The error can be made as small as desired by allowing more pulses in the code, but this requires more pulses between samples and hence increases the bandwidth needed to transmit the code. Coding therefore introduces into the modulation process an unavoidable quantitization error which may be classed as noise. The nature of this noise will be considered in Section 1.6.

Sampling of a signal also produces a discontinuous output - in this case, discontinuous in time. However, unlike amplitude quantitization, there need be no error introduced, provided that the sampling rate is sufficiently high: the Sampling Theorem claims that no information is lost if the signal is sampled at a rate equal to at least twice the highest frequency present in the signal. This Theorem is discussed in Section 1.3 where it is also shown that all that is needed to regain the original signal after sampling is a low-pass filter. The sampling process is ideally suited to time-multiplexing, for several different input signals may be sampled and coded in cyclic order and transmitted on the one channel.

A PCM system also needs synchronism between the coder at the transmitter and the decoder at the receiver so that the code can be interpreted correctly. Synchronization information must be transmitted over the link, and it therefore encroaches on the bandwidth available for the signal. However, synchronization is not a requirement unique to PCM, because any sampled or time-multiplexed system needs a means of separating and distributing the successive frames at the receiver.

The advantage provided by PCM in return for the wider bandwidth, the coding error and the more complex equipment was seen intuitively by its inventor: since the receiver has to distinguish between only the presence and the absence of a pulse, high quality transmission is possible using much lower signal-to-noise

power ratios than other modulation methods allow. In fact, it will be shown in Section 1.7 that for a received signal-to-noise ratio greater than 20 db the probability of error is less than 10^{-8}, corresponding to one error every minute for speech transmission, which is virtually noiseless. The figure of 20 db compares very favourably with the 60-70 db generally considered necessary for high-quality AM transmission. Thus PCM may be used to great benefit on low-grade links. It will also be shown in Section 1.8 that PCM makes the best bargain in exchanging transmitted power for bandwidth, compared with other wideband modulation methods.

An allied advantage of binary pulses is a reduction in the number of repeaters needed on a long link, because, provided the signal-to-noise ratio at each input is greater than 20 db, the signal can be completely regenerated at each station, and the noise acquired between stations does not accumulate.

Despite the claims in favour of PCM, however, it is not necessarily the best modulation method for a particular link. For example, in situations where the signal-to-noise ratio is high, FM may be preferable because above the threshold the signal-to-noise ratio continues to improve for FM, but for PCM the improvement is not significant; it is then that the complexity of PCM equipment weighs against it.

1.3 Sampling

All pulse-modulation methods - PAM and PPM as well as PCM - require the process of sampling in their production. PAM is, in fact, a step in the production of PCM, where it is followed by quantitization and coding. The sampling process and its limitations will therefore be shown from a consideration of PAM, which is easy to visualize.

If the AM carrier is changed to a series of periodic narrow equal-amplitude pulses, the modulation results in a series of narrow amplitude samples of the input signal, which constitutes PAM. The Sampling Theorem guarantees that these

samples contain sufficient information to permit exact re-construction of the input signal, provided that the sampling rate is at least twice the signal bandwidth. This result is not really remarkable, because the Fourier series which describes a signal band limited to fc/s needs 2f coefficients per second, and therefore gives sufficient information at the same rate.

Nevertheless, a rigorous proof of the theorem will be given in Appendix A, and it will also be given here in an illustrative manner. Furthermore, it will be shown that the original signal can be regained from the PAM signal simply by use of a lowpass filter of cutoff frequency equal to the original signal bandwidth.

The consequences of using too low a sampling rate are very important: spurious signals then appear in the baseband, and they cannot be removed with a filter, or any other means. This fact is considered in detail in Section 4, where experimental verification is given.

It is a wise precaution to deliberately band limit the input to the sampler so that unexpected transients cannot cause malfunctioning, and also, since practical filters are not ideal, to allow a guard band by making the ratio of sampling frequency to filter bandwidth greater than the minimum value of two.

The spectrum of PAM depends upon the width of the sampling pulses and on their rate. Suppose the sampling signal s(t) is a periodic series of pulses of unit amplitude, width , and period T which can be represented as the Fourier series

$$s(t) = \frac{1}{T}\sum_{n=-\infty}^{\infty} c_n e^{j\frac{2\pi n}{T}t}$$

$$= \frac{\tau}{T}\sum_{n=-\infty}^{\infty}\left\{\frac{\sin\frac{2\pi n}{T}\tau}{\frac{2\pi n}{T}\tau}\right\} e^{j\frac{2\pi nt}{T}},$$

by expansion of coefficients,

$$= \frac{\tau}{T}\left\{1 + 2\sum_{n=1}^{\infty}\frac{\sin 2\pi n\frac{\tau}{T}}{2\pi n\frac{\tau}{T}}\right\} \cdot \cos\frac{2\pi nt}{T}\Big\}. \qquad \ldots\ldots 1)$$

Then the signal after sampling is

$$f_s(t) = f(t).s(t)$$

$$= d.f(t).\left\{1+2\sum_{n=1}^{\infty}\frac{(\mathrm{Sin}2\pi nd)}{2\pi nd}\cos\frac{2\pi n_t}{T}\right\} \quad \ldots 2)$$

where $d=\frac{\tau}{T}$ is the duty cycle of the sampler. This consists of the original signal together with sideband terms distributed about the harmonics of the sampling frequency, the amplitudes of sidebands decreasing with n as $\frac{\sin\pi dn}{\pi dn}$. The spectrum is sketched in Figure 1.1 for the case where the bandwidth of f(t) is much less than $\frac{1}{T}$.

As the width of the sampling pulses is decreased, $d\to 0$, and $\frac{\sin\lambda dn}{\pi dn}\to 1$ regardless of n, so the spectrum of $f_s(t)$ becomes less weighted. However, the energy which is put into the higher sidebands is taken from the lower ones, as can be seen from the factor d multiplying f(t) in equation 2). Also as $d\to 0$, s(t) approaches a series of delta-functions, and in the limit the spectrum of $f_s(t)$ can be found by convolving the transforms F(jw) and S(jw):

$$F_s(jw) = \int_{-\infty}^{\infty} F(\lambda).s(jw-\lambda)d\lambda$$

$$= \int_{-\infty}^{\infty} F(\lambda).\sum_{n=-\infty}^{\infty}\left(jw - j\frac{2\pi n}{T} - \lambda\right)d\lambda$$

$$= \sum_{n=-\infty}^{\infty}\int_{-\infty}^{\infty} F(\lambda)\,\delta\left(jw - j\frac{2\pi n}{T} - \lambda\right)d\lambda$$

$$= \sum_{n=-\infty}^{\infty} F\left(jw - j\frac{2\pi n}{T}\right)$$

by definition of the delta-function $\ldots 3)$

This represents a set of f(t) spectra distributed about $n\frac{2\pi}{T}$, the harmonics of the sampling frequency, with no amplitude weighting of the sidebands, as predicted. Each sideband actually has zero amplitude because the correct sampling pulses have unit amplitude rather than the infinite value of the delta-function.

From the spectrum of the output there can be seen an upper limit of f_m, the bandwidth of the input, before the modulation process causes distortion by overlapping the fundamental signal components with the first lower sideband. The limit is $f_m \leqslant \frac{1}{2T}$, or, in other words, the sampling frequency must be greater than

twice the bandwidth of the input. This is equivalent to requiring at least $2f_m$ uniformly-spaced samples per second in order not to destroy the information in the input, which is a statement of the Sampling Theorem for periodic sampling of a band-limited signal.

Since the input information is carried in any sideband of the PAM signal, the obvious way to demodulate $f_s(t)$ is to pass it through a low-pass filter with a cutoff of $\frac{1}{2T}$ c/s, as shown in Figure 1.2 The filter has the same characteristic as the bandlimiting filter in front of the modulator, and again if the minimum sampling rate has been used, $f_m = \frac{1}{2T}$, and an impossible filter is required.

A rigorous proof is given in Appendix A showing that f(t) may be reconstructed from samples taken at intervals of T seconds, provided, of course, that $\frac{1}{T} < 2f_m$, and also showing that a low-pass filter is sufficient to do this. This proof shows that the filter output is

$$g(t) = \frac{\tau}{T} f(t),$$

where the factor $\frac{\tau}{T}$ represents the ratio of the filter to the sampling-pulse bandwidths.

If $\tau \ll T$ most of the energy of $f_s(t)$ lies outside the filter bandwidth (see Figure 1.1) and the demodulation process is very lossy. A simple demodulator can be made with a boxcar or voltage-holding circuit (see Section 3.2.2) which stores the amplitude of the sample until the next sample is received. In this way it stretches the sample width τ to the sample period T, and therefore, from previous considerations, it applies to the spectrum of $f_s(t)$ a $\frac{\sin n\pi d}{n\pi d}$ filter. Since τ has been widened to T, d = 1, and the filter has zero transmission at frequencies $\frac{n}{T}$, the harmonics of the sampling frequency. This response is sketched in Figure 1.3 superimposed on the spectrum of $f_s(t)$, and it can be seen there that the boxcar circuit by itself is a poor filter for demodulation purposes, its response being down to only $\frac{2}{\pi}$ of its peak value at half the sampling frequency. It therefore needs a further low-pass filter if the permissible signal band-width is to be utilized. Nevertheless, the boxcar

has a transmission of approximately unity over most of the signal bandwidth and it prevents the losses involved in a linear filter demodulator at the expense of a slight signal spectrum distortion.

1.4 Quantitization and Coding

An example of a continuous signal and its quantitized version is shown in Figure 1.4. The maximum swing of the signal is A volts, and the quantitizing levels are equally separated by a volts, so that the quantitized signal may take on $s = \frac{A}{a}$ possible values. If the signal lies within $\pm \frac{a}{2}$ of any level, it is given the value of that level.

Once a signal has been quantitized it is impossible to restore the continuous form exactly, and the resulting random error is called quantitization noise. The nature of this noise is considered in Section 1.6.

Numbering the levels to some base provides a code for representing the instantaneous value of the quantitized signal. Lower bases result in code digits which have fewer possible values, and the binary, or base -2, code results in digits which can have only the two values 0 or 1. Figure 1.5 shows successive binary numbers in positional notation: the right-hand digit, if a 1, has a "weight" of 2^0; the next digit to the left has a weight 2^1; the next, 2^2; and so on until sufficient digits have been used which can represent the desired number. The decimal equivalents of these binary numbers may be obtained by summing the contributions from each position. As an example,

$$101 = 1.2^2 + 0.2^1 + 1.2^0 = 4 + 1 = 5$$

In general, n digits in a system of base b can represent b^n levels, so that higher base coding uses less digits but each digit has more possible values.

The code digits corresponding to the level number are made into a PCM pulse-group by generating a pulse for each digit and giving each digit the required number of possible levels. For binary coding the pulses must represent either 0 or 1, that is, they are either absent or present. The pulses must also be placed in a pattern which has a positional significance so that the correct weight may be given to each. If the pulses are

placed serially in time with the least significant digit last, the appearance of the code group corresponds directly to the binary number equivalent, as shown in Figure 1.6 (a) for a four-digit code. The same value in ternary (base-3) code is shown in Figure 1.6 (b). Only three digits are needed, but each may have three values.

It is not essential to code the levels in a numerical order, nor to place the least significant digit last: any unique correspondence between the level and its code is sufficient. The cyclic or reflected code has a sometimes-useful property that the codes for successive levels differ by only one change in any of the digits. The coding may also be made redundant by using more digits than the minimum in order to detect or even correct noise errors in the received code by means of patterns which were not transmitted.

1.5 Coding and Bandwidth

In Section 1.3 it was shown that when a signal of bandwidth f c/s is sampled, 2f samples of it per second are needed. It will be shown that 2f pulses per second can be accommodated on a channel of bandwidth f c/s. This means that transmission of the samples does not require any extra bandwidth. However, when the sample is represented by a code group of n pulses, 2nf pulses per second are produced, and a bandwidth of nf is needed on the channel. Thus the price paid for coding is an increase in bandwidth proportional to the number of pulses in the code. Higher-base codes need less digits to represent the same number of quantization levels, but they lose the low-threshold benefit of lower-base codes; in fact, it will be shown in Section 1.7 that the signal power needed to remain above the threshold increases roughly as the square of the code base, which means that binary coding makes the most efficient use of the extra bandwidth.

To show that 2f pulses per second can be transmitted over a channel of bandwidth f c/s, consider each received pulse to have the form

$$\frac{\sin \pi \left(\frac{t-mT}{T}\right)}{\pi \left(\frac{t-mT}{T}\right)}$$

where $T = \frac{1}{2f}$ is the period between pulses. This is the form of the pulse response of a low-pass filter with cutoff at f c/s. The nature of this function of t is that its value is zero at multiples of T from its centre, so that if the received pulses are sampled at the instants mT the only contribution to the output comes from the pulse occurring at that time. The pulses may therefore be detected independently, and the bandwidth of the channel is sufficient.

1.6 Quantitization Noise

The error produced by quantitization may be classed as noise, but it differs from thermal noise in having an amplitude distribution limited to $\pm \frac{a}{2}$ (Figure 1.4). However, if it is assumed that all instantaneous values within this range are possible, the mean squared value of the error voltage is

$$\overline{\varepsilon^2} = \frac{1}{a} \int_{-\frac{a}{2}}^{\frac{a}{2}} \varepsilon^2 \, d\varepsilon = \frac{a^2}{12} .$$

Since the maximum signal swing is A = as, the ratio of peak signal to rms noise is 12 s, and the corresponding power ratio is

$$\frac{S}{N} = 12 s^2 = 12 b^{2n} \qquad \ldots 4)$$

for a code group of n pulses each having b levels (Section 1.4.) Now, the bandwidth is proportional to n, so that the quantitization signal-to-noise ratio increases exponentially with bandwidth (or decibel S/N increases linearly with bandwidth).

This result differs from the linear increase given by uncoded wideband modulation. In FM, for example, doubling the S/N, that is, the precision of the signal representation, requires doubling the signal amplitude, which doubles the frequency deviation and hence also the bandwidth. In binary PCM, doubling the bandwidth permits twice as many code pulses, which squares the number of quantitization levels which may be used.

Equation 4) is tabulated in decibels for values of s in Figure 1.7. It can be seen that binary coding to 64 levels gives a signal-to-noise ratio of 47 db, which corresponds to good

intelligibility of speech. A further improvement in S/N may be made for signals which, like speech, have a wide dynamic range, by relating the quantitization error to the signal amplitude. Unequal quantitization spacings grading from fine at low levels to coarse at high levels may be simulated by amplitude compression of the input signal prior to linear quantitization, and this technique using a logarithmic taper has been used effectively on telephone systems.

1.7 Signal Threshold and Error Rate

By coding the information so that the transmitted pulses have fewer possible levels, PCM achieves a better signal-to-noise ratio for the same bandwidth than other modulation methods. It also produces a sharp threshold in signal level above which detection is almost error-free and below which the performance deteriorates rapidly. This will be shown for binary pulses by considering the probability of noise being mistaken for a pulse when none was sent or causing a pulse to be deleted.

For binary pulses of amplitude A, the presence or absence of a pulse is decided by whether the received signal is greater or less than $\frac{A}{2}$ at the sampling instant. For gaussian noise of rms value σ, the probability that the noise voltage will exceed $\frac{A}{2}$ is

$$P(v>\tfrac{A}{2}) = \int_{\frac{A}{2}}^{\infty} \frac{1}{\sqrt{2\pi}\,\sigma} e^{-\frac{v^2}{2\sigma^2}}\, dv .$$

If a pulse is also present, the error probability corresponds to the pulse and noise together dropping below $\frac{A}{2}$:

$$P(v<\tfrac{A}{2}) = \int_{-\infty}^{\frac{A}{2}} \frac{1}{\sqrt{2\pi}\,\sigma} e^{\frac{-v^2}{2\sigma^2}}\, dv .$$

The two probabilities given by these equations are equal due to the symmetry of the distribution, so the probability of error is

$$P = \tfrac{1}{2} - \frac{1}{\sqrt{\pi}} \int_0^{\frac{A}{2\sqrt{2}\sigma}} e^{-\lambda^2}\, d\lambda .$$

On the basis that pulses have a probability of occurrence of $\frac{1}{2}$ in a long message, this equation gives the probability of an error in the detection of any code digit. It is plotted in Figure 1.8 A distinct threshold in the region of 20 db is evident, above which

the error probability falls below 10^{-8} and below which it rises rapidly to 10^{-4}. For a pulse rate of 100 kc/s, as might be used for speech transmission, these correspond roughly to an error every 20 minutes and every second, respectively. Thus, even though the noise power has been increased by the wider bandwidth, PCM requires much less signal power at threshold than AM, for which the corresponding error-rate requires about 60-70 db.

The above proof may be repeated for pulses coded to a higher base. The separation between the b possible pulse amplitudes must then be adequately larger than the noise to keep the error-rate down, and it has been shown[19] that the average signal power needed to do this is

$$S = k^2 N (b^2-1)/12, \qquad \ldots\ldots 5)$$

where k is a factor related to the allowed error rate and N is the noise power in the coded-signal bandwidth. The greatest coding efficiency-in terms of signal power required to reach the threshold - is obtained for the minimum value of b, corresponding to binary coding, and the power rises nearly as the square of the code base.

1.8 Efficiency of Bandwidth Utilization

It was shown in Section 1.7 that PCM, through its coding, exchanges bandwidth for power, and that the best exchange is obtained with binary coding. The efficiency of this exchange can be assessed by comparing the information capacity of a PCM system with the theoretical limit for a channel with the same bandwidth and power.

The information capacity of an ideal channel is expressed by a relationship due to Shannon[11]

$$C = B \log_2 \left(1 + \frac{S}{N}\right) \text{ bits per second} \qquad \ldots\ldots 6)$$

where S is the average signal power and N is the white-noise power in the channel bandwidth B c/s. This shows that the ideal trade of power for bandwidth is exponential.

In the PCM system with an input signal band limited to f c/s and sampled at the minimum rate, 2f samples per second are produced. Each sample must be quantitized to one of s levels,

and if all levels are equally likely each sample carries $\log_2 s$ bits of information. The rate of transmission from the quantitizer is therefore

$$C = 2f \log_2 s \text{ bits per second}$$

Since the coder does not change the rate of information flow, but converts the s levels into n pulses each permitted b levels,

$$C = 2f \log_2 b^n$$

$$= nf \log_2 b^2 \text{ bits per second}$$

Now, 2 nf is the actual pulse rate from the coder, and is ideally twice the channel bandwidth (Section 1.5). Therefore

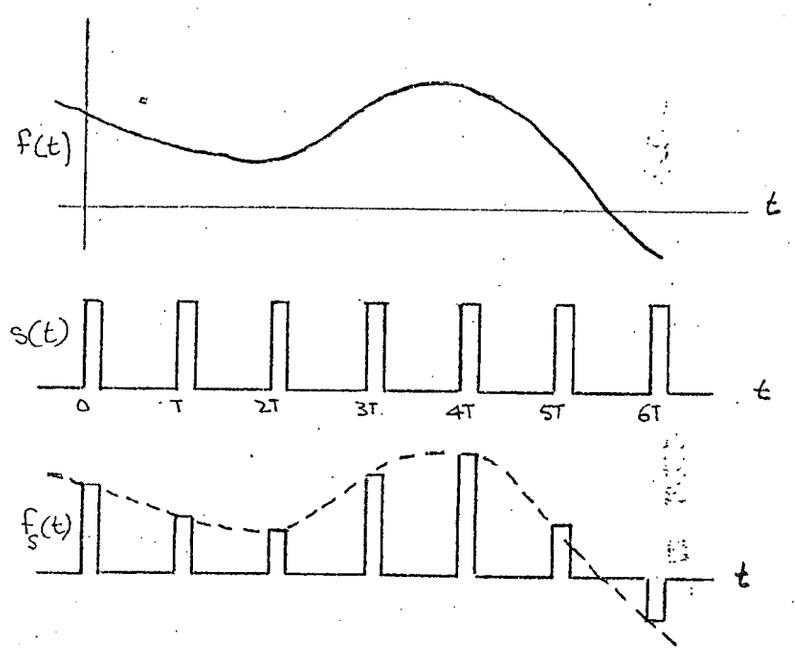
$$C = B \log_2 b^2 \text{ bits per second}$$

Substituting for b^2 from equation 5),

$$C = B \log_2 \left(1 + \frac{12S}{k^2 N}\right) \text{ bits per second} \qquad \ldots.7)$$

Comparison of the PCM capacity (equation 7) with the ideal figure (equation 6) shows a similarity of form, so that in PCM power and bandwidth are exchanged on the ideal exponential basis.

The comparison also shows that PCM requires $\frac{k^2}{12}$ times more power than the ideal system to achieve the same capacity. Shannon has shown that this factor is about 8 times (9 db) for binary coding.


f(t)
t
s(t)
0
T
2T
3T
4T
5T
6T
t
$f_s(t)$
t

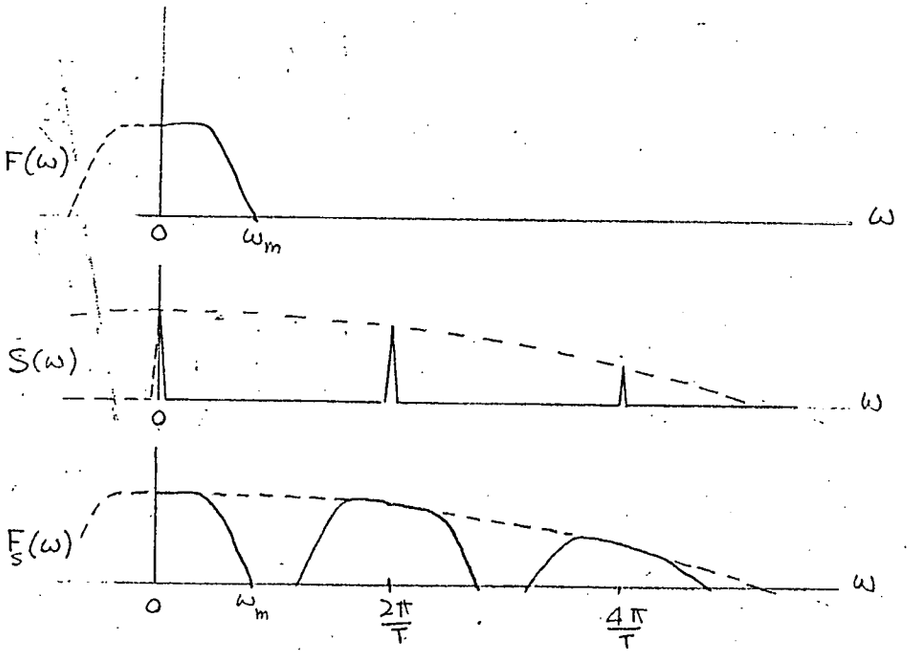

F(ω)
0
ω_m
ω
S(ω)
0
ω
$F_s(\omega)$
0
ω_m
$\frac{2\pi}{T}$
$\frac{4\pi}{T}$
ω

FIGURE 1-1

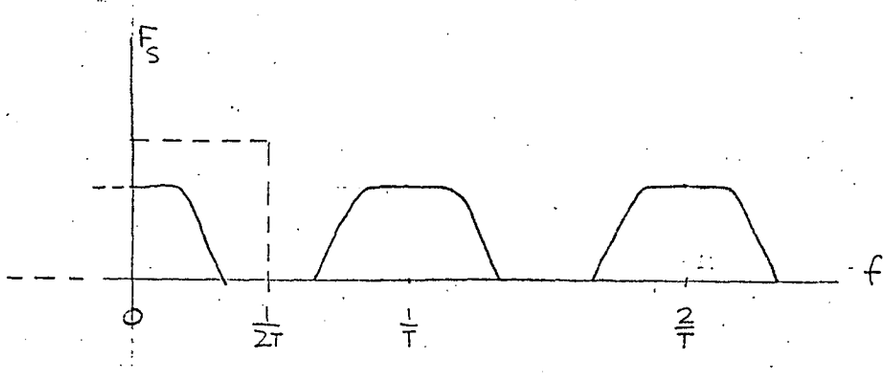


FIGURE 1-2

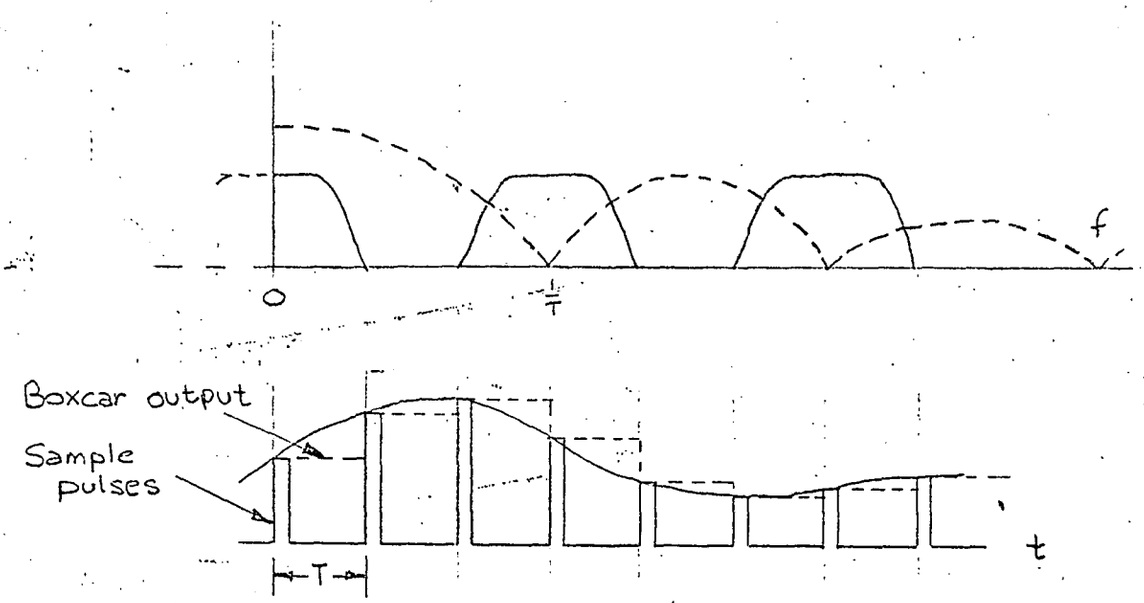


FIGURE 1-3

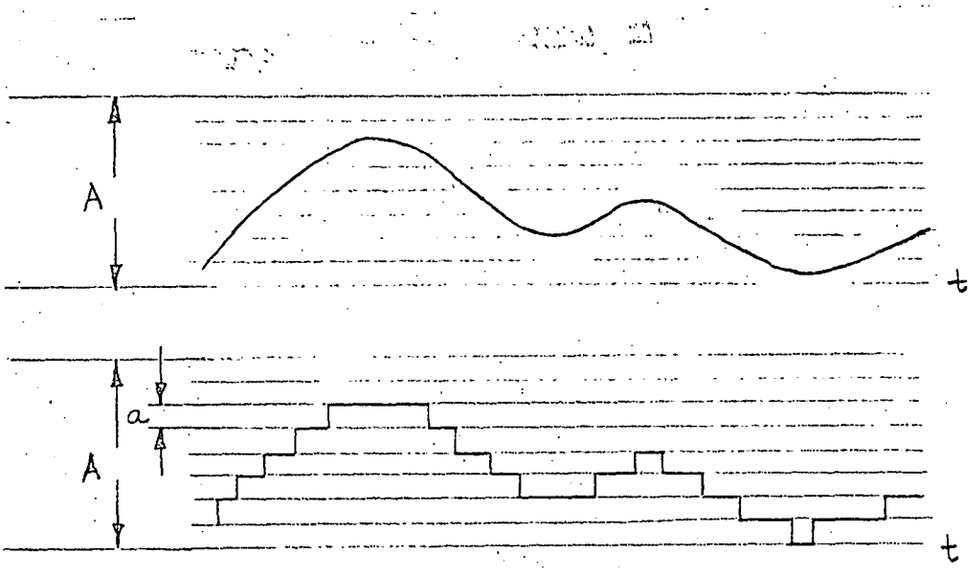
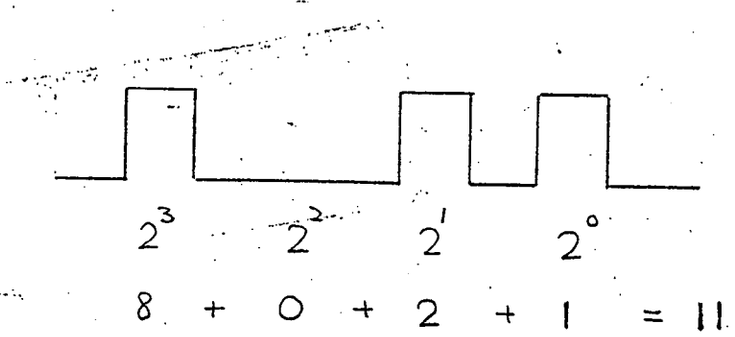


FIGURE 1-4

Binary	Decimal
0 0 0	0
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	4
1 0 1	5
1 1 0	6
1 1 1	7

FIGURE 1-5



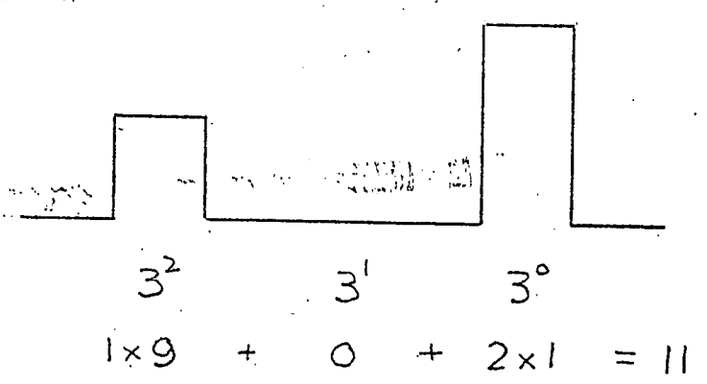


FIGURE 1-6

S	n	$\frac{S}{N}$ (db)
2	1	17
4	2	23
8	3	29
16	4	35
32	5	41
64	6	47
128	7	53
256	8	59

FIGURE 1-7

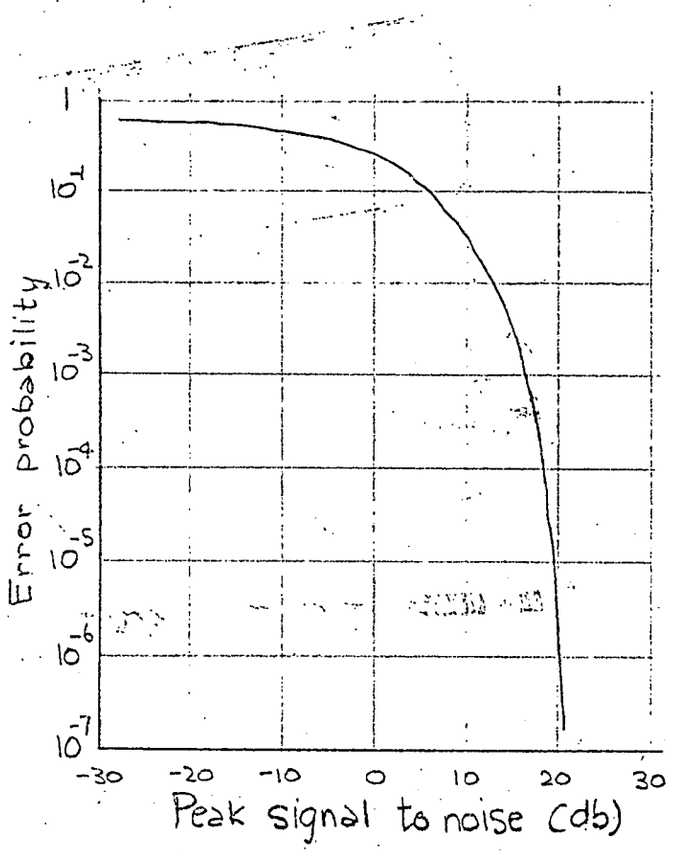


FIGURE 1-8

2. PRODUCTION AND DEMODULATION OF PCM

The production of a PCM signal must involve the processes, discussed in Section 1, of filtering, sampling, quantitization and coding. The code must then cause the generation of appropriate pulse patterns with which a synchronizing signal must be grouped. In the demodulation of the received PCM signal, which will be assumed to require pulse regeneration, the code pulses must be sampled synchronously, decoded and filtered.

This Section is concerned with the general requirements of the processes of coding, synchronization and regeneration. Coding and decoding techniques which have some relevance to the production of PCM will be considered. The type of information to which must accompany the code to permit synchronization, and its separation and use at the demodulator are discussed. The requirements of a pulse-regenerator for restoring the amplitude and timing of code pulses are also investigated.

2.1 Coding Methods

The coding of a signal essentially involves its conversion from analogue to digital form, and decoding is the reverse operation. In the process of coding the signal will be automatically quantitized if the digital form admits less possible values of the signal than the analogue form has, so that a separate quantitizing operation may not be necessary.

Many types of coders have been devised for instrumentation purposes, usually to measure displacement or rotation of a mechanical member. Attention will be restricted here to methods which are capable of high-speed and high-accuracy conversion of an electrical signal to digital form.

2.1.1 The Coding Tube

The original PCM coder[4] was a cathode-ray tube containing horizontal and vertical deflection plates and an anode mask with gaps corresponding to the binary code, as sketched in Figure 2.1. Horizontal deflection was a linear ramp which scanned the mask in the time required to produce a pulse group, and vertical deflection was proportional to the analogue input signal. The electron beam produced a series of anode current

pulses whose pattern was dependent on the input, and therefore, with a suitably shaped mask, binary coding was obtained.

This method is capable of very high-speed operation due to the low inertia of the electron beam, but its accuracy and reliability are limited by the non-linearity of the deflection system, the finite diameter of the beam, and the mask shape errors.

A variant of this method uses an external mask and senses the code with an array of photoelectric cells. The horizontal beam deflection may be replaced by a sheet beam the code being scanned if necessary at the output of the photoelectric cells. With this type of coder, any code may be obtained by the use of an appropriately-cut mask.

2.1.2 The Pulse-Counter

A coder developed from pulse-width modulators employs a time measurement to replace the spacial deflection used in the coder tube. The method is outlined in Figure 2.2. A linear ramp voltage is started at the instant of gating pulses from a stable oscillator into a counter, and the pulses are cut off when the ramp voltage reaches equality with the input signal, as determined by a comparison circuit. The counter then contains a digital number proportional to the time taken for the ramp voltage to reach the input value and therefore proportional to the input signal at the instant of equality.

This method requires not only a linear ramp, but a stable oscillator, and if it is to operate at high speeds it needs a very high frequency oscillator. It also has a disadvantage as a PCM coder that it gives the value of the input at a variable time after the initiation of the coding process, and the code is not available until then.

2.1.3 Feedback Coders

Both the coding-tube and pulse-counter methods may be made more accurate by the use of feedback. If the output code is decoded to give an analogue measure of the output, this may

be compared with the input and caused to stop some scanning process when a null is reached. For example, the coding tube may be provided with a vertical scan which is made to halt by a signal from a nulldetector monitoring the input and the feedback voltages. Thisis sketched in Figure 2.3.

The pulse-counter, when provided with feedback as shown in Figure 2.4 becomes the tracking coder invented by Barney(31). The input and feedback voltages are compared and cause the counter to scan up or down until a null is reached. This device continuously tracks the input signal and the code is always available inthe counter, except during transient excursions of the input voltage, at which times the oscillator can provide only a limited rate of change of the count.

Because of this, sampling of the input for scan purposes is best made after the coding, and can be done by transferring the counter reading quickly into separate storage at every sampling instant. The transfer must be rapid because the count may change during transfer, if not due to an input change then due to the dithering of the comparator resulting from the quantitization error.

Another result of the tracking characteristic is that the oscillator frequency must be high enough to change the counter reading by full-scale between two samples, for the input may change by this amount and this quickly if the minimum sampling rate is used. The minimum oscillator frequency needed for tracking a signal of bandwidth f c/s to an accuracy of n binary digits is (2^n-1). 2f pulses per second, so that high-accuracy operation at high speed may be limited by the counting circuits.

In both these feedback coders the accuracy is determined primarily by the decoder. Types of decoder suitable for these coders willbe discussed

in Section 2.1.4.

2.1.4 The Weighing Coder

A type of coder which has no open-loop equivalent speeds up the coding process by providing a set of reference voltages for comparison with the input. Its operation corresponds to the method used in weighing on abeam-balance when a set of graded weights is available, and this gives rise to the name. This coder has a set of binary weighted voltages (each half its predecessor), ameans of summing these accurately in any combination, and a means of comparing the sum with the input voltage; this is shown in Figure 2.5. If the number of such voltages provided is n, any input voltage (with appropriate scaling) can be quantitized to 2^n levels, and can be equalled by use of some combination of the n voltages after at most n attempts. For example, if the smallest weighted voltage is one volt and four voltages are available in all, any voltage from zero to 15 may be made up from combinations of 8, 4, 2 and 1 volts. Thus eleven volts is equalled by 8+2+1 volts, or, written in serial binary notation (Section 1.4)

$$1\,0\,1\,1 = 1.2^3 + 0.2^2 + 1.2^1 + 1.2^0$$
$$= 8 + 0 + 2 + 1$$
$$= 11.$$

In general, the input may be represented as the sum

$$e_{in} = kE\left[a_n 2^n + a_{n-1} 2^{n-1} + \ldots + a_1 2^1 + a_0 2^0\right] \quad \ldots 1)$$

where K is a scale factor dependent onthe magnitude of the least weighted voltage, and the a_i are the binary digits (0 or 1) which are to be found by the coding process.

It is possible to complete the "weighing" against n binary-weighted voltages in n operations by a trial-and-error routine. Each of the voltages, starting with only the largest, is added in turn to make a

voltage which is compared with the input, any excess being reported by a comparator. After each comparison the voltage just added is left in if the resulting sum is less than the input, but it is removed otherwise. The next smaller voltage is then added to the sum for trial. Only n weighings are needed because after the least voltage has been tried the input and the sum differ by less than this amount. If the inclusion of a particular weighted voltage inthe sum is indicated by an output pulse, and a rejection by no output pulse, the complete output represents the a_i in equation 1) and therefore is the binary coding of the input.

Other weighing routines are possible, such as the addition to the input of the next smallest voltage instead of the removal of the previous voltage after an excess sum is encountered. Another method uses only one reference voltage equal to half the full-scale input and multiplies the difference between this and the input by exactly two at each weighing if the difference is positive, but by one if the difference is negative: every positive difference corresponds to a binary code digit, and every negative difference to digit. These techniques differ only inthe practical method of achieving the same result. The latter coder, for example, requires one amplifier with an accurate positive gainfor each digit inthe code, and this is costlier to provide than a set of voltages scaled down successively.

The weighing coder is a closed-loop device, feedback coming from the progressive generation and comparison of an analogue voltage. In fact the means of obtaining the feedback voltage immediately provides a means of making a decoder: for a code digit of any weight a voltage is generated proportional to that weight, and all contributions to the code are summed.

This is shown in Figure 2.6. Thus the weighing coder and a simple decoder are very similar.

Another practical advantage of the weighing coder for PCM applications is that the code is available in serial binary positional notation (most significant digit first) while the coding is proceeding, and the coding starts at the time of making the first weighing. Therefore the transmission of the code can take place during the coding operationinstead of needing to be delayed as is the case for other types of coder. Consequently, slower conversion is possible and a slower code pulse rate may be used for the same rate of sending code groups.

The accuracy of the weighing coder is dependent on the accuracy of weighted voltages and of their summing, and the decoder has the same limitations. The only speed restriction could come from the switching and summing of the voltages, but this is offset by the slower conversion rate possible with progressive code generation. No rate-limiting effect is experienced because the coder does not have to track the input, but the input sample must be retained throughout the coding period.

Consideration must be given to the problems of providing the accurate weighted voltages and a means of summing them in any combination. Two techniques using passive components will be assessed.

2.1.4.1 Ladder Network

In the resistive ladder network shown in Figure 2.7 each interior shunt resistor has twice the value of the series and terminating resistors, and all the ideal current sources which may be switched to the nodes are equal. This choice of resistance ratios gives the network the property that the output voltage e_o measured across the terminating resistor by any current source i_j is equal to 2^j times the

voltage caused by i_o. Furthermore, by superposition, the output voltage caused by any number of the current sources is equal to the sum of the output voltages due to those sources acting individually, and is a binary function of the state of the current source switches.

The arrangement of resistances is such that the load on every interior node ($j = 1, \ldots, n-1$) is 2R looking to the left, to the right, or down. The load on every interior node is therefore $\frac{2}{3}R$. The load on the exterior nodes ($j = 0, n$) is also $\frac{2}{3}R$. Then each source j sets up a voltage of $E_j = \frac{2}{3}RI$ between the node j and earth, where I is the magnitude of each of the current sources. Because of the resistance values, a voltage E_j at node j is attenuated by $\frac{1}{2}$ at node $j+1$, $\frac{1}{4}$ at node $j+2$, etc. Hence

$$e_o = \frac{E_o}{2^n} + \frac{E_1}{2^{n-1}} + \ldots + \frac{E_n}{2^o}.$$

But $E_j = i_j \times \frac{2}{3}R$, where $i_j = 0$ or 1 depending on the state of the switch S_j.

Let the switches be set up to the coded value of the number p, represented by

$$p = a_n 2^n + a_{n-1} 2^{n-1} + \ldots + a_o 2^o.$$

Then
$$e_o = \frac{2}{3}RI \left\{ \frac{a_o}{2^n} + \frac{a_1}{2^{n-1}} + \ldots + \frac{a_o}{2^o} \right\}$$

$$= \frac{2}{3}RI \times \frac{1}{2^n} (a_o 2^o + a_1 2^1 + \ldots + a_n 2^n)$$

$$= \frac{2}{3}RI \times \frac{1}{2^n} \times p.$$

Thus the output voltage is a linear function of the coded number, provided that the network is ideal.

This network has several advantages in a practical weighted voltage generator. Good current sources can be made and matched, and the switch characteristics need not be perfect: when open they must appear as high resistances to earth,

and when closed they can be non-critical resistances in series with current sources. The network resistors have only two values, which also simplifies the problem of selection.

2.1.4.2 Weighted Resistor Network

A scheme using two voltage sources and a set of weighted resistors is shown in Figure 2.8. The currents are summed in the load resistor R_c after selection of the voltage source has been made with the change-over switches. Let the subscripts i, j denote those resistors connected to E_o, E_1 respectively.

By superposition, the output voltage $e = e_o + e_1$, where e_o, e_1 are the outputs due to E_o, E_1 respectively, with E_1, E_o respectively short-circuited. With E_1 short-circuited, all the resistors r_j and R_c are in parallel, and together are in series with all r_i taken in parallel.

Put $$\frac{1}{\sum \frac{1}{r_i}} = A;$$

$$\frac{1}{\frac{1}{R_c} + \sum \frac{1}{r_j}} = B.$$

Then $$e_o = E_o \times \{B/(A + B)\}$$

$$= E_o \times \frac{1 \Big/ \left\{ \frac{1}{R_c} + \sum \frac{1}{r_j} \right\}}{\left\{ \frac{1}{R_c} + \sum \frac{1}{r_j} + \sum \frac{1}{r_i} \right\} \Big/ \left\{ \sum \frac{1}{r_i} \times \left(\frac{1}{R_c} + \sum \frac{1}{r_j} \right) \right\}}$$

$$= \left(E_o \times \sum \frac{1}{r_i}\right) / \left(\frac{1}{R_c} + \sum \frac{1}{r_i} + \sum \frac{1}{r_j}\right)$$

$$= \left(E_o \times \sum \frac{1}{r_i}\right) / \left(\frac{1}{R_o} + \hat{\sum_o} \frac{1}{r_k}\right).$$

Similarly, $$e_1 = \left(E_1 \times \sum \frac{1}{r_j}\right) / \left(\frac{1}{R_o} + \hat{\sum_o} \frac{1}{r_k}\right).$$

Therefore, $$e = e_o + e_1$$

$$= \left(E_o \times \sum \frac{1}{r_i} + E_1 \times \sum \frac{1}{r_j}\right) / \left(\frac{1}{R_c} + \hat{\sum_o} \frac{1}{r_k}\right).$$

Now for binary coding, $r_k = \frac{R}{2^k}$,

therefore, $$\hat{\sum_o^n} \frac{1}{r_k} = \frac{1}{R}\left(2^0 \, 1 \, 2^1 + \ldots + 2^n\right)$$

$$= \frac{2^{n+1} - 1}{R},$$

and also $\sum \frac{1}{r_j} = \sum \frac{2^j}{R} = \frac{1}{R} \sum 2^j = \frac{1}{R} \times p$,

where p is the value of the coded number (always $p < 2^{n+1}$),

and $\sum 2^i + \sum 2^j = \sum_0^n 2^k = 2^{n+1} - 1$,

therefore $\sum 2^i = 2^{n+1} - 1 - \sum 2^j = 2^{n+1} - 1 - p$,

therefore $\sum \frac{1}{r_i} = \frac{1}{R} \sum 2^i = \frac{1}{R} (2^{n+1} - 1 - p)$.

Substituting these three results,

$$e = \frac{\left(\frac{E_o}{R}(2^{n+1} - 1 - p) + \frac{E_1}{R} \times p\right)}{\left(\frac{1}{R_c} + \frac{2^{n+1} - 1}{R}\right)}$$

$$= \frac{\left(E_o (2^{n+1} - 1 - p) + E_1 p\right)}{\left(\frac{R}{R_c} + 2^{n+1} - 1\right)}$$

$$= \frac{\left(E_o (2^{n+1} - 1) + p(E_1 - E_o)\right)}{\left(\frac{R}{R_c} + 2^{n+1} - 1\right)} \qquad \ldots\ldots 2)$$

$$= a(b + pc),$$

which is a linear function of p, but offset from the origin. The change in output voltage per unit change in number is

$$\frac{\Delta e}{\Delta p} = (E_1 - E_o) / \left(\frac{R}{R_c} + 2^{n+1} - 1\right)$$

This is independent of p, and can be made large for a given maximum number $(2^{n+1} - 1)$ by making $E_1 - E_o$ large and $\frac{R}{R_c}$ small. If p has only one sign, E_o can at best be made zero, which makes e proportional to p, from equation 2.

Although an accurate voltage source is practicable, the switch arrangement is difficult to achieve non-mechanically because the contacts must have a very low resistance and offset voltage when closed. The normally closed contact cannot be omitted without loss of accuracy. A further difficulty lies in wide range of resistance values which can result from large values of n: high power dissipation in low resistances may affect the resistor stability, while leakage resistance may be significant when high values are used.

For these reasons this type of weighted voltage generator was rejected in favour of the ladder network.

2.1.4.3 Tolerance Analysis

Ideally the voltage generator obeys equation so that the relationship between the code supplied to the switches of the ladder network and the voltage obtained from it is a linear staircase, as suggested in Figure 2.9. Any departure from linearity can be attributed to inaccuracy of the current sources or of the network resistances, and tolerances must be placed on these to meet the linearity specification.

The staircase is generated by combinations of the weighted voltages, so that two successive steps could be made up from quite different numbers of these voltages and their values would be subject to different sets of errors in these voltages. For example, the successive code numbers 0 1 1 1 1 1 and 1 0 0 0 0 0 of a six-digit code use five sources and one source respectively, and if all the sources in the first case are low in their tolerances while the other single source is high the staircase will have a high-step discontinuity. Similarly, if the five sources are high in their tolerances and the single source is low the discontinuity will be a shallow step.

The linearity can therefore be controlled by limiting the variation in step height as the number of code digits changes. A convenient measure of the nonlinearity is the fraction ε of the nominal step size q by which any step d departs from nominal.

Thus $q - d = \varepsilon q$,

or $\varepsilon = 1 - d/q$.

The worst case of a step discontinuity occurs at half full-scale for pure binary code because there the maximum change in the number of contributing sources takes place. The weighted-voltage tolerances

may therefore be found by considering the maximum permissible value of ε at this point.

In the ladder network, each weighted voltage can be in error due to errors in the current source, the node input resistance and the successive attenuation factors. The current source errors will be considered here by assuming that allthe resistors are exactly matched, and since the currents are all nominally equal they will also be given the same fractional error Δ although they may have either sign. The nominal voltage E_j developed at node j by the source I_j can be expressed in terms of the nominal step size q because all the E_j are equal, and the largest weighted voltage E_n is equal to half the input voltage range. Thus $E_j = E_n = 2^{n-1}q$. The contribution of E_j at the output, after attenuation by the network, is therefore $E_j/2^{n-j} = 2^{j-1}\,q$, or, including the error, $2^{j-1}\,q\,(1 \pm \Delta)$.

Now consider the worst high-step discontinuity when all the sources I_1 to I_{n-1} are on the lower limits of their tolerance and I_n is on its higher limit. (This is sketched in Figure (2.XO)). Then the total output at half full scale is

$$\sum_{j=1}^{n-1} 2^{j-1}\,q\,(1-\Delta)$$

$$= (2^{n-1} - 1)(1-\Delta)q,$$

and the output after one extra digit is

$$2^{n-1}\,q\,(1+\Delta).$$

therefore $$d = (2^{n-1} - 1)(1-\Delta)q - 2^{n-1}\,(1+\Delta)q$$

$$= (1 + (2^n - 1)\,\Delta)q.$$

Now $$d/q = 1 - \varepsilon$$

so that $$\Delta = -\varepsilon/(2^n - 1).$$

Similarly, if the same step is shallow, as in Figure 2.11, $\mathcal{E}$ is positive, and again

$$\Delta = \mathcal{E}/(2^n-1) \qquad \ldots 3)$$

This case is significant, for if $\mathcal{E} > 1$ the staircase is no longer a monotonic function of the code, as sketched in Figure 2.12 and the ambiguity in voltage makes coding impossible.

The maximum value which $|\mathcal{E}|$ may be allowed to take is $\frac{1}{2}$, corresponding to a half-sized step. This figure is chosen because subsequent decoding with a weighted-voltage generator having the same tolerance will still reproduce the input signal to within the nominal quantitizing limits of the coder.

Substitution of $\mathcal{E} = \frac{1}{2}$ in equation 3) gives the maximum fractional error tolerable in the current sources as $\Delta = \pm 1/2(2^n-1)$.

2.2 Synchronization

To demodulate a pulse-code it is necessary not only to be able to identify individual pulses but also to ensure that an account is kept of the significance to be given to each pulse. For this reason the code groups are transmitted in frames whose start and finish are identifiable, and in which the positions that pulses may occupy are pre-arranged in a pattern of code-weights.

The start of each frame and the timing within it can be communicated on a separate channel, but in small systems this is wasteful because this information can be included with the data. A frame can be identified by asignal which cannot be a pattern of data pulses, and the most obvious signal is a special group of pulses in every frame. This, of course, wastes channel bandwidth by requiring transmission of more pulses for the same data rate. A more subtle method which minimizes this wastage makes use of the fact that the data cannot change as quickly as half the sampling rate (see Section 1.3) and so uses a signal at this rate, made up most simply of a pulse in a fixed position in every alternate frame, and no pulse in this position in the other frames. In either case the frame signal may be separated with a filter.

Conventional PCM systems transmit the code pulses in each frame in return-to-zero form, and need to identify the pulse-rate as well as the frame-rate. A synchronization method has been devised which requires knowledge of only the frame-rate. Hence, it would be possible to use the non-return-to-zero (NRZ) form and save on bandwidth, as suggested in Figure 2.13 However, because in NRZ there is little energy present at the pulse-rate (on the average), this could complicate the process of pulse-regeneration (Section 2.3) which is essential on noisy transmission links.

2.2.1 Flywheel synch.

Ideally, a synch pulse need be transmitted only as often as it is needed to prevent the receiver timing from drifting so far that the pulse code-weight is lost. This means that quite long codes or groups of codes could be sent in each frame, making time-division multiplex attractive. However, such a method would require tolerances on the initial frequency and the rate of drift of the individual receiver, and ignores the possibility that a synch pulse might be lost, or one falsely inserted, by noise inthe transmission system.

In practice it is desirable to transmit as many synch pulses as the data and channel bandwidths will allow, and also to make the receiver as immune as possible to the effects of missing or spurious synch pulses. This is achieved by a method expressively called "flywheel synch" whose name is derived from the large energy reservoir fed by synch pulses, which controls the frequency of the timing oscillator in the receiver. It is shown in block form in Figure 2.14.

The flywheel oscillator can be pulled into synchronism from an initially incorrect frequency, and, once locked, can withstand relative frequency drifts to an extent dependent upon the rate at which the energy reservoir can react to change and the gain of the loop. The greater the amount of energy that is extracted from

the synch pulse, the more rapidly will synchronism be attained and the more tightly will it be held, but the more sensitive will the system be to noise.

The detector in Figure 2-14A is a form of correlation circuit which performs continuous comparison of the controlled and controlling signals, and produces an output which is an odd function of the phase difference. The flywheel is a lowpass filter to average the detector output, and it must have zero bandwidth if the correlation averaging time is to be infinite. However, the product of two functions of different fundamental frequencies contains a component having the difference frequency, which cannot be passed by a zero-bandwidth filter. If the receiver oscillator is to possess a pull-in range of frequencies the filter bandwidth must therefore be opened to allow the expected frequency difference. It also follows that as the pull-in range is extended by shortening the averaging-time, the phase control suffers; but it is the phase-sensitivity, or change in frequency per unit change in phase, which determines the hold-in range, since the two detector inputs then have the same frequency. Some compromises are therefore necessary for satisfactory performance, and these must be governed by the particular application. The flywheel filter usually contains both lag and lag-lead sections, and it may even employ a switch to change the filter characteristics when synchronism has been achieved, so that the conditions for minimum synchronization time and minimum noise bandwidth can be made independent.

2.2.2 Code-pulse detection

The oscillator inthe receiver must provide the timing needed for sampling the received code when a pulse is due. Information is therefore required about the pulse frequency and phase within the frame. If all frames have the same known internal timing arrangement, this information may be obtained by synchronizing the oscillator to a frequency suitably higher than the frame rate, counting its output, and then gating these signals to obtain time-slot pulses. One of these, at frame rate, may become the strobe pulse used to operate the synch system, and it must maintain the correct phasing between the received frame and the receiver frame timing. The other time-slot pulses may then be used to strobe the received code pulses.

Thus, provided that the receiver oscillator can be satisfactorily synchronized to a lower-frequency signal by means of a signal derived from itself by frequency-division, only frame-rate information is needed inthe synch signal. It willbe shown in Section 33.2 that this operation is possible in a flywheel system.

2.2.3 Synch Detector

A very simple synch detector, making novel use of a property of the clamp or d-c restoring circuit, has been developed for use inthe PCM equipment. Its operation is described here, and further applications are discussed in Appendix D

The basic clamp circuit shown in Figure 2.15. is for clamping the positive peak of the input waveform to earth. The capacitor C is charged rapidly through the diode to the peak amplitude of the input waveform, and since it cannot discharge when the input changes sign (except into a load resistance which is assumed high), it superimposes a negative d-c shift on the input so that the output is never positive.

The modification used in the synch detector is to clamp the input not to earth but to another voltage generator of the particular form shown in Figure 2.16. Both inputs are constant amplitude pulses, and for the purposes of explanation are of the same frequency, but the clamp bias B has a smaller mark/space ratio than the input A. Different clamping actions occur with this circuit depending on the relative timing of the input and bias.

(a) Bias zero between the input's positive and negative transition.

The action is similar to that of the simple clamp in that the capacitor is charged rapidly through the diode when the input goes positive, its right-hand plate being held at zero potential, approximately.

When A goes negative, C retains its charge and the output goes negative, and if its amplitude is less than the peak value of A, the diode remains back-biassed. The output is therefore the same as for the simple clamp, as shown in Figure 2.17(a).

If B exceeds A in amplitude, the output changes to the amplitude of B during its presence by charging C to this new value. This causes the output to appear as the input waveform clamped to a voltage which is the difference between the peak values of B and A.

(b) Bias negative between the input's positive and next negative transition.

This relative timing is shown in Figure 2.17(b) The capacitor is initially charged to the peak value of A, and is further charged through the diode when B goes negative. Since it cannot discharge when B falls to zero, the output remains at the peak value of B until A goes negative taking the output further negative by the peak value of A. Subsequently the output appears as the input waveform clamped to the peak value of the bias waveform.

(c) Bias negative during the input's positive transition.

This case is shown in Figure 2.17(c) and its analysis is similar to that of case (b), above.

(d) Bias negative during the input's negative transition.

Figure 2.17(d) shows the first two cycles, and this case also yields the same ultimate output as case (b), above.

The output therefore has two distinct mean values, the input being clamped either to zero or to the bias peak value depending on the relative times of their transitions.

If the input and bias waveforms have different fundamental frequencies, their relative phasings will slip at the difference frequency and cause the clamp to produce

an output whose mean value (per input cycle) varies at the slip frequency. The output changes abruptly (within one input cycle) as the positive-going edges of the two waveforms pass, as sketched in Figure 2.18. This phase response has the form desired of an ideal synch detector, except for the steady-state delay of t_1. In such an application, waveform B would be derived from the received synch pulse, and waveform A from the output of the receiver oscillator.

The fact that the average output per cycle is non-zero is very useful inthe frequency control of a-stable multivibrators, and since the actual amplitude can be made as large as is desired in the clamp circuit, the need for amplification is eliminated.

It can be seen from Figure 2.18 that the widths of the negative parts of the two waveforms are unimportant in the action of the clamp circuit, as long as $t_2 < t_1$, but they do govern the fraction $\frac{t_1 - t_2}{t_3}$ of the slip cycle during which the clamp output is low. If this ratio can be made nearer to 0.5 the requirements of the flywheel filter are eased because more energy is concentrated at the slip frequency.

2.3 Regeneration

Two of the most important features of PCM transmission are the extent to which the signal may deteriorate while still bearing information, and the possibility of repeated regeneration of the signal without distortion. The causes of signal degeneration can be classed as predictable or unpredictable, and these are differently amenable to regeneration. Predictable distortion is that resulting from known characteristics of the transmission channel, such as limited bandwidth, while unpredictable distortion is due to the superimposition of spurious signals onto the signal.

The major cause of predictable distortion is limited channel bandwidth. High-frequency restriction results in rounded and delayed pulses (Figure 2.19(a)) which may be unsuitable for gating operations inthe decoding process unless they are regenerated. Poor low-frequency response causes droop distortion (Figure 2.19(b)),

because the transmitted signal contains a d-c component. By itself this is not serious because clamping can restore the d-c if the average pulse-height is sensibly constant. As would be expected, predictable distortion can be minimized if the extent of its effects is known in the particular application.

Noise, however, is not so readily overcome. The problem of determining the presence or absence of a particular pulse, and its effect on the received S/N ratio, is considered in Section 1.7 with the result that information is best interpreted from signals either side of a level equal to half the average pulse-height (Figure 2.20) Before level-sensing can be applied, though, the d-c component must be restored, and this is not done so successfully in the presence of noise, although it is used in television reception. The only noise-discriminating action which can be of certain help is retiming of the received signals, wherein use is made of the fact that the expected time of occurrence of each pulse is known from the demodulator.

Synch pulses as well as code pulses may be advantageously retimed, but only for repeater station regeneration; retimed synch pulses cannot be used in the synch detector because they themselves determine the timing via the flywheel oscillator. Their occurrence and length must be found by analogue methods for this purpose.

2.3.1 Regeneration Scheme

A complete pulse-regeneration scheme is given in Figure 2.21. The input filter restricts the noise bandwidth, and its characteristic should be Gaussian, although it may need to suit the transmission link. It is followed by a d-c restorer which clamps the positive signal excursions to the signal peak value averaged over several frames. This places the slicing level at zero potential for the limiting amplifier, whose other function

is to remove amplitude variations introduced along the transmission path. The signal is next to be reformed and retimed, so the synch pulse is separated at this stage by an integration method discussed in Section 3.3.2.

The pulse discriminator makes use of a bipolar integrator whose output is set to zero at the end of every time slot. The polarity of the integrator output at the instant of resetting is used as an indication of the presence or absence of a pulse, and a flipflop is set or reset accordingly. Because the polarity pulses occur one per time slot, the flipflop output is also automatically timed, and it is used as the regenerated signal by this method. The action of the system is shown by the waveforms sketched in Figure 2.22.

The integrating discriminator detects a pulse as a certain minimum amount of energy of a definite polarity averaged over one time slot. In this way it is far more effective than a sampler of the slicer polarity which could falsely sample a noise pulse. The synch separator also uses integration, which helps its operation in the presence of noise, but it cannot have the assistance of retiming. Its noise rejection is performed by the flywheel of the synch system.

Regeneration by this method results in the signal's being delayed by one time slot. The receiver is unaware of this, so if signals are compared after transmission via two paths employing different numbers of repeaters, the delay difference may be significant and may need compensation.

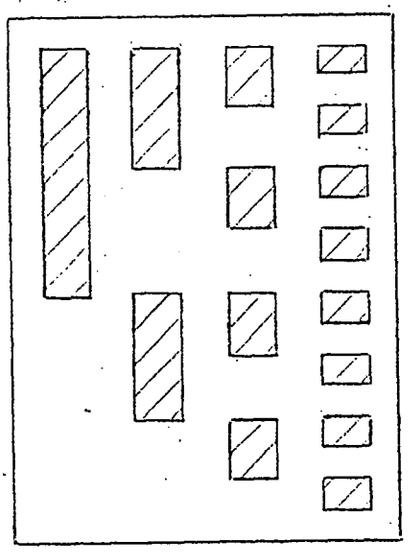


FIGURE 2-1

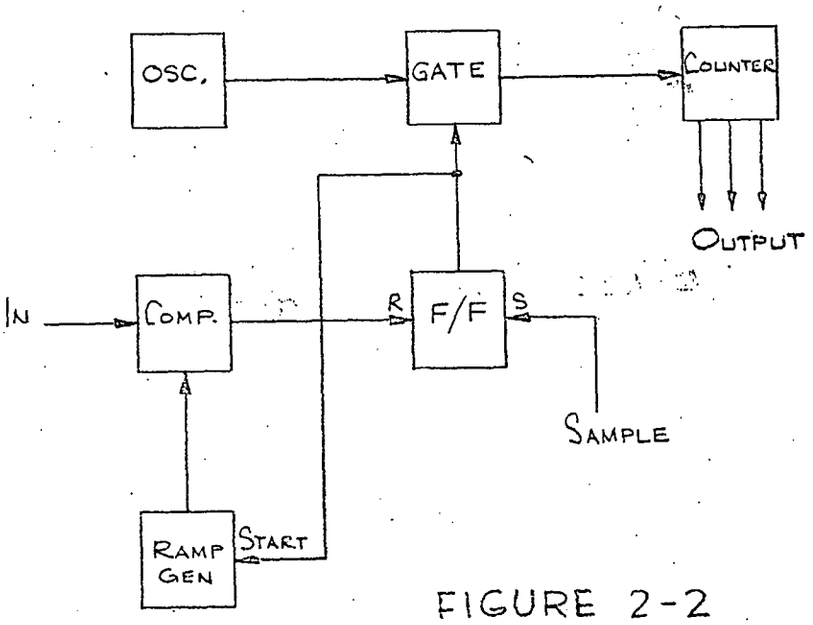


FIGURE 2-2

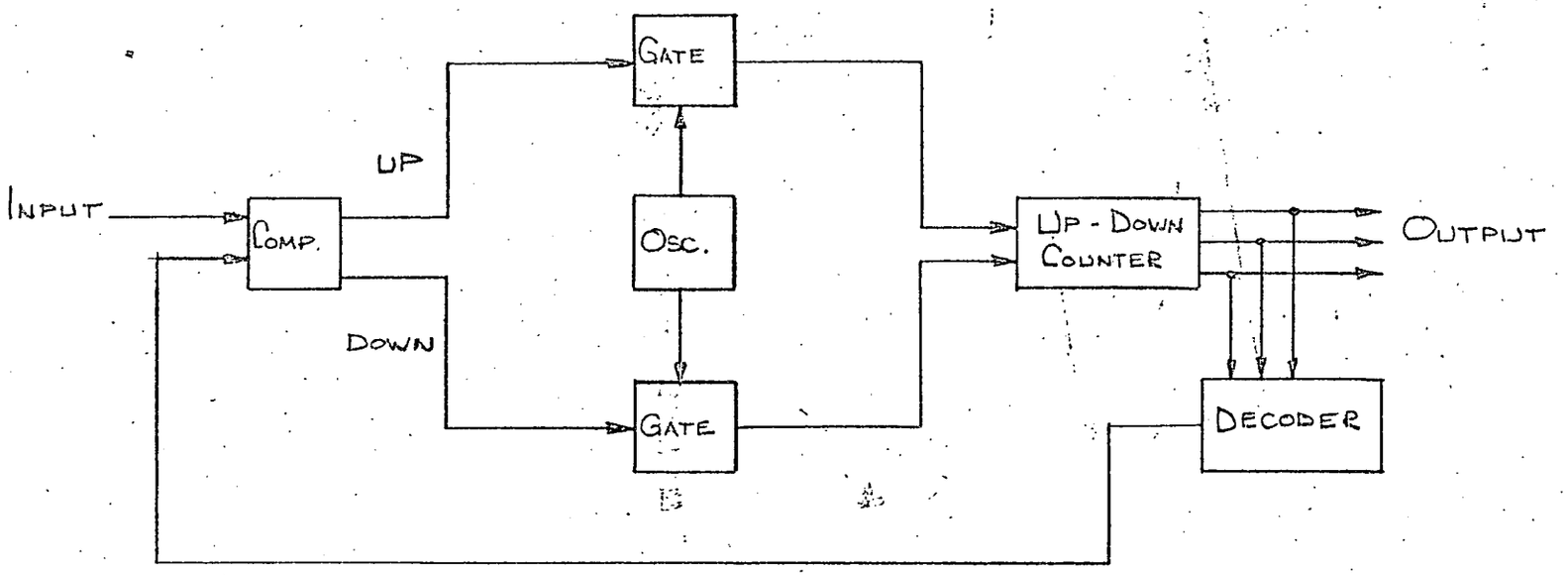

INPUT
COMP.
UP
DOWN
GATE
OSC.
GATE
UP - DOWN COUNTER
OUTPUT
DECODER

FIGURE 2-4

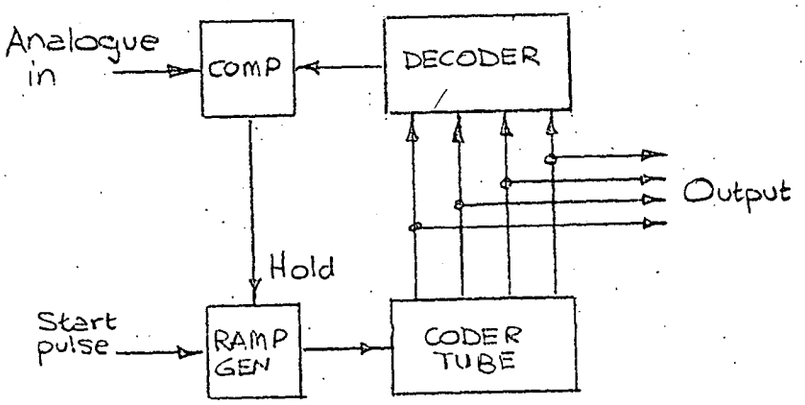
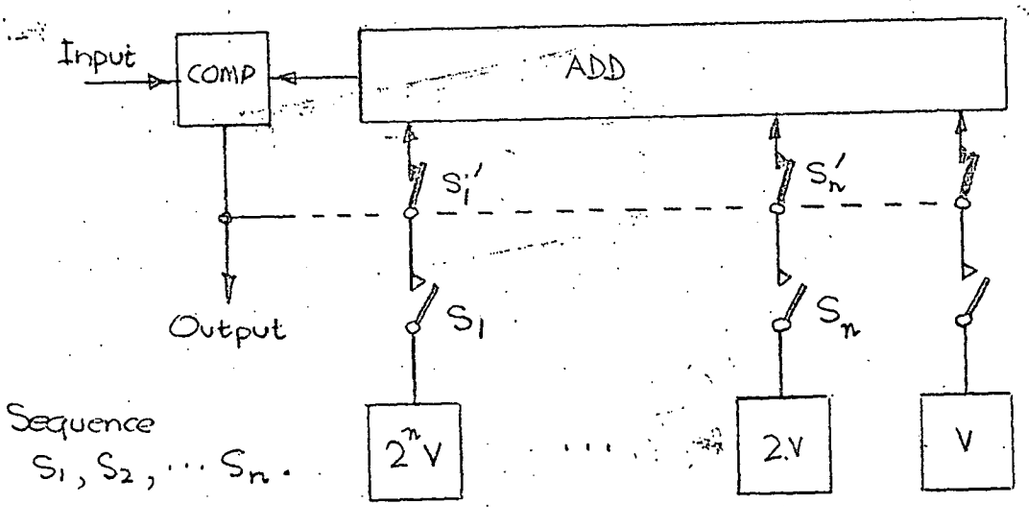


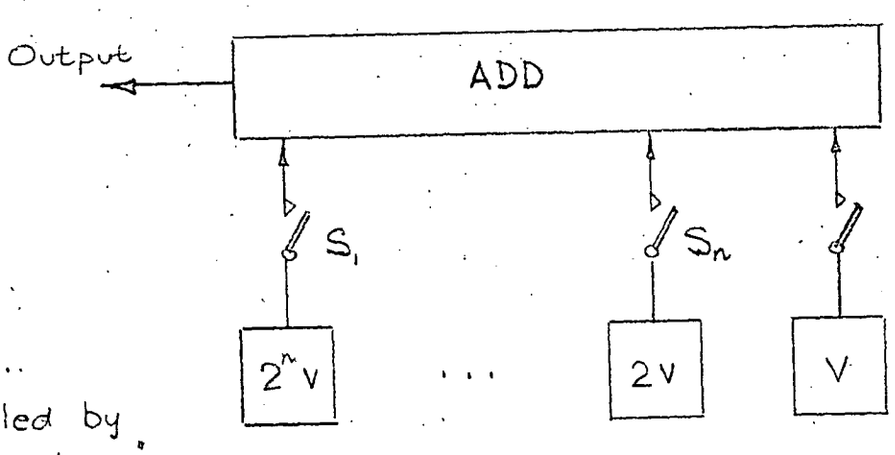
FIGURE 2-3



Sequence $S_1, S_2, \cdots S_n$.

$S_1', S_2', \cdots$ controlled by output.

FIGURE 2-5



$S_1, S_2 \cdots$ controlled by code input

FIGURE 2-6

Resistive Ladder Network

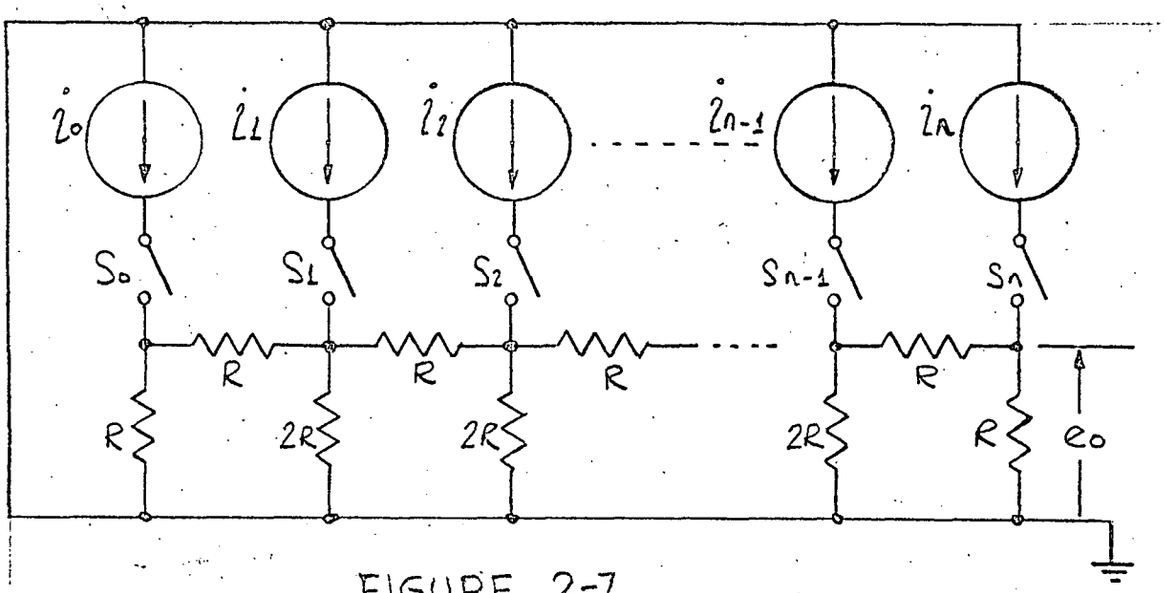


FIGURE 2-7

Weighted Resistor Network

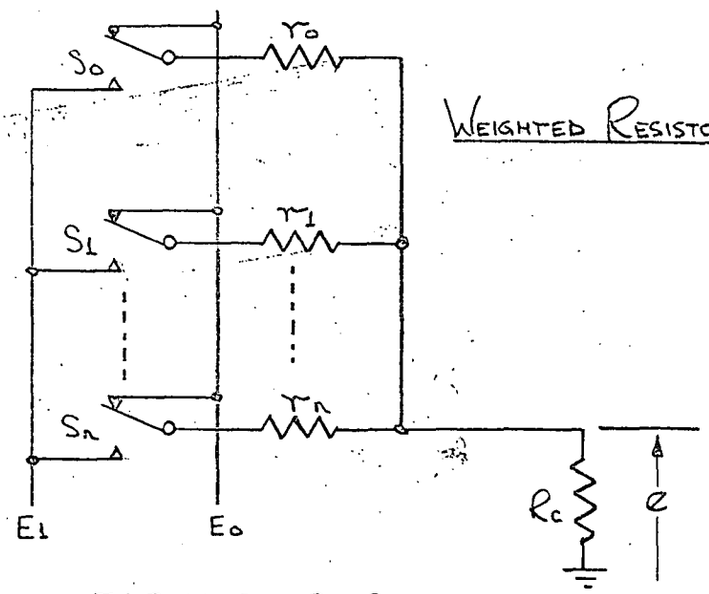


FIGURE 2-8

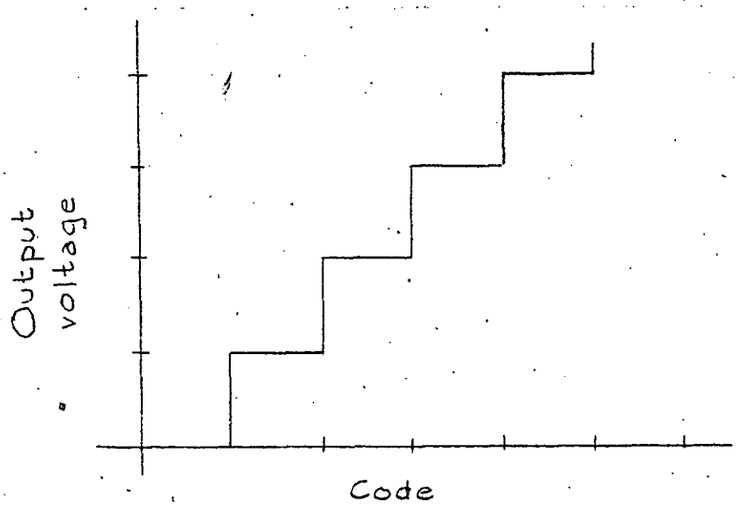


FIGURE 2-9

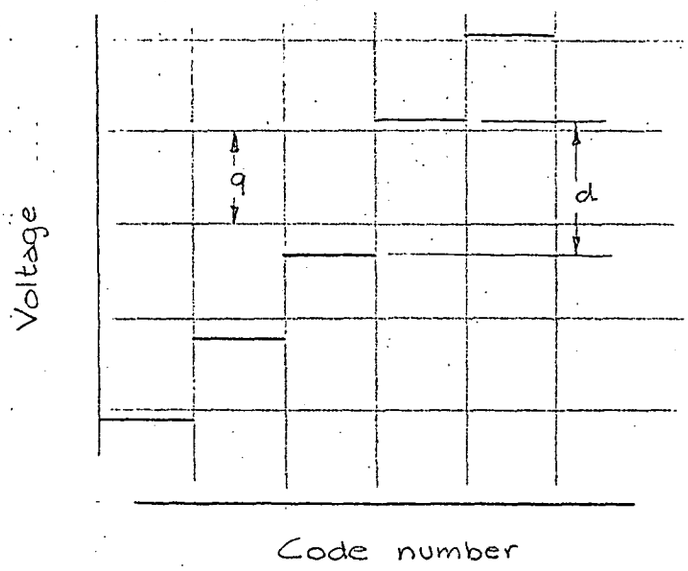


FIGURE 2-10

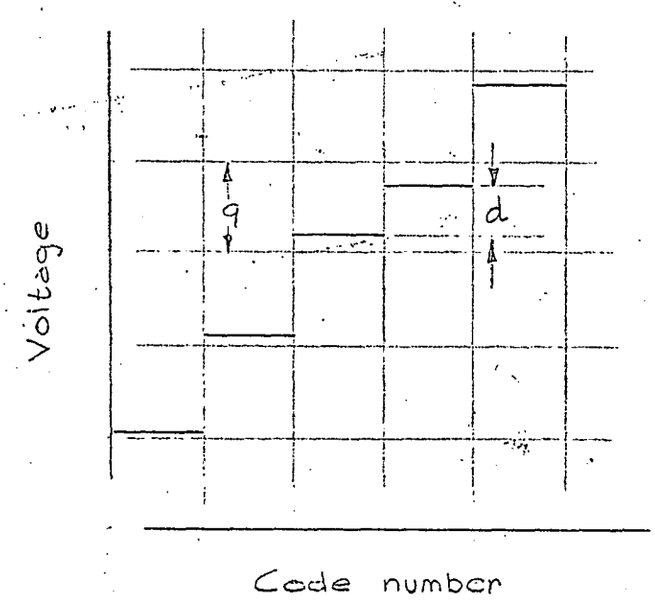


FIGURE 2-11

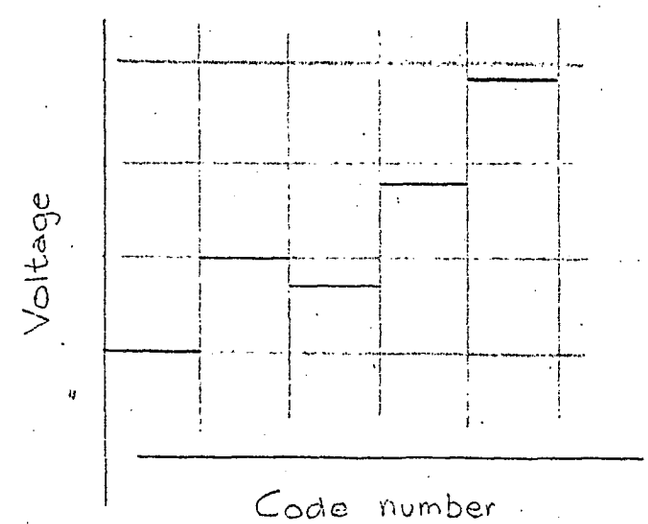


FIGURE 2-12

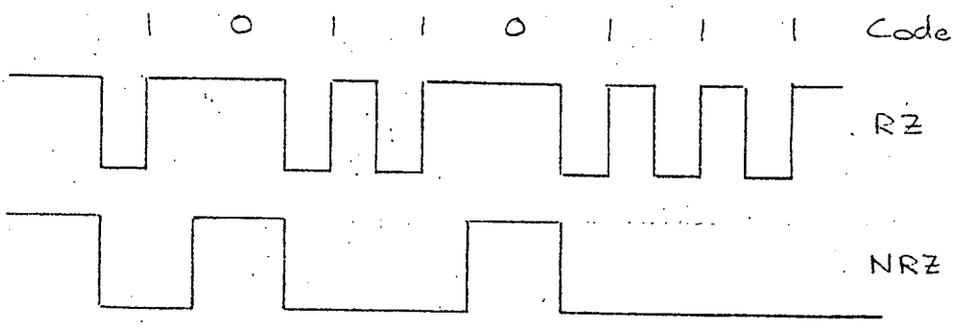


FIGURE 2-13

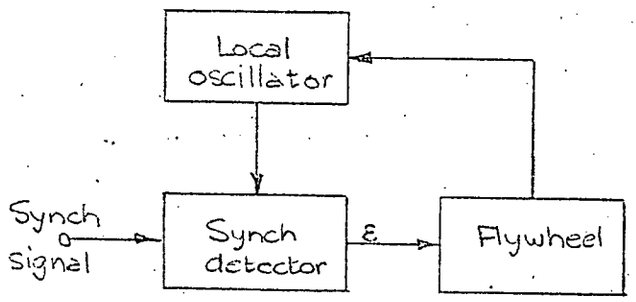


FIGURE 2-14

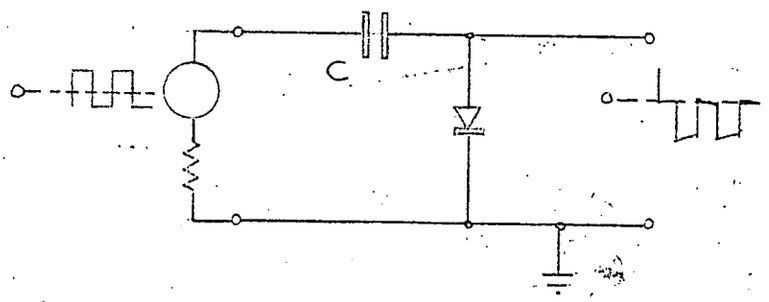


FIGURE 2-15

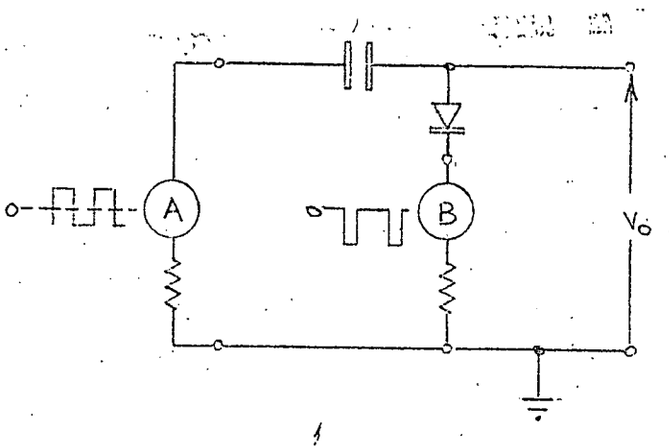


FIGURE 2-16

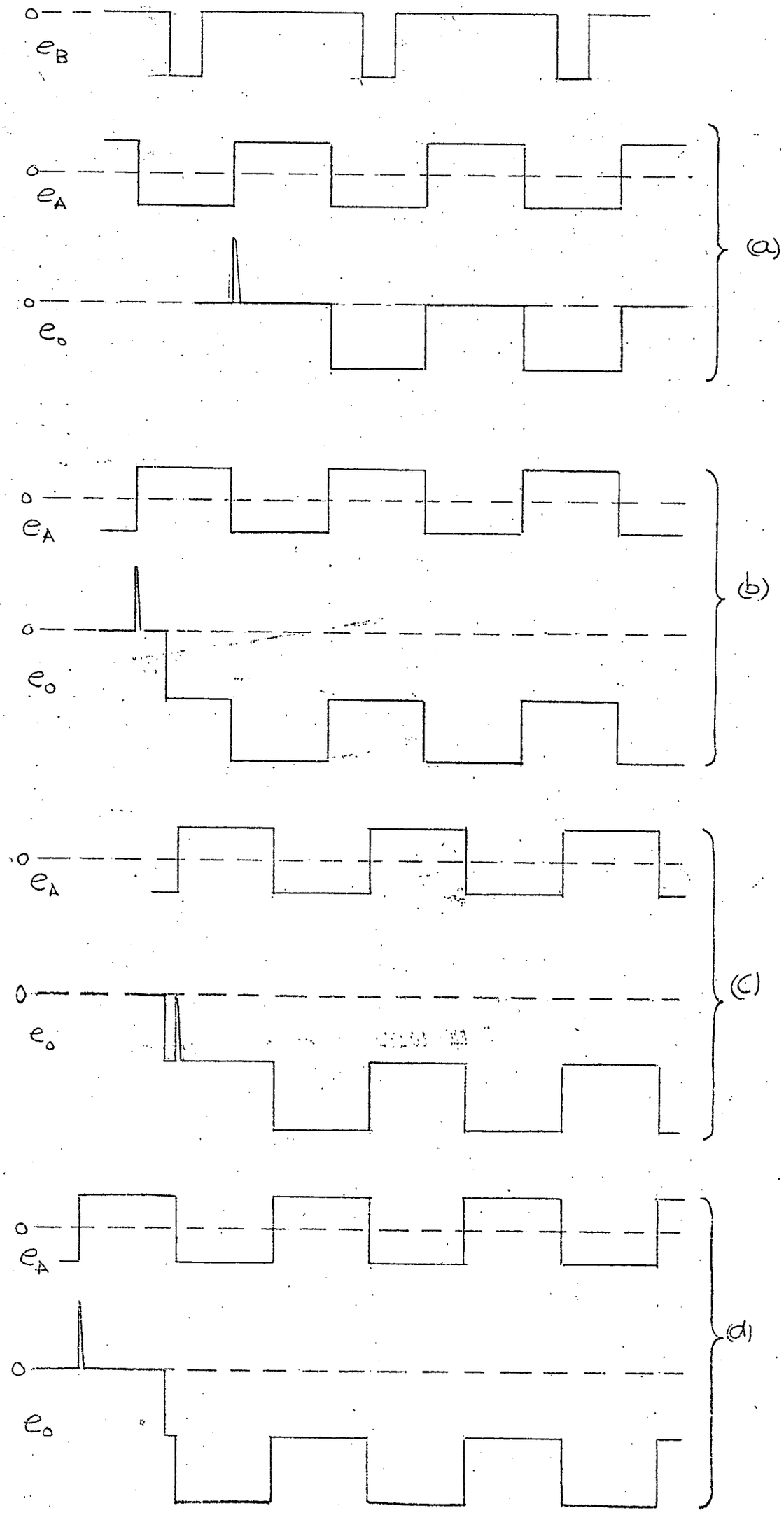


FIGURE 2-17

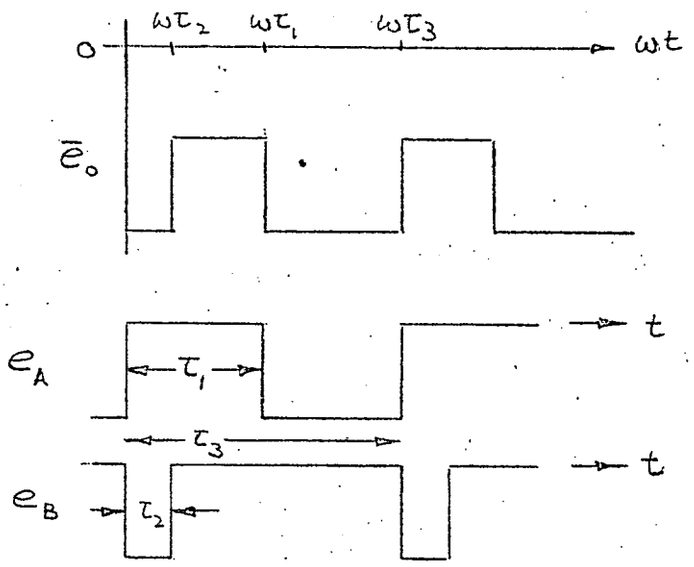


FIGURE 2-18

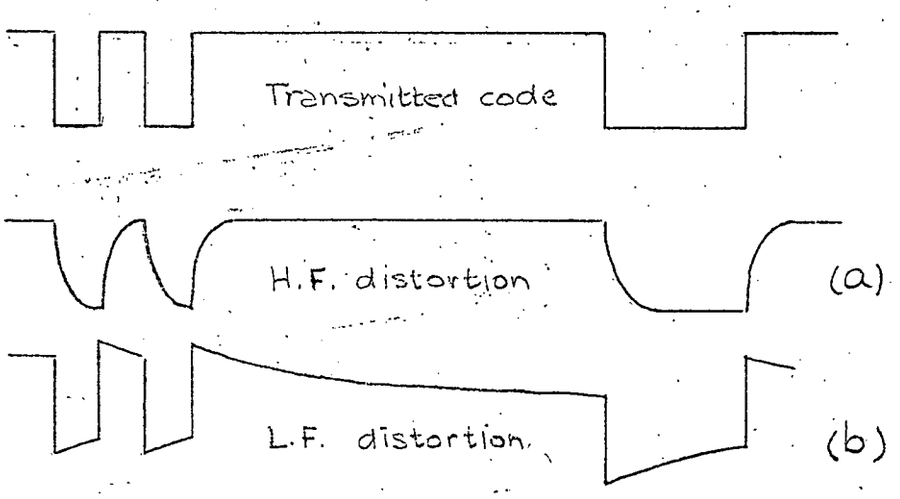


FIGURE 2-19

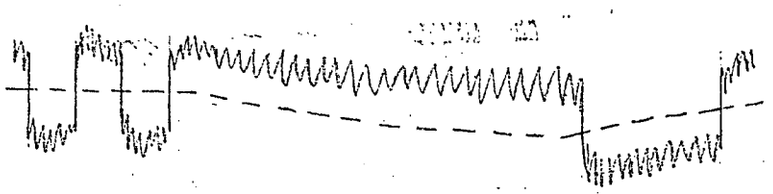


FIGURE 2-20

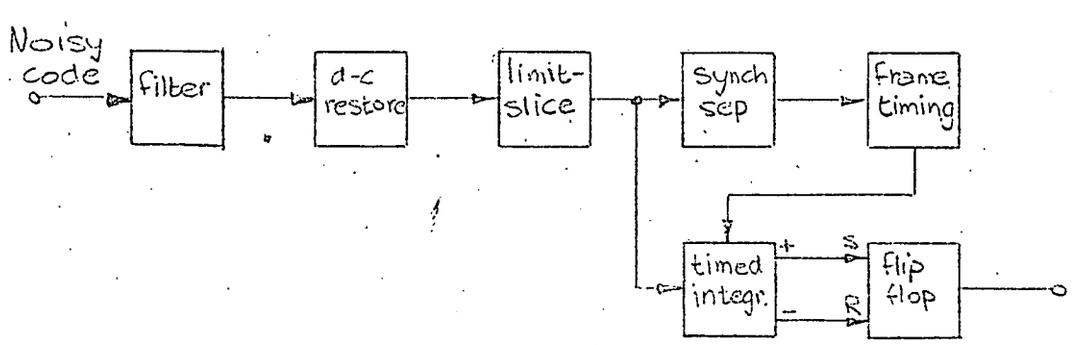


FIGURE 2-21

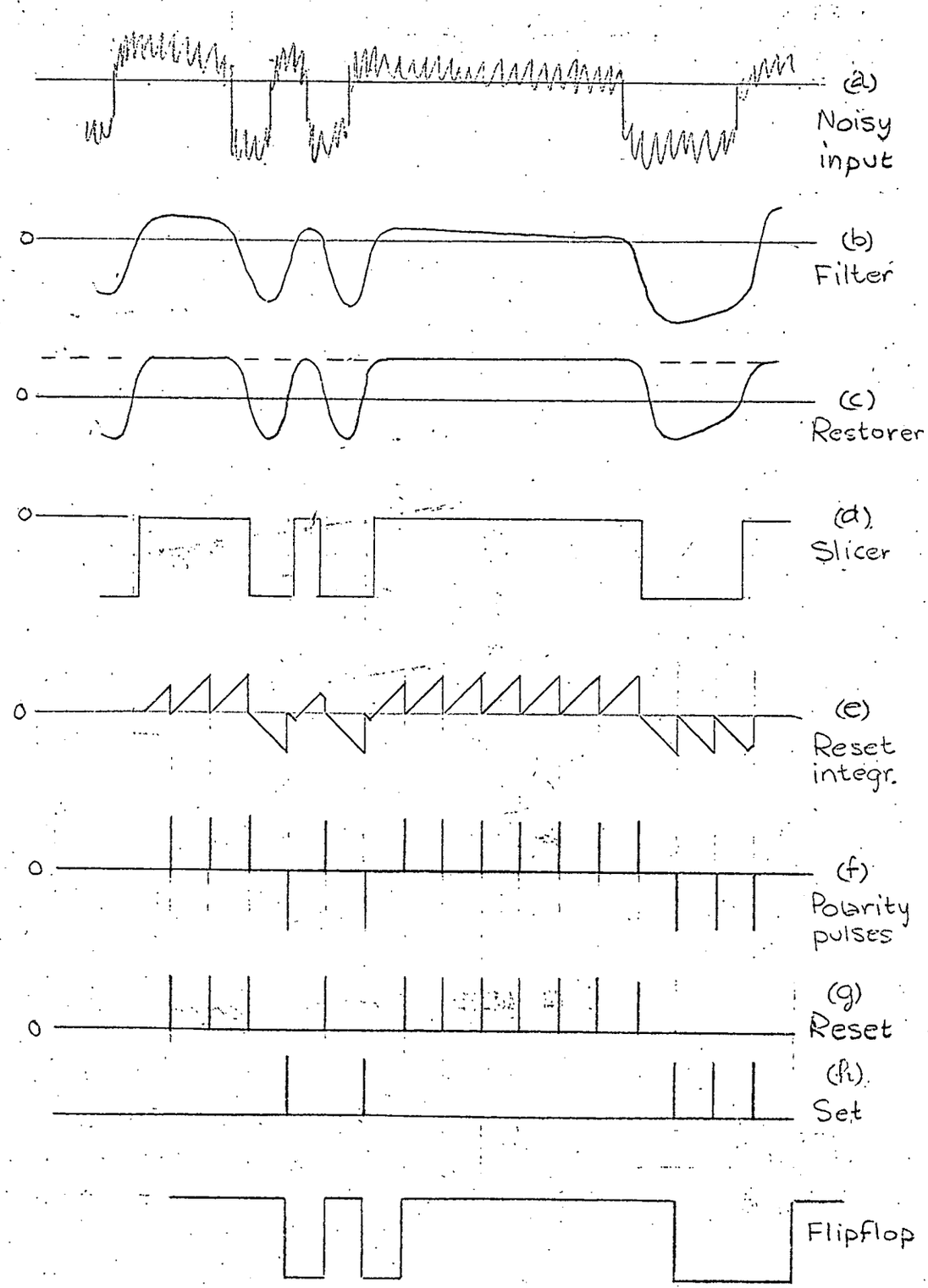

(a)
Noisy
input
(b)
Filter
(c)
Restorer
(d)
Slicer
(e)
Reset
integr.
(f)
Polarity
pulses
(g)
Reset
(h)
Set
Flipflop

FIGURE 2-22

3. PCM EQUIPMENT

3.1 General Specification

The pulse-code modulator and demodulator were designed with intended application to the telemetry of seismic signals in the frequency range 0 to 1 c/s, but this frequency was so low as to be inconvenient during the testing of the circuits, and the signal bandwidth was raised to 30 c/s.

The modulator accepts signals inthe range 0 to -5 volts and samples at a rate of 62.5 samples per second. For each sample it produces a 6 digit serial binary code and a frame synch signal, giving an output pulse rate of 1 kc/s. Coding to 6 binary digits (bits) causes a quantitization error of $\frac{1}{2} \times 2^{-6}$, or 0.8%, which is adequate for the data, and the 1 kc/s pulse rate is low enough for most transmission links likely to be used, whether line or radio. The output pulses are -12 volts for a digital 1 and 0 volts for a digital 0, and all the code pulses have the same width, but the synch pulse is three times wider. The code pulses are arranged within a frame in decreasing binary weight, as shown in the format specification, Figure 3.1. Photographs of one frame of the actual output for the codes 1 1 1 1 1 1, 0 1 1 0 0 0 and 0 0 0 0 0 0 are shown in Figure 3.2.

The demodulator accepts code which is in the proper format and has a pulse rate of approximately 1 kc/s. It incorporates a regenerator which may be used separately in repeater stations if required. Synchronization locks the demodulator oscillator to the code-pulse rate, but a coarse ($\pm$ 50%) frequency control is provided so that the oscillator can be set within the $\pm$ 25% range of the synch. system. The demodulator output is available as either a filtered or an unfiltered voltage inthe range 0 to -5 volts, and in phase with the modulator input. The unfiltered output is constant over the period of one frame but delayed by one frame relative to the input code.

External regulated power supplies are required for both units. The modulator load is 60 mA at +12 volts and 180 mA at -12 volts, and the demodulator load is 35 mA at +12 volts and 160 mA at -12 volts.

3.2 Modulator

The modulator uses a weighing coder because with this type the code is available serially as it is produced, starting at the instant of initiating the coding process. This simplifies the format of the output frame and results in the lowest code pulse rate; it also gives the coder circuits the lowest operating speed. These decisions were made so that if high-speed applications for the equipment were considered, the techniques would offer the least possible restriction.

However, the weighing coder requires that the input sample be available throughout the coding process, that is, for almost a full frame, and a means of storing the amplitude of the sample is therefore necessary. This is done with a "boxcar" circuit.

Since no coding can be done while the input is being sampled, this period is utilized for generating the synch pulse. The timing of the sampling, the successive weighings, and the production of the code and synch pulses is controlled by a set of time-slot pulses generated in each frame from a master oscillator.

3.2.1 Block Diagram

The arrangement of the modulator is given in Figure 3.3. A sampler and boxcar circuit provide one input to a high-gain differential d-c amplifier, the other input being weighted voltages with which the input is compared. Further d-c amplification converts the difference signal to a standard-height pulse, whose presence denotes that the weighted voltage sum has exceeded the input sample, or whose absence

denotes the opposite condition. In accordance with the weighing-coder method (See Section 2.1.4) the presence of a pulse requires the removal of the last weighted-voltage, and this is performed by AND gates which strobe for an output code pulse in a particular time slot, and correct the voltage generator if an output is obtained.

The desired output code contains a digit for every weighted-voltage which is needed to make up the input sample, and is obtained by producing no digit when a pulse is received from the comparator, and a digit when no pulse is received. This is done with a (logical) inverting amplifier. To obtain blanked slots between the code digits, pulses are inserted by gating into the inverter input, so that they appear as spaces in the code output.

The weighted-voltage generator is controlled by six bistable stores. If the contents of a store are set to "1", then it switches into the comparator the appropriate voltage, while if it contains a "0", no voltage is supplied. The stores are all reset to "0" at the end of every coding operation, and each is set to "1", beginning with the most significant voltage, at the start of the time slot into which it may place a code digit. The stores may also be reset by the AND gates which strobe for pulses from the comparator; then the weighted-voltage is removed as soon as the comparator shows the input has been exceeded by the sum of the weighted voltages used. The only store which is reset in such an event is the last one to have contributed a voltage, and the sum for comparison falls to its previous value so that the next smallest weighted voltage may then be added. If no reset command is received from the strobing gates, the store remains set, and that weighted-voltage is left in the sum. This digital feedback loop ensures that the sum of the voltages is always less than the input voltage, and the error is decreased after each comparison.

The timing oscillator drives a chain of 4 bistable multivibrators, and the 16 equal time slots which make up a frame are generated by combining the outputs of these dividers in a set of AND gates. One of the slots is allocated to performing the sampling operation, so that the sampling frequency is 1/16 of the oscillator frequency. Other time slot pulses are used for setting the stores successively, for strobing the comparator output, for inserting blanking and synch pulses, and for resetting the stores at the end of each coding operation.

3.2.2 Circuit Description

In the following circuit diagrams, time-slot pulses are numbered according to their positions in the frame.

3.2.2.1 Sampler and Boxcar (Figure 3.4)

The analogue input signal is accepted by an emitter follower, primarily to provide a low charging impedance for the boxcar circuit. Because its load current can flow in either direction, a complementary emitter follower is used.

The boxcar circuit consists of a storage capacitor and a transistor switch which isolates the capacitor from the input except during the sampling period. When a sampling pulse is applied tothe switch drive resistor, one of the collector-base junctions of the two switch transistors is forward biassed and that transistor conducts heavily using its collector as an emitter. In this state the collector-emitter voltage drop is less than the collector-base drop, so that the other transistor has its emitter-base junction forward biassed and it also conducts. The capacitor is then connected to the input by a very low resistance

and offset voltage, and it is charged or discharged rapidly from the emitter follower. When no sampling pulse is present the switch drive resistor is returned to earth potential and neither collector-base junction can conduct. The switch transistors are selected for high gain and low collector-base leakage.

The storage capacitor is followed by a two-stage emitter-follower which has a very low input current to prevent discharge, and this permits non-destructive use of the stored sample. These transistors are also selected for high gain and low leakage, and the capacitor is a polyester type to avoid diclectric leakage.

The results achieved with this circuit are illustrated in the photograph in Figure 3.5, which shows the droop in the boxcar output during one frame to be 25 mv, or 0.5% of full scale.

3.2.2.2 Comparator and Pulse Amplifier (Figure 3.6)

The outputs from the boxcar and the weighted voltage generator are compared by being direct-coupled to opposite inputs of a long-tail differential amplifier. The smallest difference which must be discriminated is half the least-weight contribution, that is $\frac{1}{2} \times 2^{-6} \times 5$ volts = 40 mV, and the amplifier has a differential gain of about 20 for small signals; a diode clamp limits the output excursions to prevent saturation from large signals, such as can occur during the first few weighings. Since the common-mode signal on the two inputs has a range of 5 volts, the emitter resistance for the amplifier must be compliant as well as high valued, and it is composed of a transistor operating as a constant current source.

Stabilization of the amplifier against thermal drifts is not difficult due to the generous offset voltage allowance of $\pm$ 20 mv. Gross base-emitter

voltage variation is minimized by tight thermal coupling between the two transistors, and variation in base currents, due to different coefficients of current gain, does not cause significant voltage offset because the source impedances for the amplifier are low and equal.

The output of the comparator is regeneratively amplified to a standard-height digital pulse by two Schmitt triggers isolated from the comparator by an emitter follower.

The photographs in Figures 3.7, 3.8 and 3.9 show, in order, the outputs of the comparator and the two Schmitt triggers, all for the code 0 1 1 0 0 0.

3.2.2.3 Format Blanking, Inverting Amplifier, Output Stage (Figure 3.10)

The pulse amplifier output is combined in an OR gate with the appropriate interdigit time slot pulses, and then taken via an isolating emitter follower to the coincidence (AND) gates where the code pulses are strobed. The OR gate output is also inverted by a common-emitter amplifier to form the correct pulse code and supplied to the modulator output terminal at low impedance from an emitter follower.

3.2.2.4 Coincidence Gates (Figure 3.11)

The blanking OR gate output supplies one input to each of five two-input AND gates. The other inputs are timing pulses in the first five of the six digit slots. An output is therefore obtained from any gate when the comparator has produced an output pulse in that time slot. No gate is provided for the sixth digit because no feedback action is necessary after the least-weight comparison.

The photograph in Figure 3.12 (a) shows the output of Coincidence Gate 5 when a pulse is present in the fifth digit slot of the output. Figure 3.12(b) shows the output of Gate 3 when the output code contains no pulse in the third digit slot. Both these photographs used the same CRO synch signal to show the relative timing.

3.2.2.5 Stores (Figure 3.13)

One store is provided for each of the first five code digits. They are set successively to switch the weighted voltages into the comparator, and are reset if no code digit is generated as a result of this. The sixth digit is controlled not from a store but from its time slot pulse, since no further comparison need be made after it has been chosen.

The store consists of a bistable multivibrator or flip-flop with three collector-triggering inputs. One collector is triggered by the setting time slot pulse, and from this collector the output of the store is taken to the weighted voltage switch. The other collector carries the two resetting inputs, one from the appropriate coincidence gate via a pulse-shaper, the other from the time slot pulse which is used to reset all the stores at the end of the coding operation. If a coincidence gate resets the store, the main reset pulse which follows has no effect on the state of the store.

An analysis for the design of the bistable multivibrator is given in Appendix B.

The photograph in Figure 3.14(a) shows Store 2 set by its time slot pulse, but subsequently reset by a coincidence pulse, while Figure 3.14(b) shows Store 2 set normally, but not reset until the end of coding. Figure 3.15 shows Store 3 likewise reset by the main reset pulse.

It may be noticed that if a store is provided for the sixth digit, the six stores contain the output code in parallel form just prior to their being reset. The contents of the stores may therefore be sampled at the completion of the coding if a parallel output code is needed for operation of data handling equipment.

3.2.2.6 Weighted-voltage Generator (Figures 3.16(a) and (b)

The set of voltages weighted in the ratio of the decreasing binary sequence $1 : \frac{1}{2} : \frac{1}{4}$; $\frac{1}{8} : \frac{1}{16} : \frac{1}{32}$ is obtained by driving fixed currents into a resistive network having particular attenuation properties. (See Section 2.4.4) This network, shown in Figure 3.16(b) has its resistances chosen so that every current-injection point presents the same input impedance, and so that application of equal currents at these points in succession results in an output voltage which is successively in the required ratio, while simultaneous application of equal currents at any of the inputs causes an output voltage which is the sum of the voltages produced by individual currents at these points. The values of the currents and resistances governs the network output voltage, and hence the scaling of the modulator input.

The current sources, one of which is shown in Figure 3.16a) use transistors operated in the common-base connection to obtain a high output impedance, and the NPN type is needed to develop negative weighted voltages. All the currents are made equal by driving the bases from the same temperature-compensated Zener-diode voltage source and providing equal high-stability emitter resistors.

This assumes that the differences in base-emitter voltages are sufficiently small compared with the Zener-diode voltage - a fact found to be true for the few 2T65 transistors available. The operating current is set high at about 3 mA so that the collector-base leakage current is relatively small, but even transistor selection could not ensure that the leakage current differences would remain less than the necessary $\frac{1}{2} \times 2^{-6} \times 3\text{mA} = 25\mu\text{A}$ over a practical temperature range of 20°C to 50°C. The available components therefore limit the equipment to a temperature differential of about 10°C unless the transistors are placed in a simple regulated oven.

The current source transistors run continuously and can feed, via diodes, either the weighting network or a bypass load, depending on the potentials on the diode anodes. The switching method is illustrated in Figure 3.17. The bypass load is connected also to a transistor clamp which, when operated by the setting of its store, cuts off the bypass diode and forces the current source to supply the weighting network. In this condition the bypass diode does not load the network node, and the forward drop across the network diode does not affect the node voltage. When the clamp is released by the resetting of the store, the source can supply the bypass load, and this resistance is chosen so that the voltage drop across it cuts off the network diode. In this condition the network is unaffected because the node is loaded with the high back-resistance of the network diode. A photograph of the output of the weighted-voltage generator for the code 000000 is given in Figure 3.18; for this code every voltage is removed after trial because the input

voltage is zero. Figure 3.19 is a photograph of the output for the code 111111, and here the voltages are seen to be all retained after trial. The C.R.O. vertical sensitivity is halved for this photograph. In Figure 3.20 is shown the output for the code 011000; here the retention of the second and third voltages and the rejection of the others can be seen clearly.

3.2.2.7 Master Oscillator, Divider Chain and Time-slot Matrix (Figures 3.21 and 3.22)

The fundamental timing of the modulator is derived from an astable multivibrator. This drives a chain of four bistable multivibrator dividers by collector triggering. The outputs of these dividers are combined in order in the 16 outputs identifying successive time slots. These diode AND gates can be conveniently laid out in an orderly pattern (see Figure 3.4) which prompts the title "matrix" for the set of diodes. Those outputs which feed the blanking OR gate are taken first through emitter followers so that the diode AND gates willnot be heavily loaded. A typical timing pulse, that for slot 1, is shown in Figure 3.23.

The triple-width synch pulse, which occurs in the same position in all frames, is generated by the omission of a blanking pulse in slot 14, and the double-width sampling pulse uses slots 15 and 16.

3.2.3 Performance

The sampling and coding parts of the modulator were checked by measuring the static linearity of the voltage-to-code conversion, the correctness of coding at frequencies up to 20 c/s, and the temperature stability of the unit.

3.2.3.1 Coder Linearity

The modulator input was supplied from a metered variable-voltage source and the input output

code was observed on a CRO. The input voltage was then increased steadily from zero to -5 volts, and the voltages at which the code changed were noted. The input was then steadily decreased from -5 volts to zero, and again the voltages at which the code changed were noted.

No significant difference was observed between the results for the two directions of scanning, other than the expected consistent shift of one step. However, the instant of a code change was ill-defined because the boxcar droop caused the last code pulse to be too narrow at the onset of its appearance and then to grow to full width as the input changed. The results plotted in Figure 3.24 give the voltage at the instant when the last code pulse was barely fully-formed.

The best-fit straight line drawn on the transfer characteristics shows the staircase to be a series of straight segments of slightly lower slope, separated by high-step discontinuities which are most predominant every 16 steps. This indicates that the second largest weighted voltage is slightly higher in tolerance than the others.

The best-fit line also shows that full-scale code corresponds to an input voltage of -4.4 volts instead of the desired -5 volts. This is due to incorrect scaling in the weighted voltage network and results from the unavailability of the desired component values in Zener diodes and high-stability resistors.

3.2.3.2 Dynamic Coding

A technique was devised for observing the correctness of the code formation and, to some extent, the linearity of coding at frequencies up to the sampling limit.

The horizontal deflection of a CRO was synchronized to the modulator frame rate and the vertical deflection was obtained from a ramp voltage connected to the modulator input. Z-modulation of the CRO beam was then obtained from the modulator output. As the vertical deflection changed, the output code passed through all its combinations and brightened the raster to form a binary-coded mask. This effect is sketched in Figure 3.25; it was not possible to obtain a satisfactory photograph due to difficulties with CRO persistence and film speed.

The linearity of the coding could be observed by noting that all the binary patterns were produced in the right order and that each code band occupied about the same vertical deflection. It was concluded that the operation of the coder was correct up to 20 c/s.

3.2.3.3 Temperature Stability

A stable d-c voltage was applied tothe input of the modulator, and the ambient temperature of the unit was slowly cycled from 20°C to 35°C and back again, while the output code was observed. A maximum change of one digit (1 in 2^6) was noted, although, due to the quantitizing process, this drift was a functions of the actual input voltage.

No drift over one hour at a constant temperature was detected.

3.3 Demodulator

The decision to use a weighing coder in the modulator was influenced by the need for a decoder, and, in fact, an identical weighted voltage generator is used in the demodulator unit. Due to the serial code transmission, the decoded voltage is not available until the end of the frame and it is therefore necessary to sample the voltage at this time and filter it by storage throughout the next frame.

Synchronization of the demodulator timing with the incoming

frame is achieved by means of flywheel synch operating at frame-rate but controlling the timing oscillator at pulse-rate. In this way regeneration and decoding of the pulses can be done from only frame-rate information, giving the least wastage of channel bandwidth.

The re-timing of the code pulses is separated from the decoding so that repeater stations may use this part of the equipment without modification.

3.3.1 Block Diagram

The arrangement of the demodulator is given in Figure 3.26. It shows some similarity to the modulator except that it has no comparator but it has a regenerator and a synch system.

The code pulses are taken to six coincidence (AND) gates, each of which has as its other input one of the demodulator time slot pulses derived from the timing unit. Each gate produces an output if a code digit occurs in that time slot, and this output triggers a binary store to switch on a weighted voltage from the generator.

A store can be set only by a pulse received from its coincidence gate, which occurs only when a code digit is present in the strobed time slot. If no digit is present the store remains in its reset state, and the main resetting pulse applied to all stores at the end of each frame has no effect upon it. In this way the weighted-voltage sum generated by all the stores depends on which of the digit slots were filled by the modulator, that is, on the code transmitted. By arranging the weighted voltages to decrease the binary sequence and to be switched on by code digits in the order in which the digits are received (greatest weight first), the sum of the voltages at the end of a code group is made proportional to the sample coded in the modulator. The photographs in Figures 3.27(a) and (b), show the voltage-generator output for codes of 111111 and 011000 respectively. Just prior to the resetting of all the stores the sum voltage is sampled and held in a boxcar circuit while the next code

is demodulated. This introduces a delay equal to the period of one frame between the taking of the sample in the modulator and the reproducing of it in the demodulator. A lowpass filter may be used finally to restore the analogue output to the same spectrum as the analogue input.

The demodulator timing pulses are generated in the same way as in the modulator, except that the oscillator is frequency-controlled by a voltage derived from its output and the incoming synch pulse by the synch detector. The synch pulse is separated from the regenerated demodulator input by an integrating process which makes use of its unique triple-width.

3.3.2 Circuit Description

Those circuits which are identical to the corresponding ones in the modulator are not described here. Where differences occur between similar circuits, these are noted. Time slot pulses are identified by their positions within the demodulator frame, and do not necessarily have the same absolute time of occurrence as identically numbered slots in the modulator because every regeneration of the code introduces a delay.

3.3.2.1 Regenerator (Figures 3.28, 3.29 and 3.30)

A positive voltage, equal to the average pulse-height measured over several frames, is generated in a leaky peak-detector, and the input signal, clamped to allow only negative excursions, is added to it by means of transformer-coupling of the input. After buffering by an emitter follower the sum is taken to the limiter/slicer, which is a differential amplifier with the second input held at the optimum slicing level, namely zero. Two outputs are provided: the first, a signal swinging from earth to the negative supply rail, is taken to the synch separator, while the second is shifted

positively by half the supply voltage and taken to the reset integrator shown in Figure 3.30. This is a simple RC filter which is reset by shunting the capacitor with a transistor switch. The discharge current flowing through a small resistance in series with the switch causes a voltage pulse whose polarity is that of the charge which was on the capacitor. This pulse is amplified in a common-base stage buffered by an emitter follower, and fed both to the "set" side of the same flipflop and via an inverter to the "reset" side of the same flipflop. The inverter is biassed to be just nonconducting, so that positive input pulses have no effect on it, while negative pulses drive it to saturation. In this way the flipflop receives positive trigger pulses on both inputs, being set if the integrator charge is positive, and reset if the charge is negative. Consequently, it changes state every time the integrator changes polarity, but the flipflop transitions can occur only at instants defined by the synch system, and they therefore represent the regenerated pulses.

3.3.2.2 Coincidence Gates (Figure 3.31)

The restored signal from the regenerator is supplied to an emitter follower. Thisprovides the low impedance needed to drive the six diode AND gates which strobe for code pulses. These gates are similar to those used in the modulator for the same purpose, except that the time-slot numbers are different.

3.3.2.3 Stores (Figure 3.32)

The basic flipflop is the same as the modulator uses, except for the triggering inputs. The coincidence gate provides the only setting pulse, and the main reset pulse is always applied to the opposite collector.

3.3.2.4 Timing Oscillator (Figure 3.33)

The synch system is arranged so that the oscillator

frequency must rise with increasing control voltage, and the synch detector gives an output which is less than the oscillator supply voltage. An astable multivibrator is used for the oscillator, with its capacitor discharge resistors returned to the control voltage, as shown in Figure 3.33. Its half-period $t = RC \log_e(1 + \frac{V}{V_C})$, so that for $t = 0.5$ m sec, $\frac{V}{V_C} \doteqdot 0.5$ and $R = 40$ KΩ to give reasonable base isolation $C = 0.005\mu f$.

The timing resistors are made partly variable with ganged potentiometers to accommodate variation in the initial frequency of the modulator oscillator while still keeping the synch system in the centre of its control range. The full circuit is given in Figure 3.33.

3.3.2.5 Synchronization Control

The received synch pulse is unique in being triple-width, and it is separated after the pulse regenerator by detecting its width with an integrator. The pulse from the synch separator has a width of about one time slot and is called the synch pulse within the demodulator.

The synch detector (Section 2.2.3) has a certain phasing of its two input signals at which relative slip produces a sudden change in its output, and this, after filtering, becomes the oscillator control voltage. Synchronism can be obtained if the synch pulse is used for the clamp bias voltage and a frame-rate signal derived from the controlled oscillator is used for the other input. Since it is necessary that the latter signal have a larger mark/space ratio than the synch pulse, the output of the last binary divider is used for the purpose.

In the absence of a code input, the frequency of the demodulator oscillator is lower than synchronous but within the pull-in range and it rises when synch pulses slip through the synch detector until the two frequencies are equal.

When the loop is synchronized the negative transistions of the two synch detector inputs occur at the same instant, so the numbering of the time slots is based on the position of the front edge of the synch pulse in the frame. There is actually a small static phase error which would cause a difference of about half the width of the synch pulse between the modulator and demodulator timings, but this is overcome by shifting the edge of the synch pulse appropriately.

3.3.2.5.1 Synch Separator (Figure 3.34)

The synch separator comprises an integrator, a voltage-slicer and a pulse amplifier.

The integrator uses an RC circuit with a charging time-constant of about two slots for negative signals, but a discharge time-constant of about one-fifth of the slot period so that the capacitor does not build up a pattern-dependent charge. This is done with a resetting diode. Figure 3.35 shows the integrator action on a frame containing the code 011000 and a synch pulse.

The slicing amplifier compares the integrator output with an adjustable voltage and produces an output pulse when the slicing level is exceeded. It uses an emitter-coupled differential amplifier which switches the second transistor rapidly between the conducting and non-conducting states; this signal is coupled to a regenerative amplifier to produce a standard-height pulse. Two of the resulting synch pulses are shown in Figure 3.36 for which photograph the oscilloscope trigger

was the same as for Figure 3.35. Variation of the preset slicing level alters the width of the synch pulse and the position of its negative transition relative to the end of the frame.

3.3.2.5.2 Synch Detector and Filter (Figure 3.37)

The two inputs to the synch detector clamp are driven by PNP emitter followers to provide rapid charging of the clamp capacitors, and the synch pulse input is direct-coupled from its amplifier to retain the correct voltage levels. Figure 3.38 is a photograph of the detector output in the synchronized condition, showing the stable phasing of the system.

The filter contains both lag and lag-lead sections to control the pull-in and jitter. In this equipment it must provide good rejection of the frame frequency so that the oscillator which is controlled by its output will not be greatly modulated at this frequency, for this would affect the demodulator timing. The filter output voltage is shown in Figure 3.39 at a scale of 50 mv per centimetre, and its effect on the oscillator is indicated in Figure 3.40 for which the oscilloscope was triggered by the leading edge of each oscillator pulse so that the modulation could be viewed as jitter of the trailing edge; the modulation effect can be seen to be negligible. Another photograph of the oscillator output is given in Figure 3.41.

3.3.2.6 Output filter (Figure 3.42)

A simple lowpass filter with a sharp cutoff frequency and good phase response is achieved by combining the steep slope of an LC half-section with the null of a parallel-T section. The half-section is chosen to show a peak in the region where the

parallel-T section starts to fall off, so that the overall response of the two cascaded sections is flatter in the pass-band. A compromise is made with the phase response, but this may be made fairly linear while yielding reasonable component values. The values shown are for a filter with a cutoff of 50 c/s designed for use in sampling experiments rather than for the PCM application. The characteristics of this filter are given in Figure 3.43.

3.3.3 Performance

The demodulator tests performed were measurements of the linearity of the decoder staircase and of the thermal drift in output voltage.

3.3.3.1 Decoder Linearity

The demodulator input was supplied with codes from the modulator, and the output voltage was measured after synchronism had been reached. The codes were swept steadily through their full range and the output voltage at each code change was noted for both increasing and decreasing voltages.

The results were almost identical to those for the modulator. This is not surprising because both units use the same component values and types in their samplers and weighted voltage generators.

3.3.3.2 Temperature Stability

A fixed code was supplied to the demodulator input, and the ambient temperature of the unit was slowly cycled from 20°C to 35°C and back again. The output voltage was monitored, and showed a maximum change of 55 mV.

The drift in output voltage over one hour at constant temperature was 17 mV.

3.4 Construction

The completed demodulator is shown in the photograph of Figure 3.44. The modulator is very similar in appearance, except for an additional row of circuits behind the panel.

Close-up photographs of parts of the units, showing the method of construction, are given in Figures 3.45, 46 and 47. The first of these shows typical stores and weighted voltage generators in the modulator, the second shows the demodulator current sources and resistor network, and the third shows the timing pulse matrix in the modulator. The circuits are made up on pairs of tag-strips spaced $\frac{1}{2}$-inch apart on brass rods which act also as busbars for supply voltages and signals. Each row of circuits is attached to the front rack-panel and is supported at the rear by spacing strips. Since many of the basic circuits are repeated in the equipment, consideration was given to a construction method using etched-wiring cards to mount and connect the components. However, the cost of commercial production of relatively small numbers of cards was prohibitive.

The only panel controls provided allow fine frequency control of the modulator oscillator and coarse frequency control of the demodulator oscillator. Input, output and power supply connections to both units are made on the front panels.

3.5 Performance of PCM system

A dynamic test was made of the full system using an imitation open-wire line as the link, but, although an experiment was devised for the purpose, it was not possible to conduct an investigation into the noise-threshold properties of PCM because the technique for detecting the frequency of errors was too complex for the facilities available. Instead, the equipment was used in an investigation of the spectra of sampled signals; this work is reported in Section 4.

3.5.1 Dynamic Response

Low-frequency signals were supplied to the modulator, which was connected to the demodulator by an equivalent one-mile open-wire line, and the output of the demodulator was observed.

The photographs in Figures 3.48 and 3.49 show the outputs obtained for sinusoidal and triangular inputs at 1.2 seconds per cycle and 2 volts peak-to-peak amplitude. No output filter was used in these experiments, which accounts for the presence of the sampling-rate component. Otherwise the reproduction appears to be excellent and bears out the results of the staircase linearity tests.

3.5.2 Noise-threshold Experiment

A proposed method for assessing the error-rate for different signal-to-noise ratios is shown in Figure 3.50. The PCM code is transmitted along two paths, one containing a simulated transmission link, a noise generator and the regenerator; and the other containing only a delay equal to that of the link and a pulse amplifier. Timing pulses taken from the regenerator are used to strobe the outputs of both paths in AND gates, which are combined so that an output is obtained only if the signals differ. Spurious pulses added by the line and regenerator will yield an output of opposite polarity to that from pulses which have been deleted so that these two types of error can be counted separately. A knowledge of the pulse rate then permits the error rate to be assessed for different code patterns if it is felt that the regenerator is pattern-sensitive.

Although no tests could be conducted, it is considered significant that during all the tests the equipment was operated in close proximity to an unsuppressed arc-welder without one apparent loss of synchronism or of significant code digits, even though the welder radiation was detected even on the power-supply rails of the equipment.

3.6 Conclusions

The successful implementation of all the requirements for a PCM system has been achieved in simple transistorized equipment. Novel circuits are used for sampling, coding, regenerating and synchronizing.

Available components restrict the accuracy of the equipment

to about 1% over a limited temperature range of 15°C, which is not satisfactory for field equipment. Nevertheless, it is considered that improved components - particularly transistors - will enable practical temperature ranges of 40°C to be reached at higher accuracy.

No obvious speed limitation was noticed at the low sampling rate used, but the technique of switching currents into inductive resistors in the ladder networks is a likely source of difficulty at the pulse rates of hundreds of kilocycles per second needed for speech transmission.

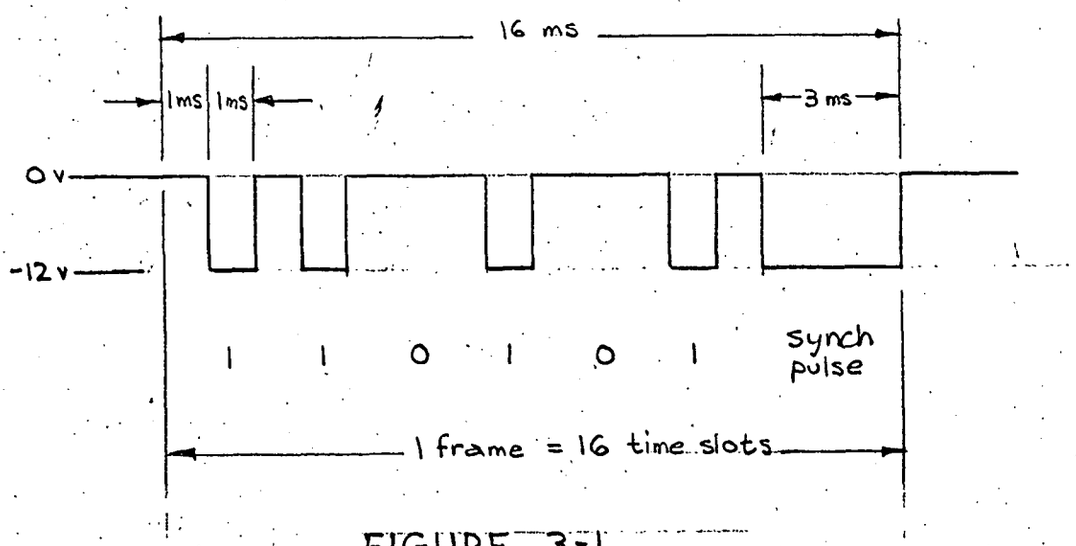


FIGURE 3-1

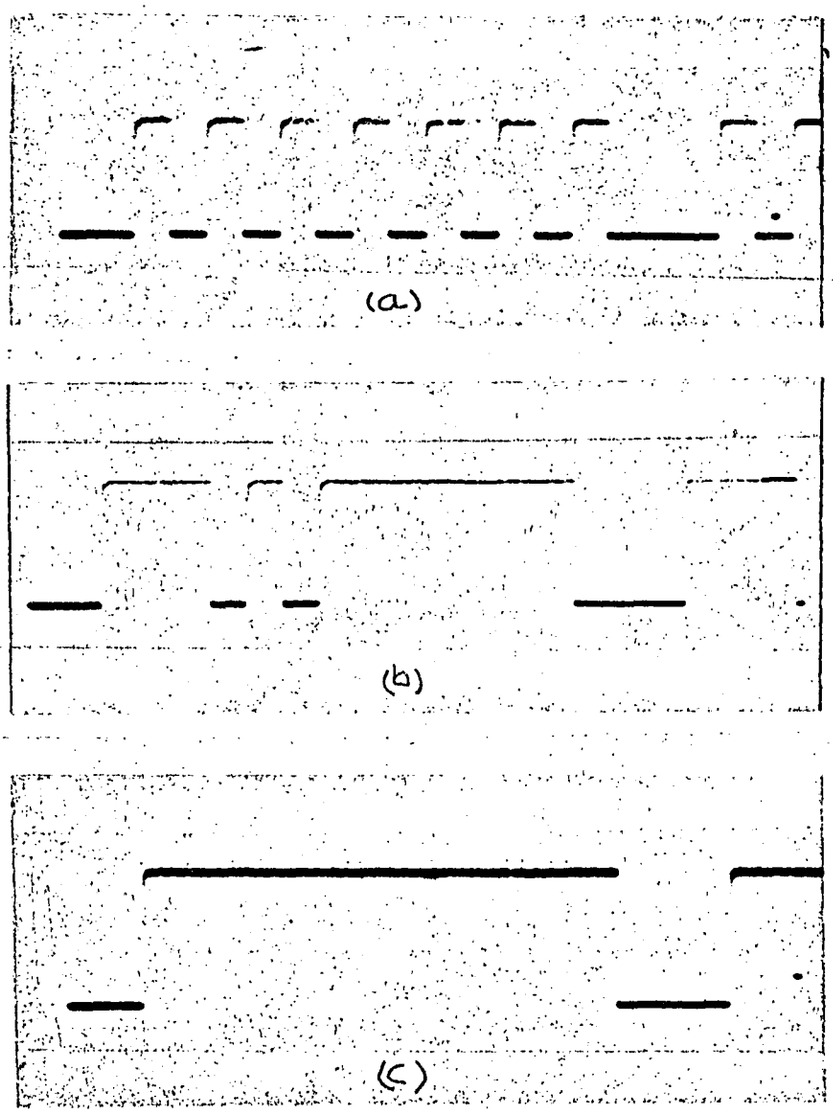


FIGURE 3-2

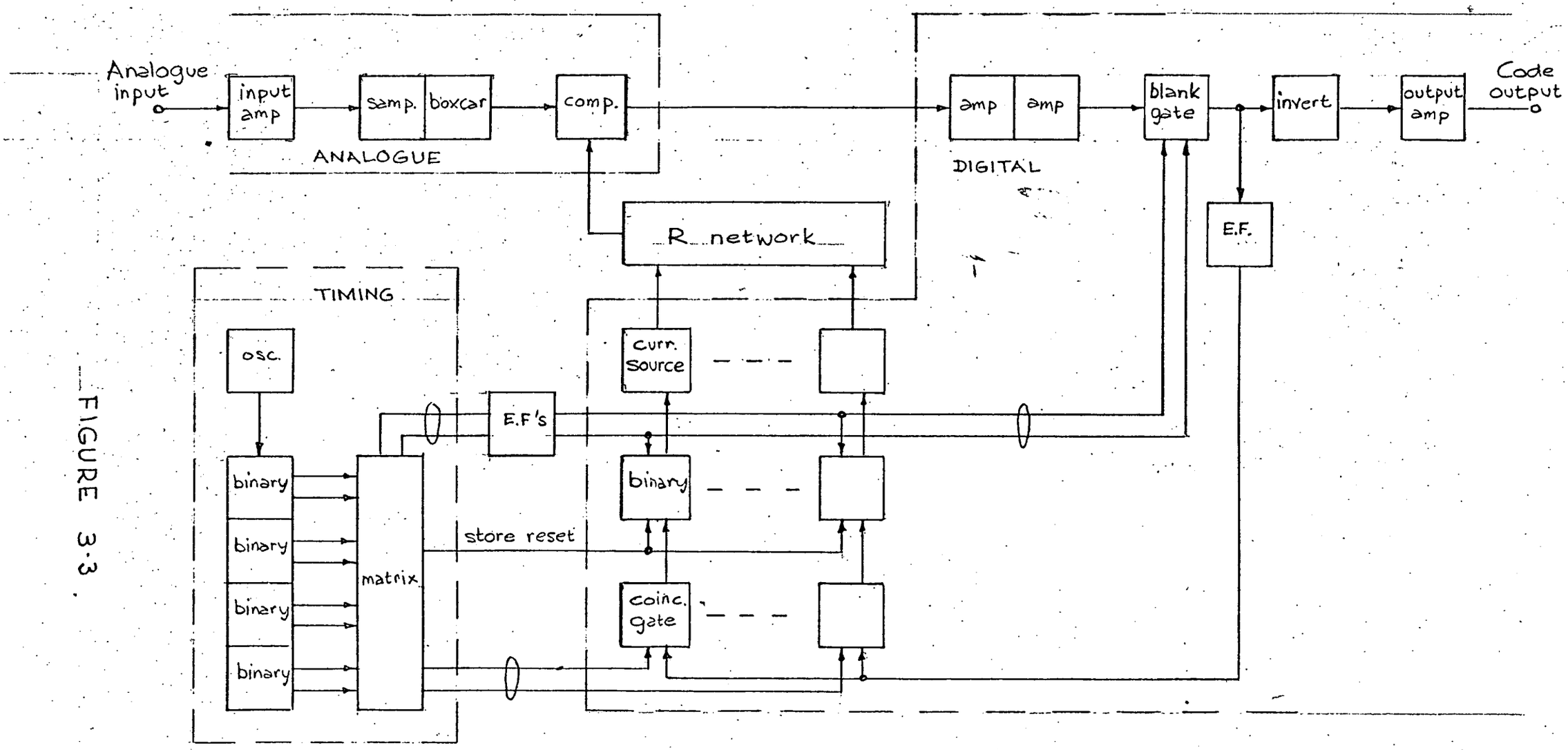

Analogue input
input amp
samp.
boxcar
comp.
ANALOGUE
amp
amp
DIGITAL
blank gate
invert
output amp
Code output
R network
E.F.
TIMING
osc.
curr. source
E.F's
binary
binary
binary
binary
matrix
store reset
binary
coinc. gate

FIGURE 3.3.

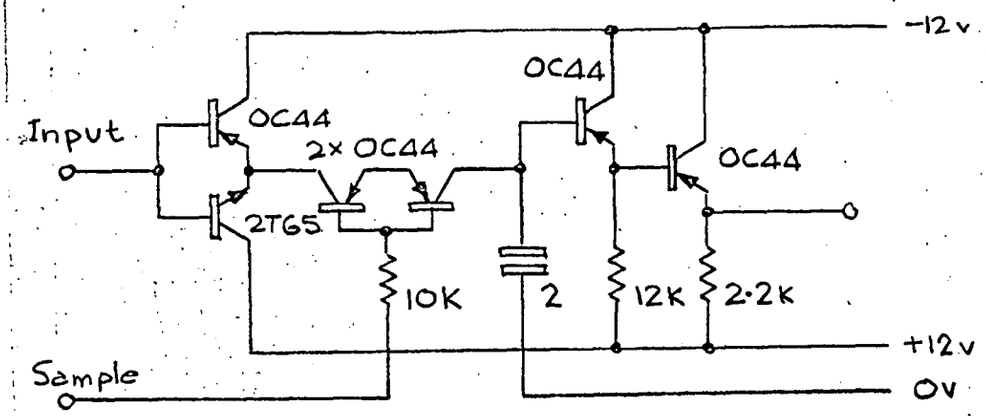


FIGURE 3-4

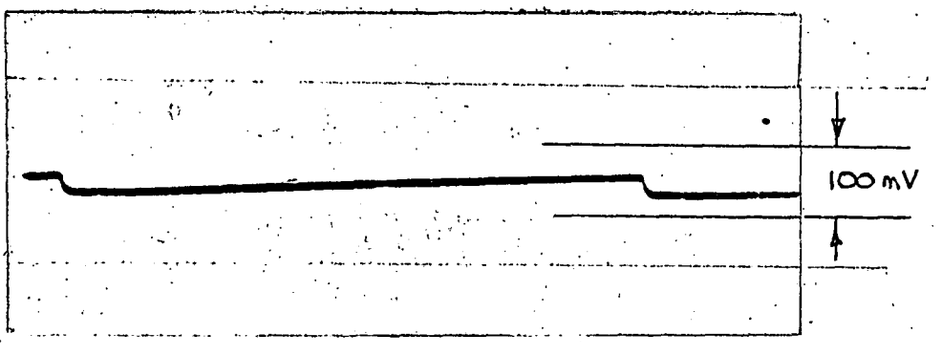


FIGURE 3-5

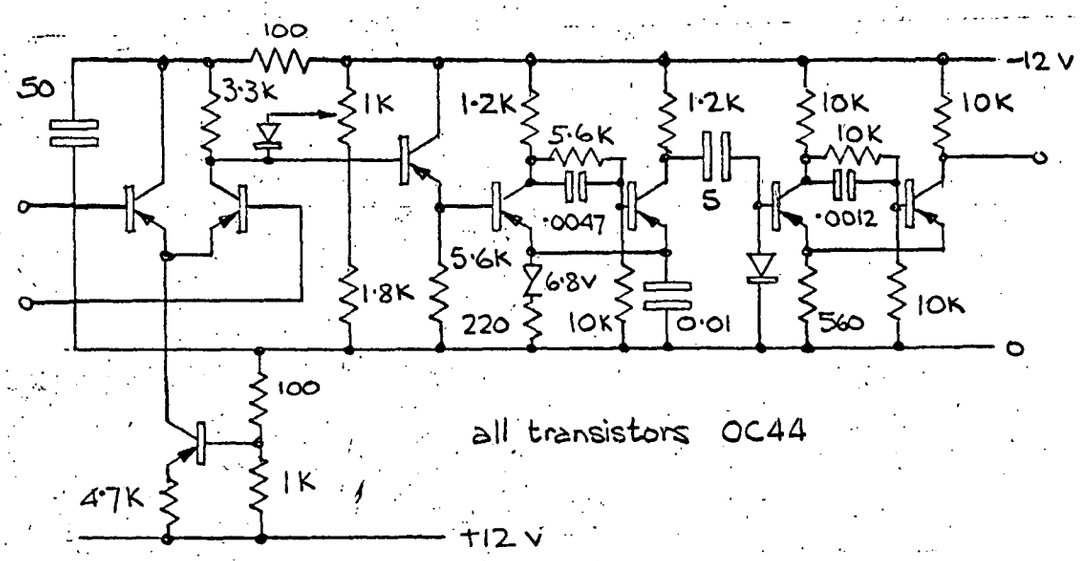


FIGURE 3-6

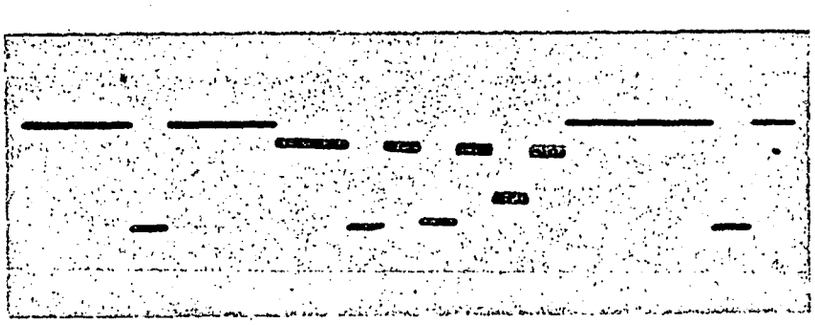
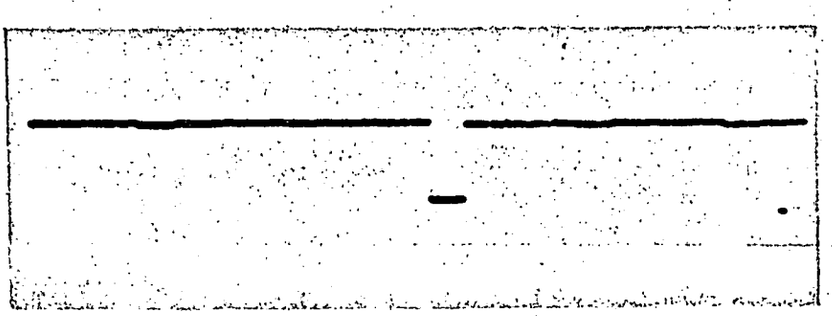
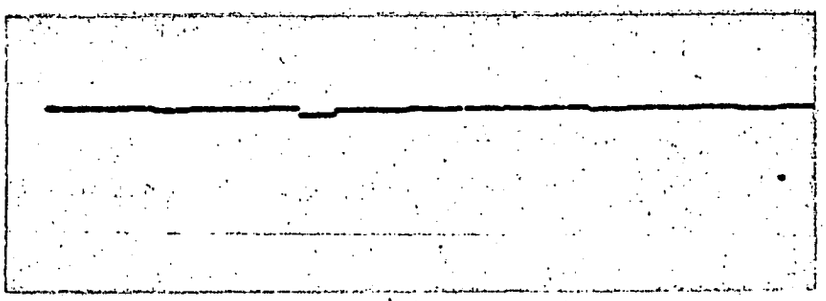


FIGURE 3-7



(a)



(b)

FIGURE 3-12

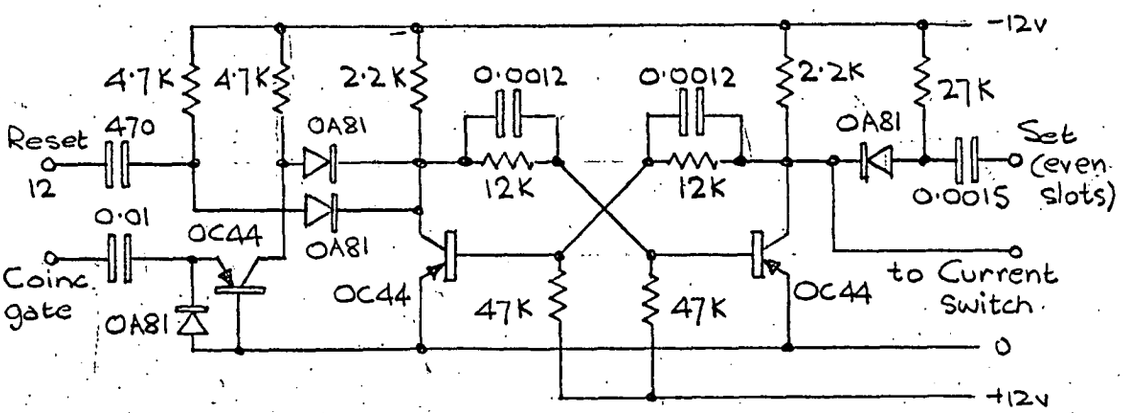
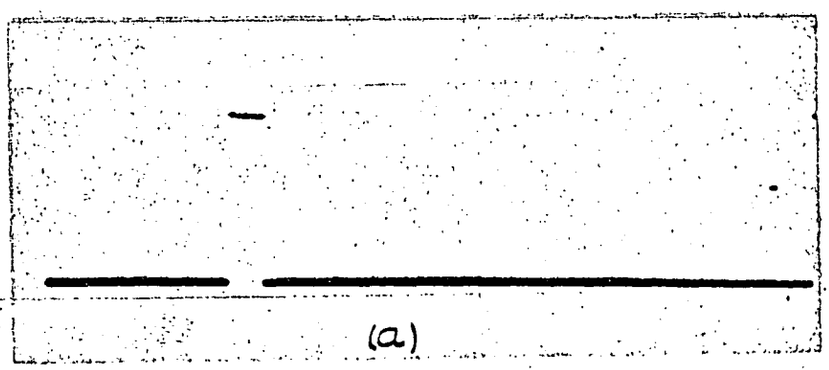
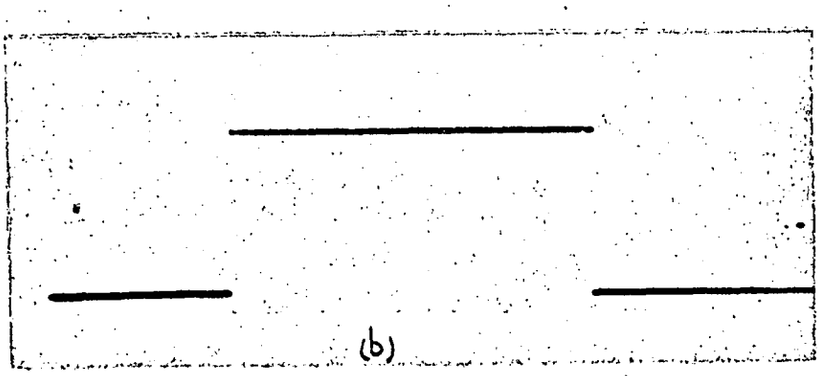


FIGURE 3-13



(a)



(b)

FIGURE 3-14

FIGURE 3-8

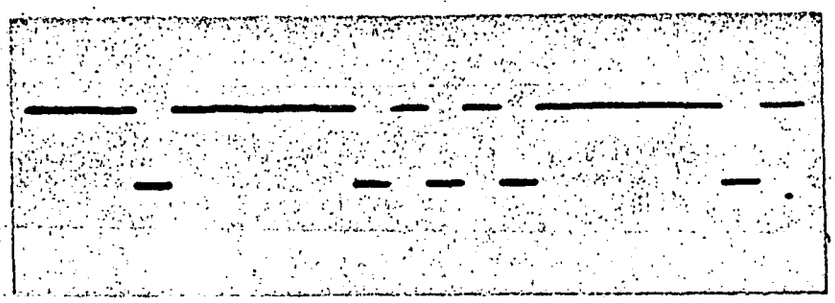


FIGURE 3-9

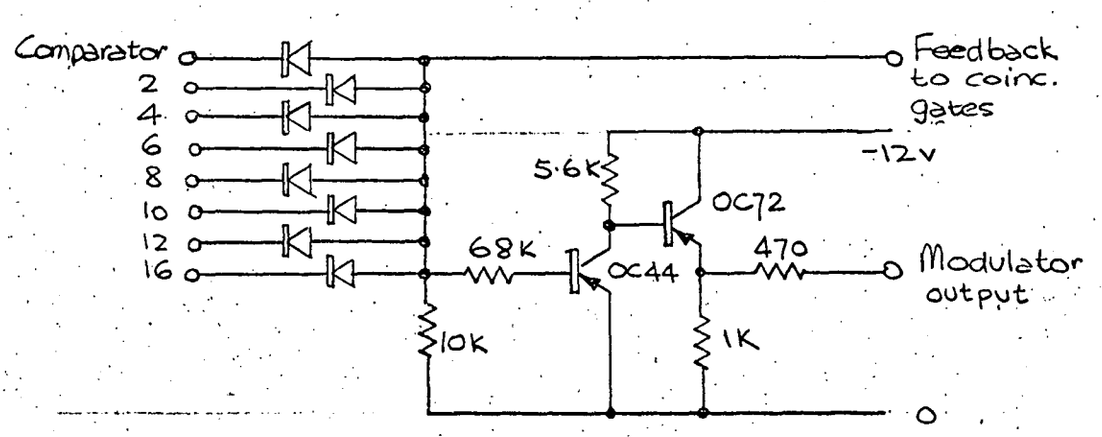


FIGURE 3-10

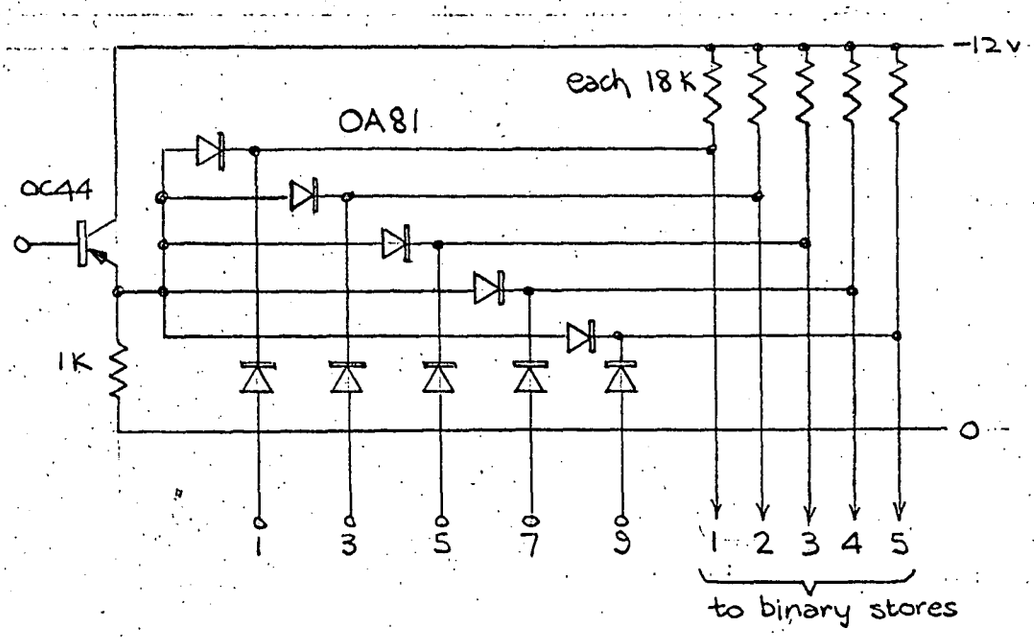


FIGURE 3-11

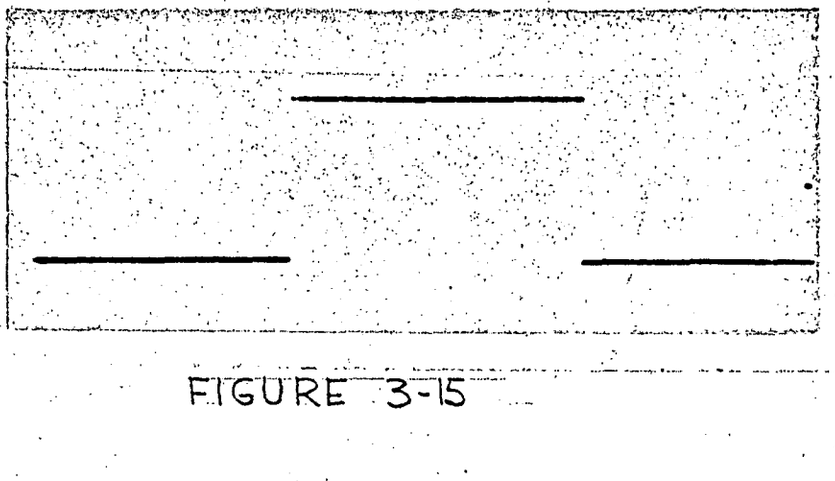


FIGURE 3-15

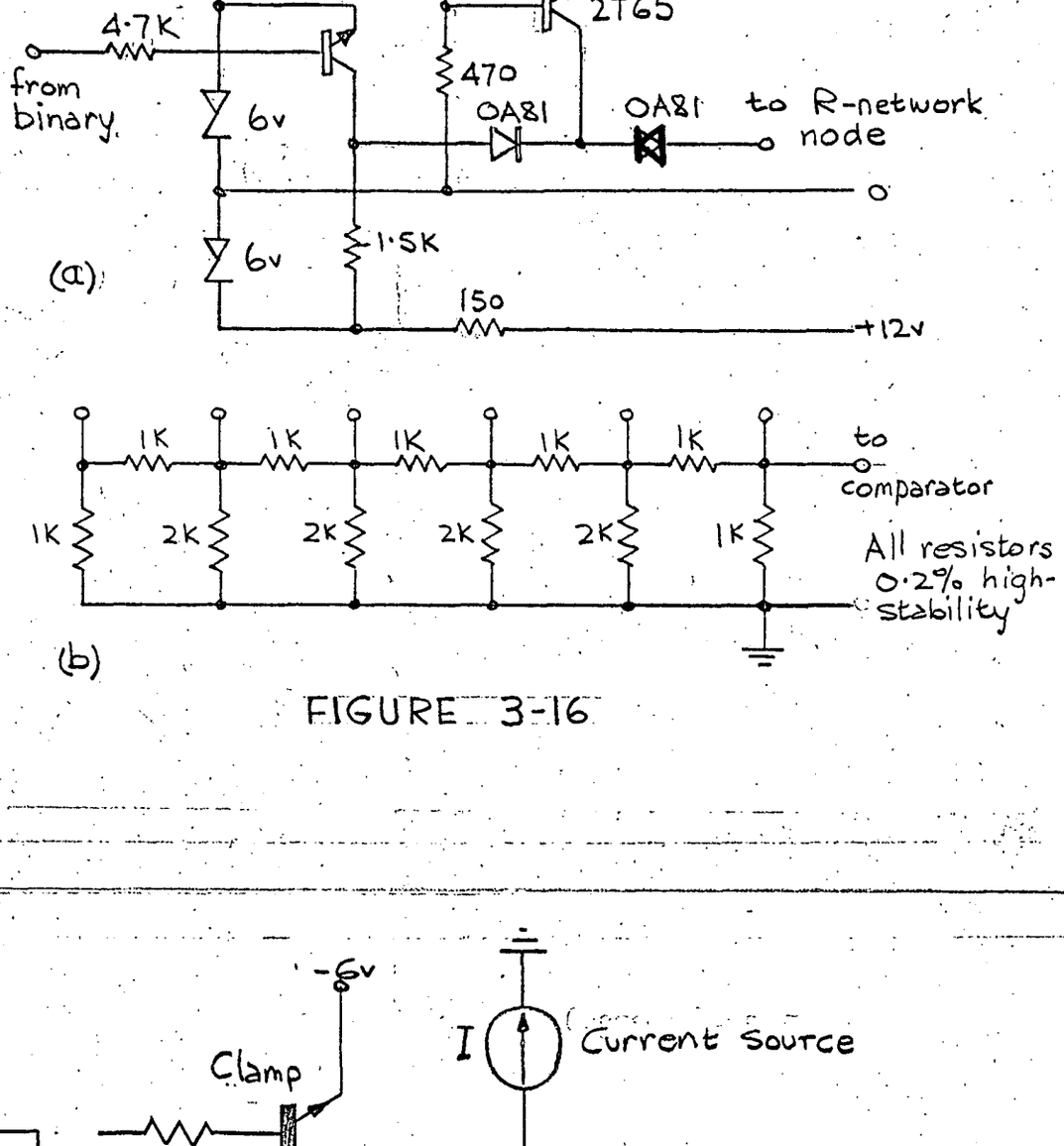


FIGURE 3-16

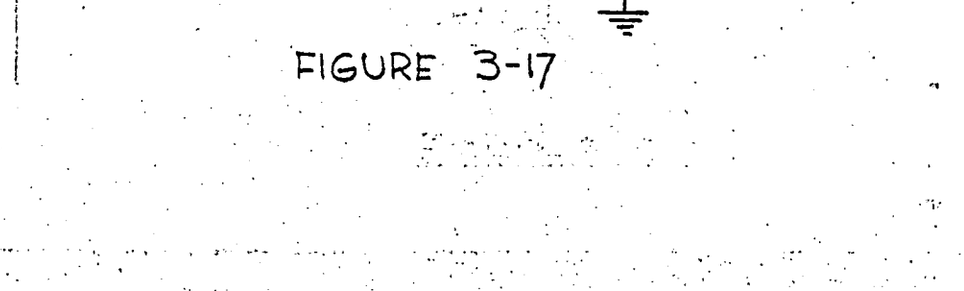
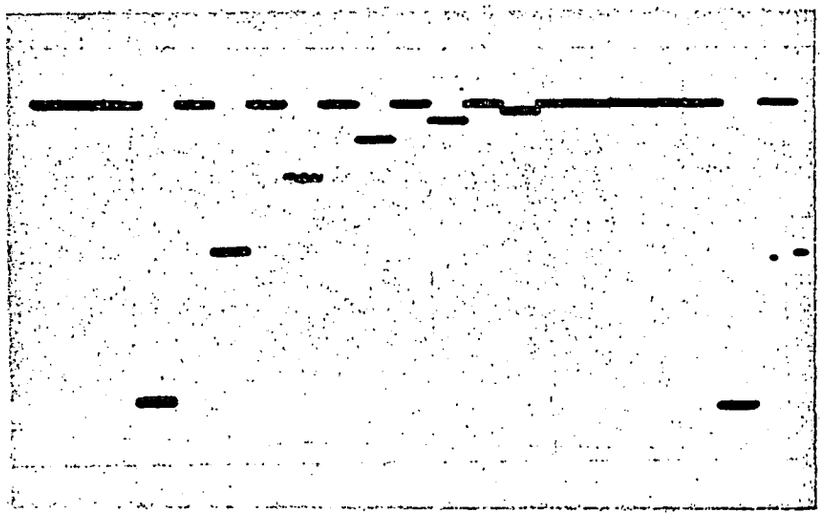


FIGURE 3-17



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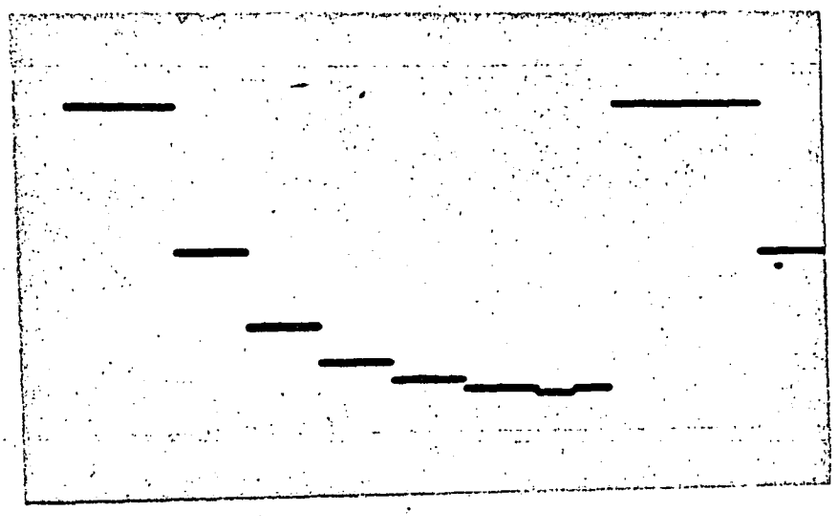

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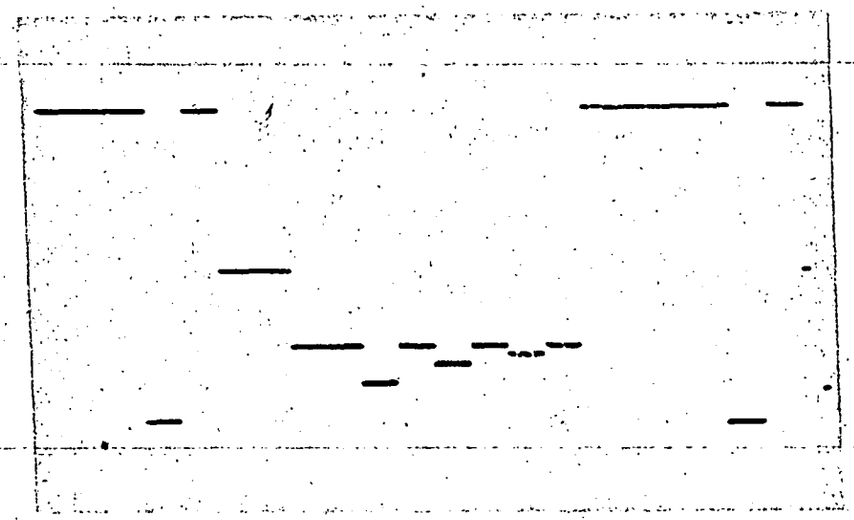

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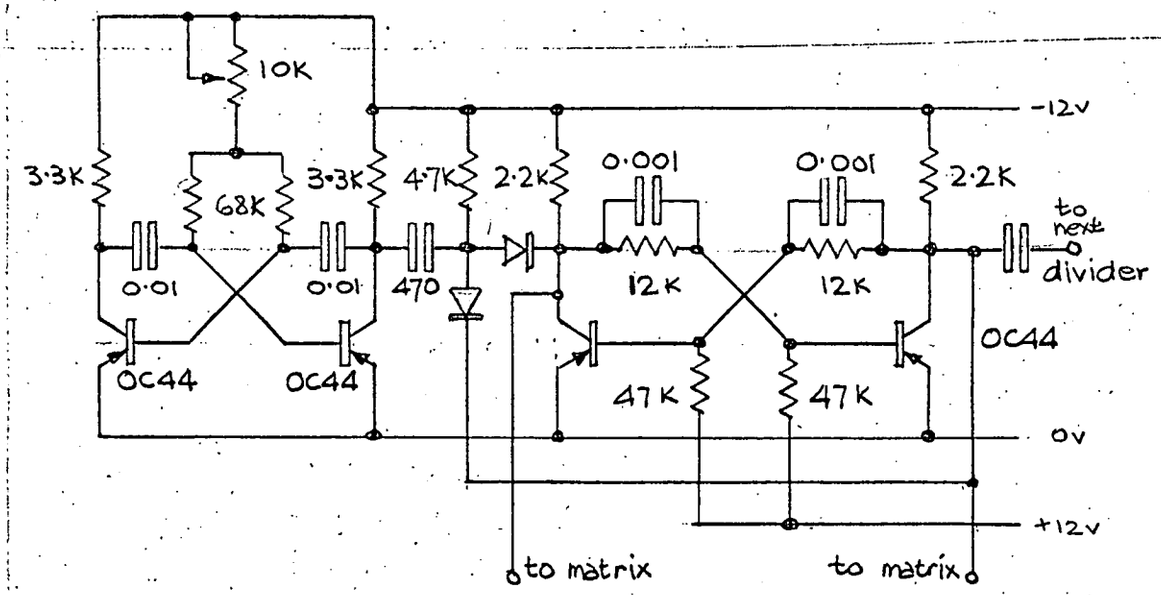

FIGURE 3-21

see next page

FIGURE 3-22

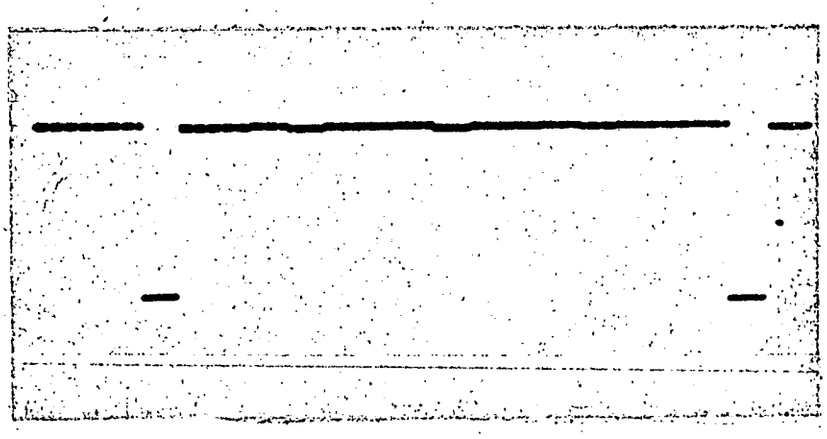

FIGURE 3-23

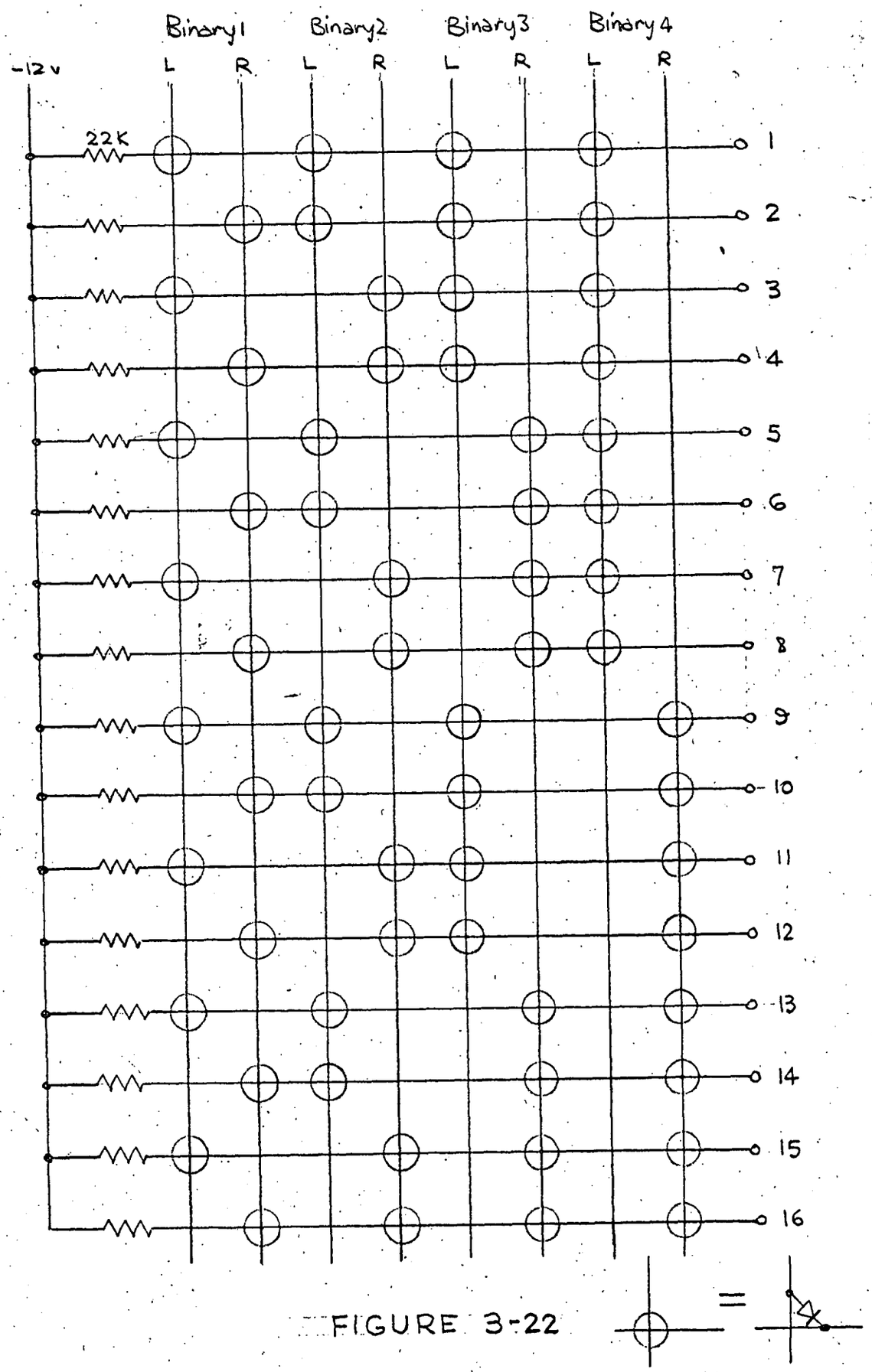
Binary 1
Binary 2
Binary 3
Binary 4
-12 v
L
R
22K
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
=

FIGURE 3-22

FIGURE 3-24

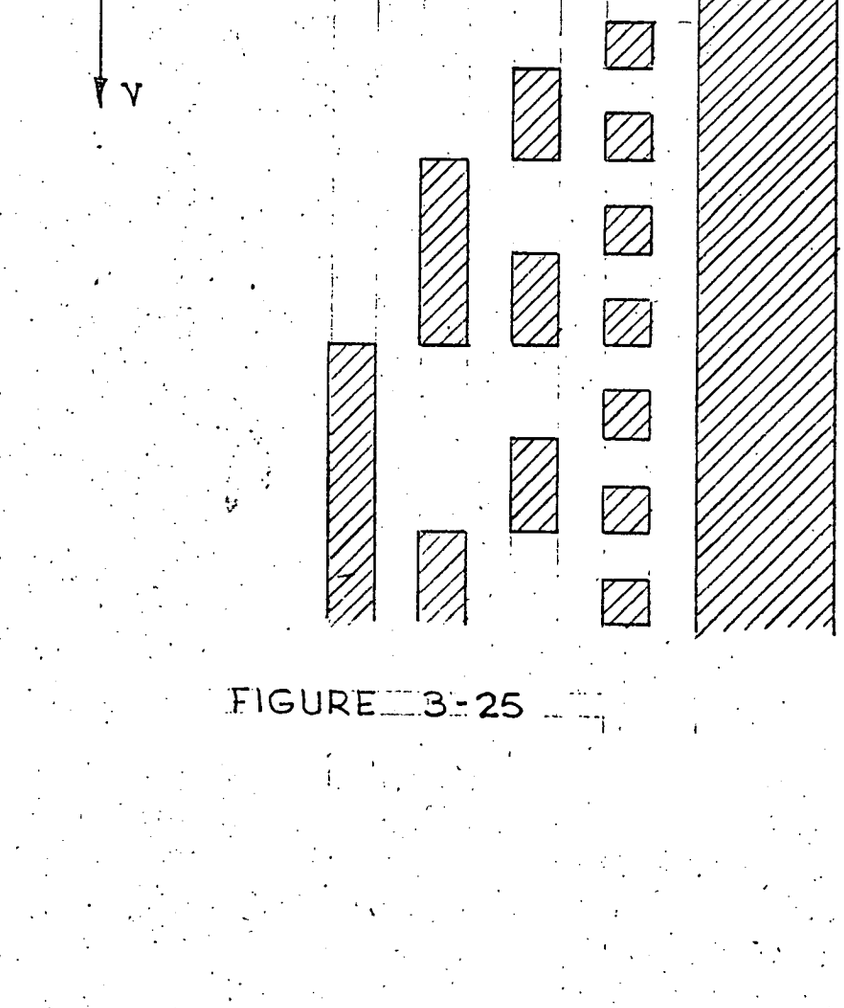

FIGURE 3-25

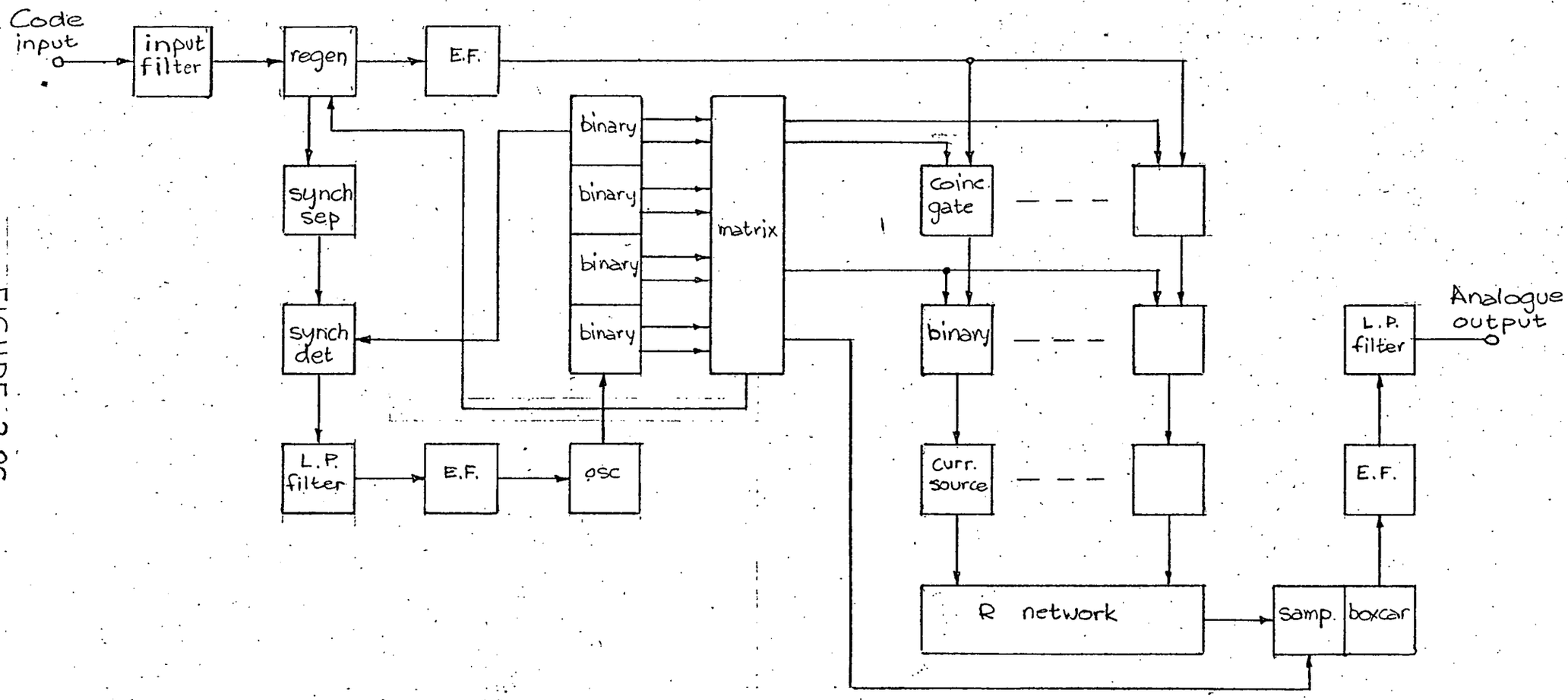
Code input
input filter
regen
E.F.
synch sep
synch det
L.P. filter
E.F.
osc
binary
binary
binary
binary
matrix
coinc. gate
binary
Curr. source
R network
samp.
boxcar
L.P. filter
E.F.
Analogue output

FIGURE 3.26

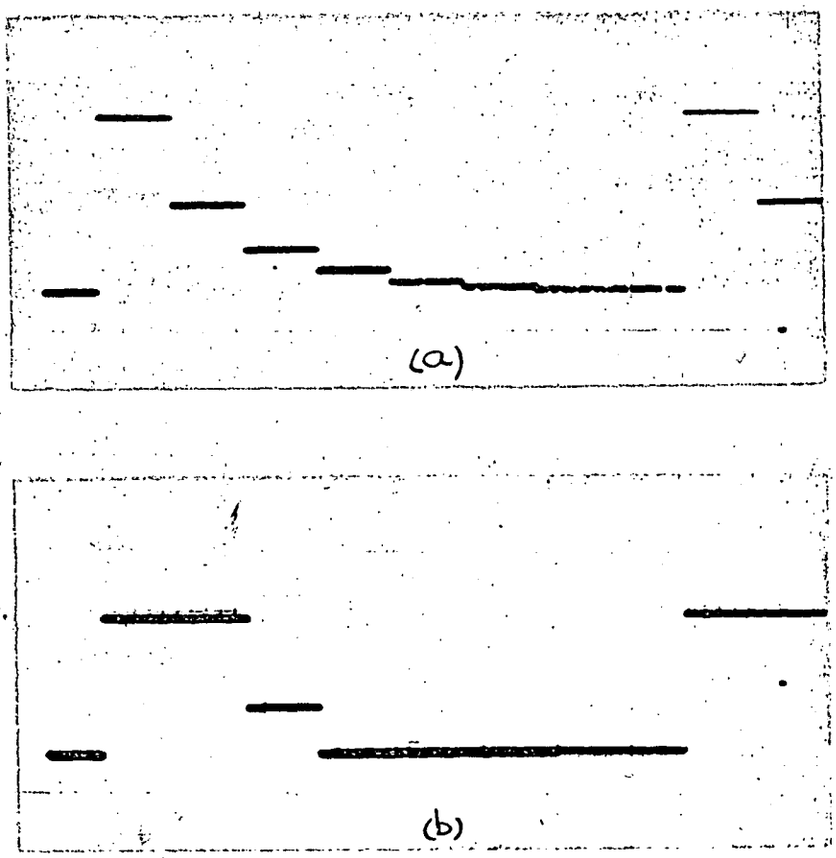

FIGURE 3-27

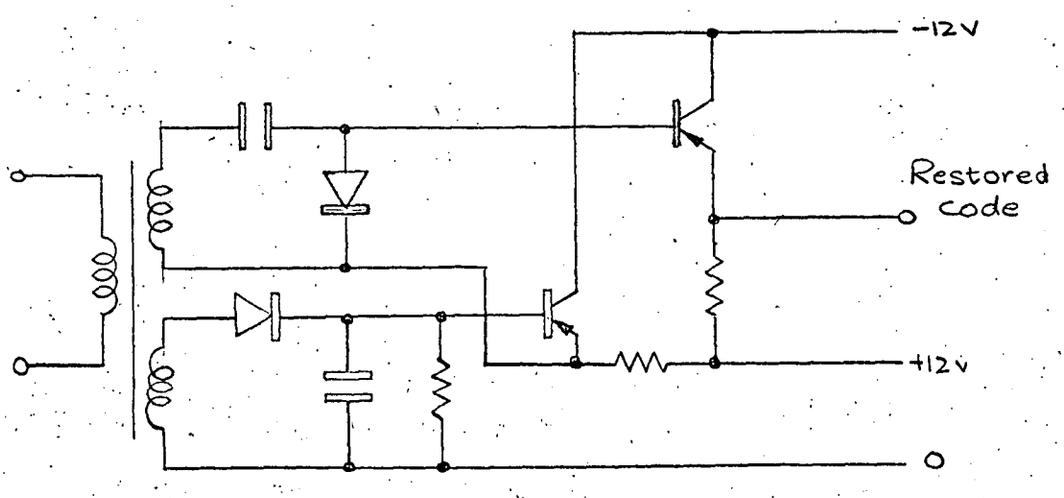

FIGURE 3-28

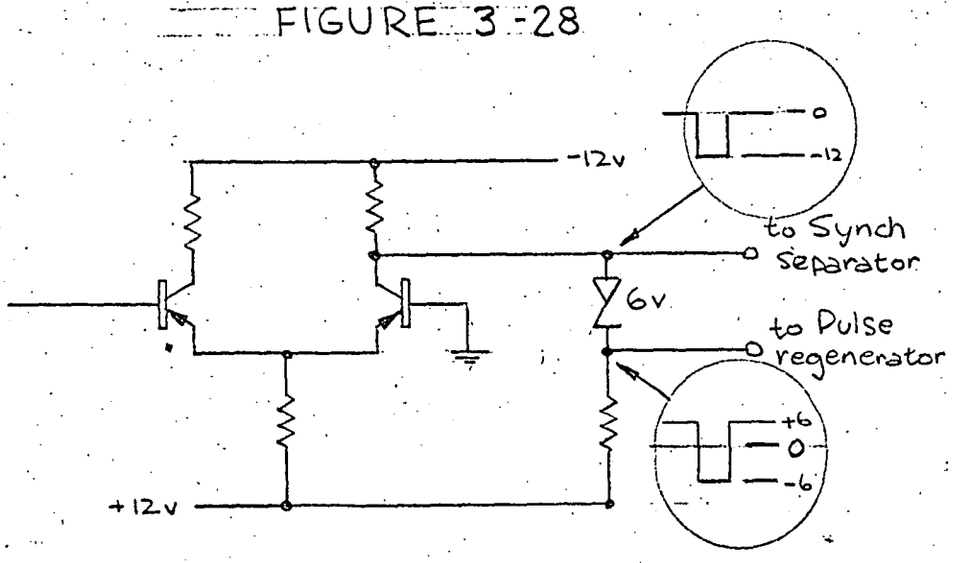

FIGURE 3-29

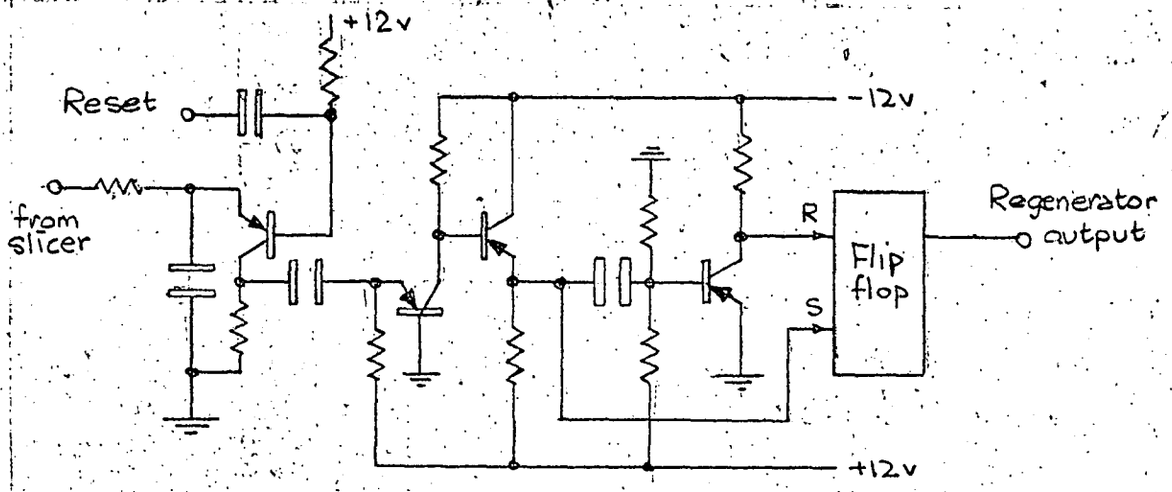

FIGURE 3-30

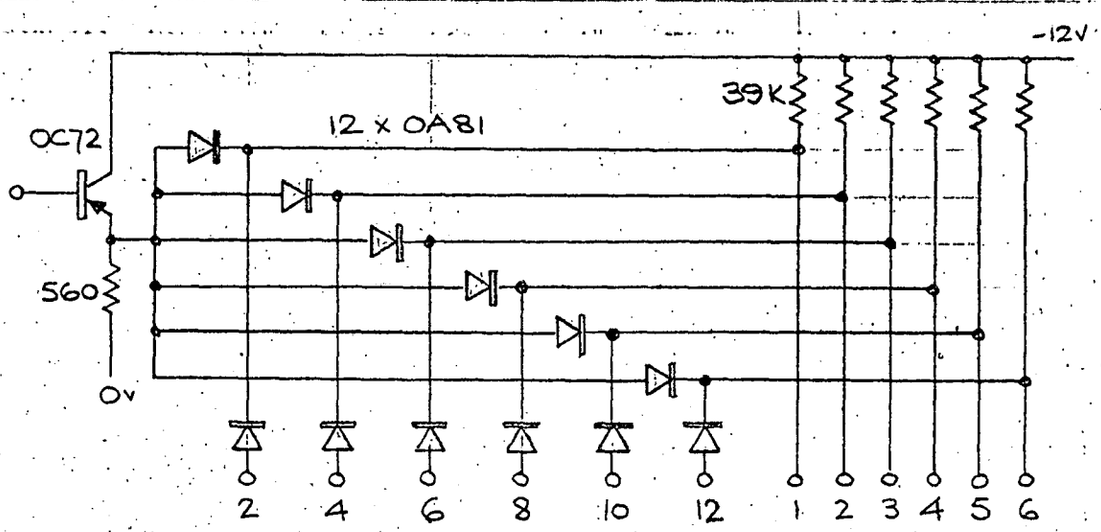

FIGURE 3-31

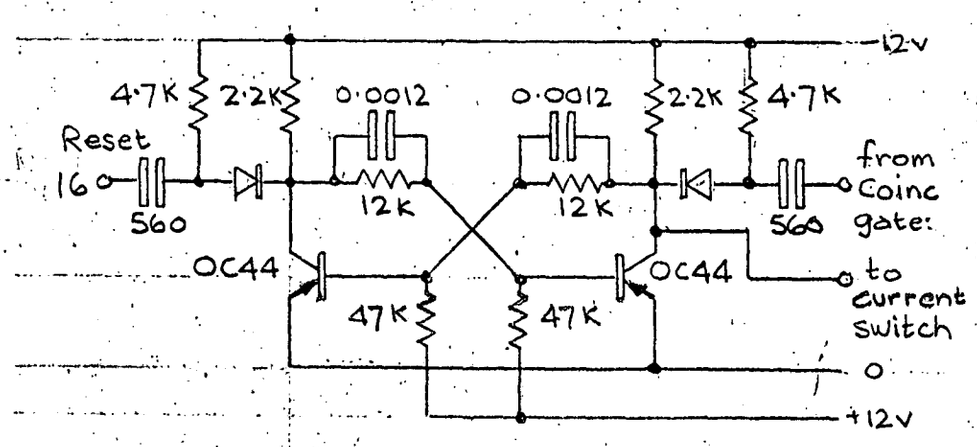

FIGURE 3-32

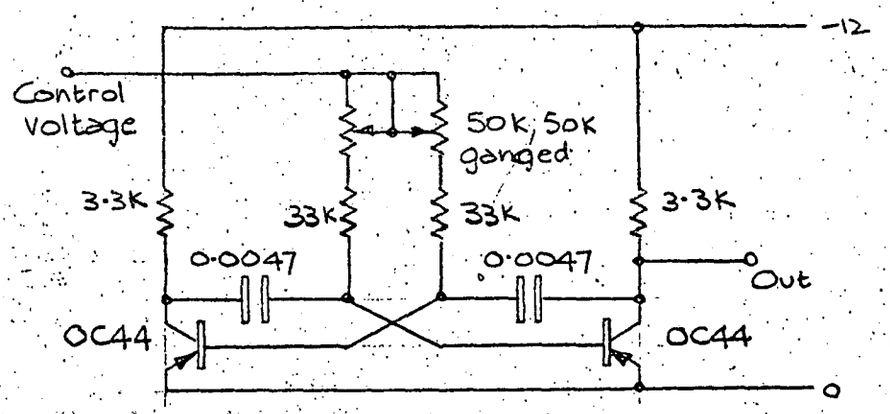

FIGURE 3-33

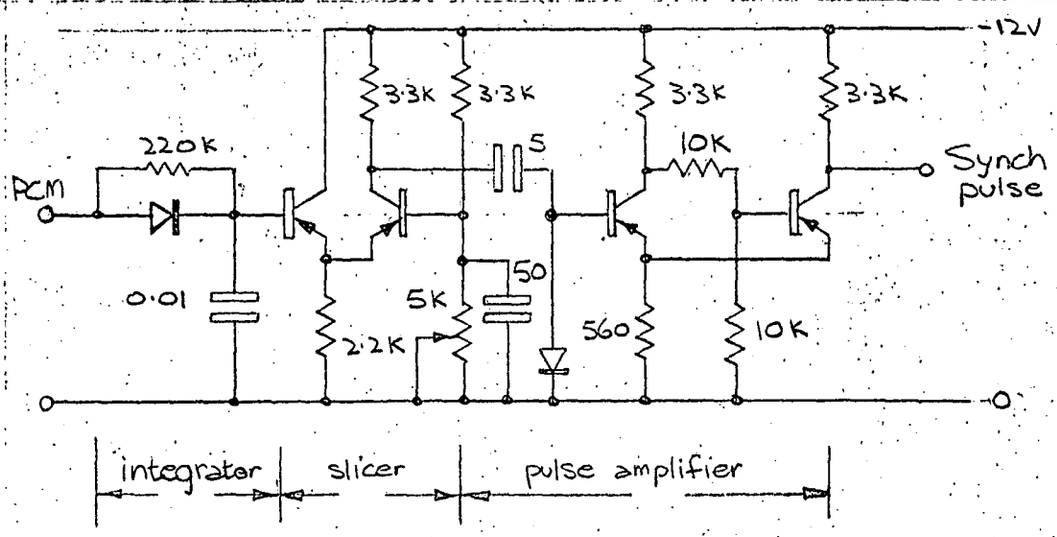

FIGURE 3-34

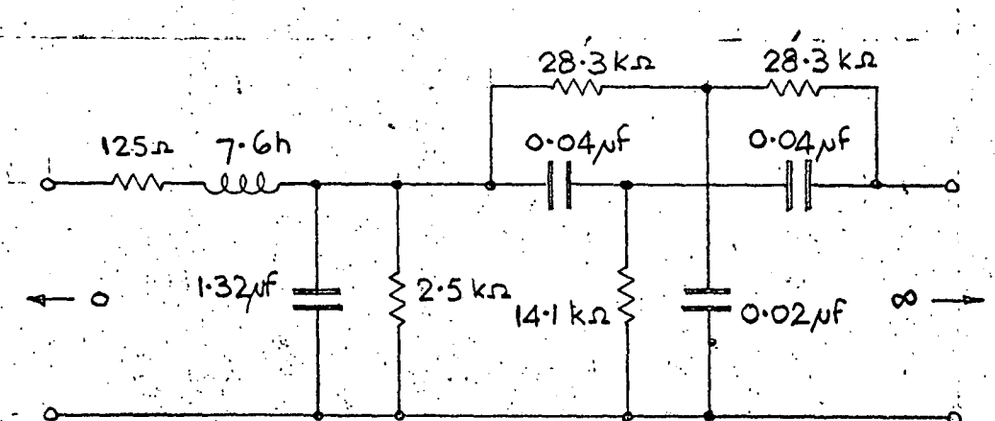

FIGURE 3-42

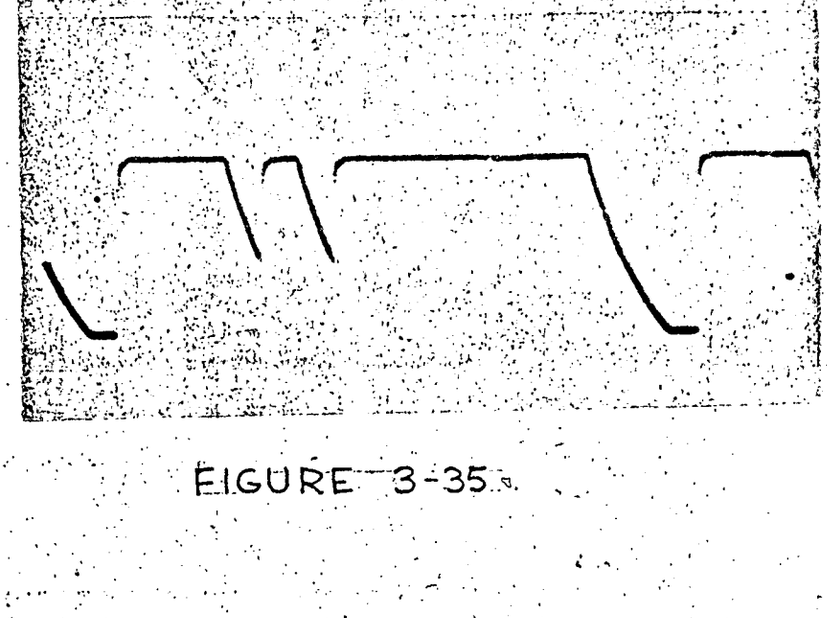

FIGURE 3-35.

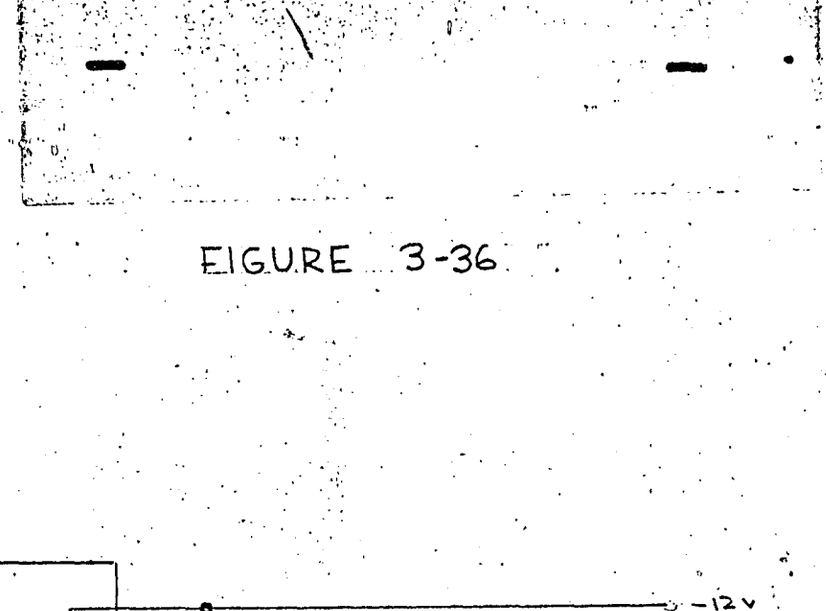

FIGURE 3-36.

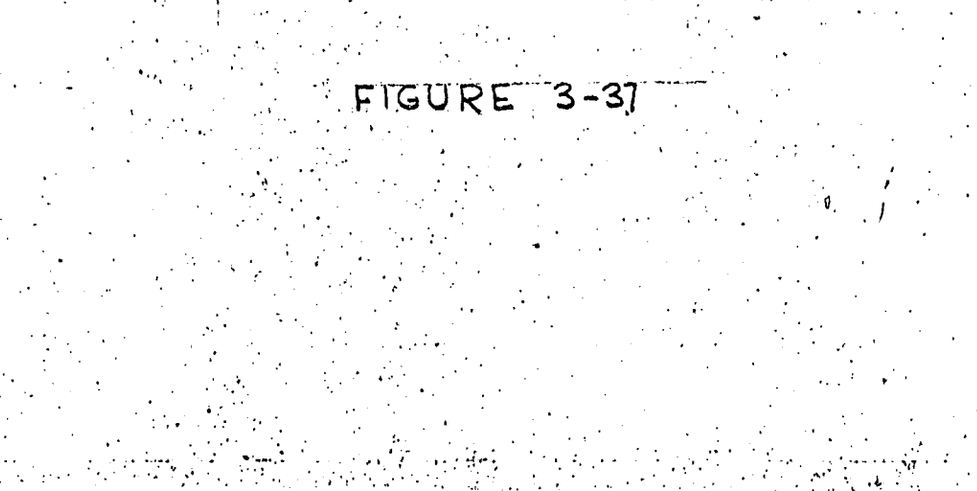

FIGURE 3-37

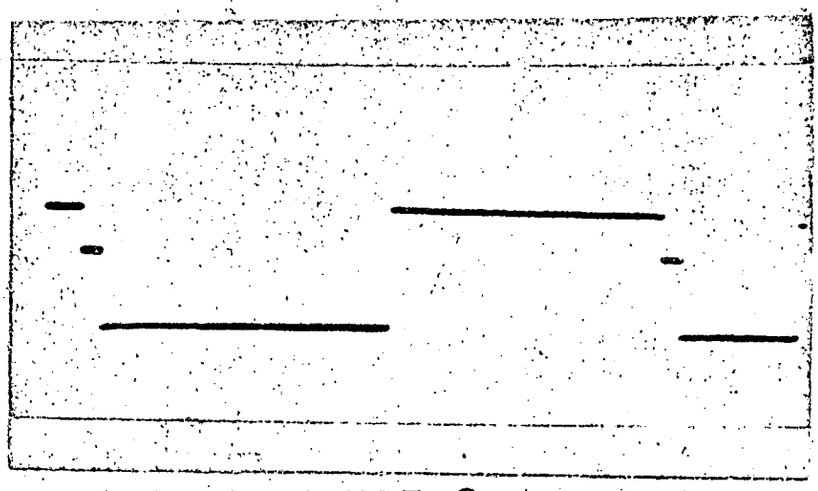

FIGURE 3-38

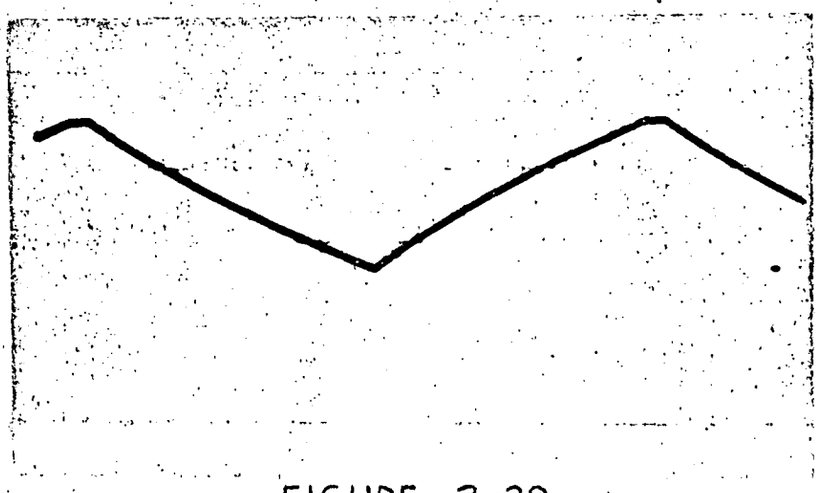

FIGURE 3-39

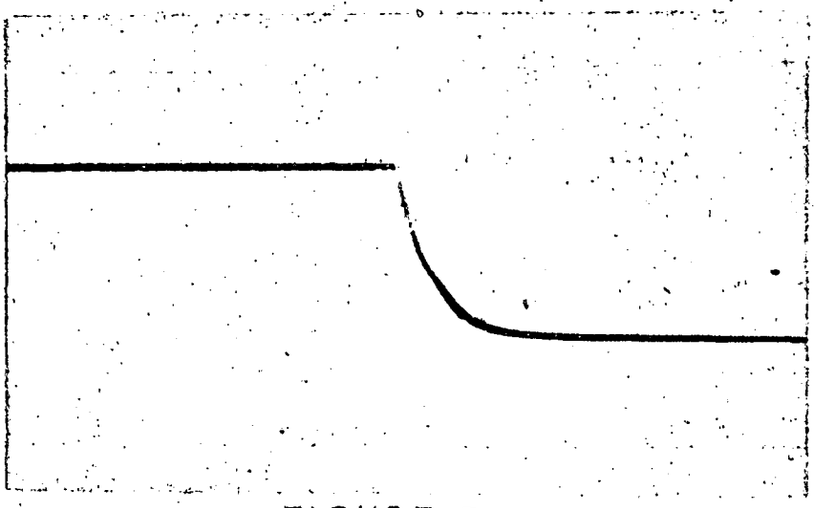

FIGURE 3-40

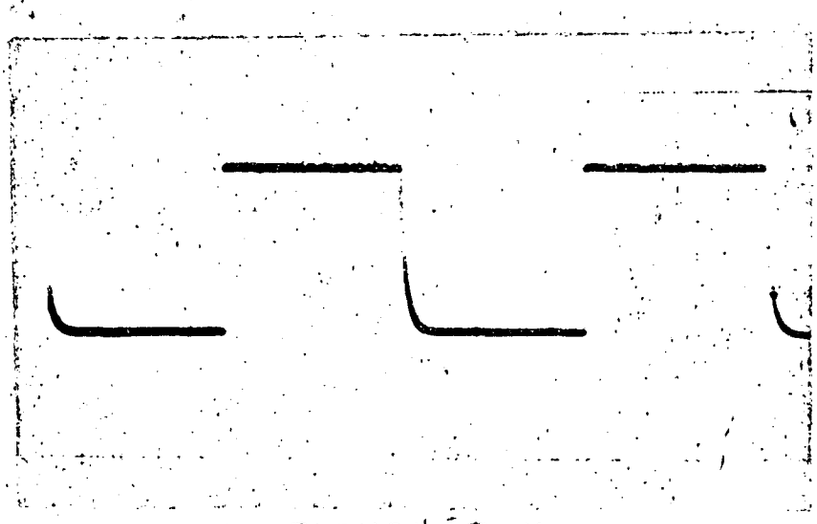

FIGURE 3-41

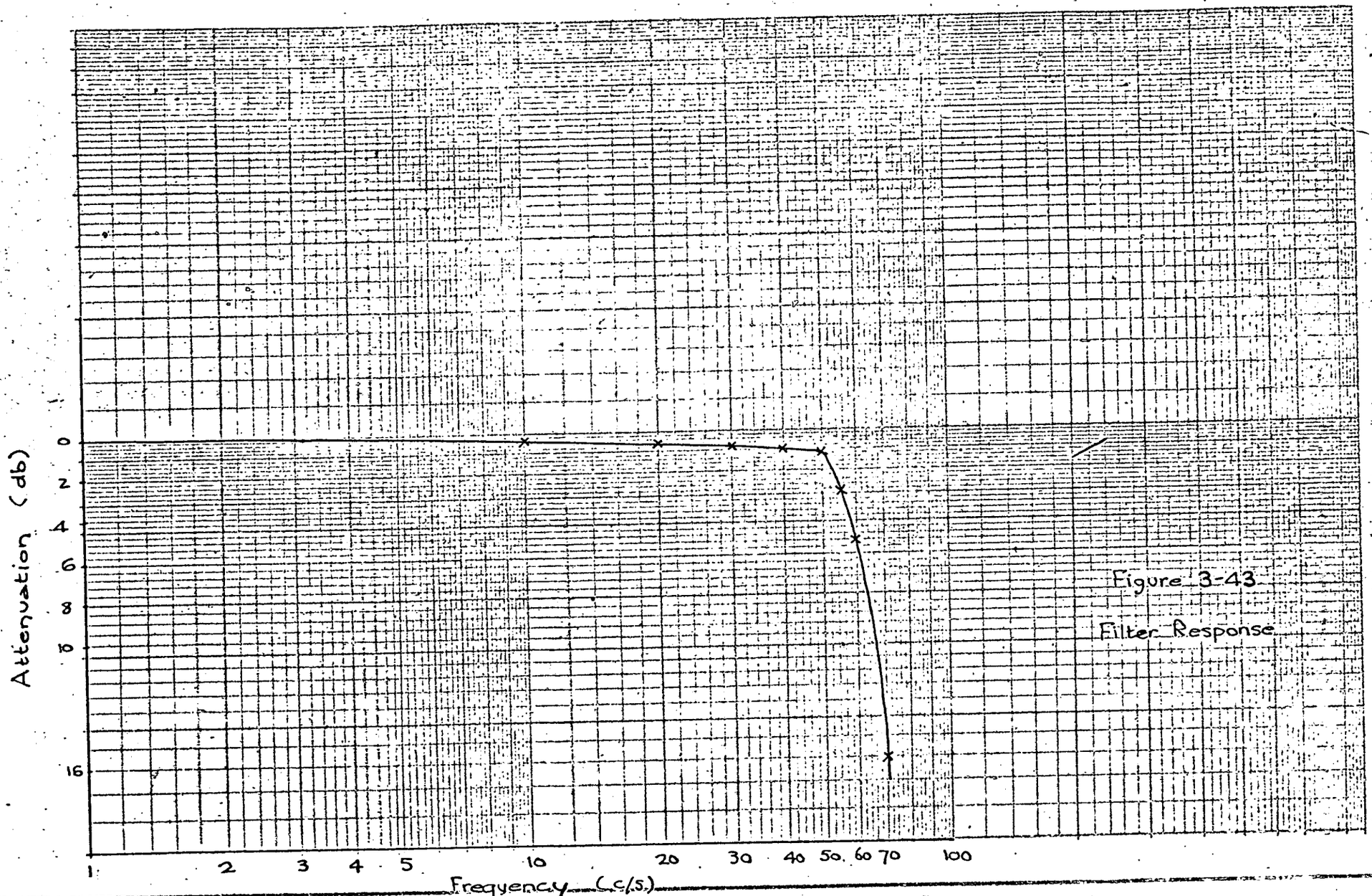

Figure 3-43

Filter Response

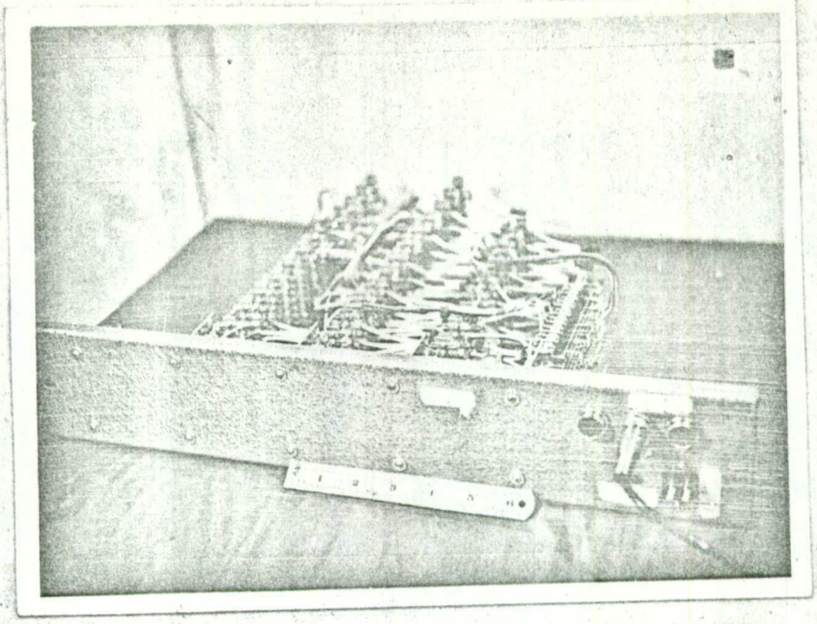

FIGURE 3-44

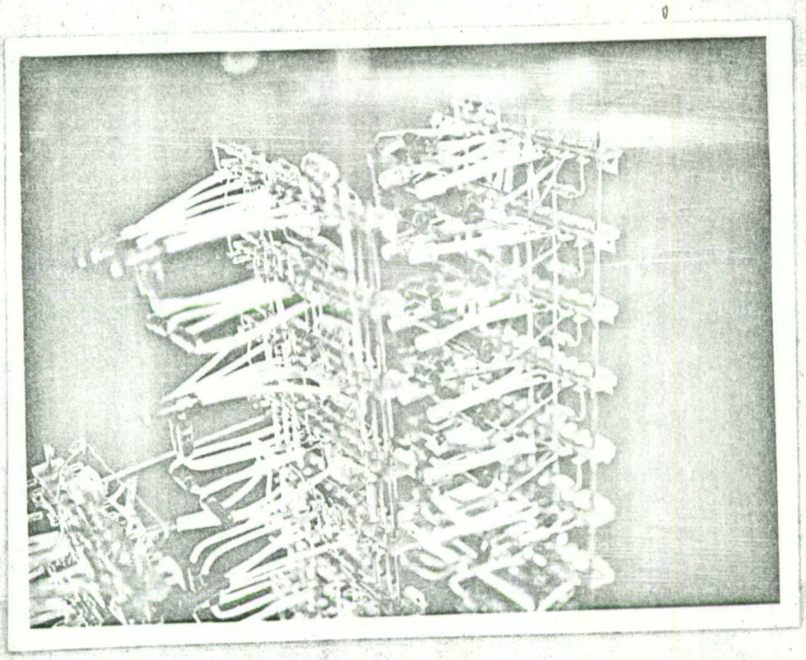

FIGURE 3-45

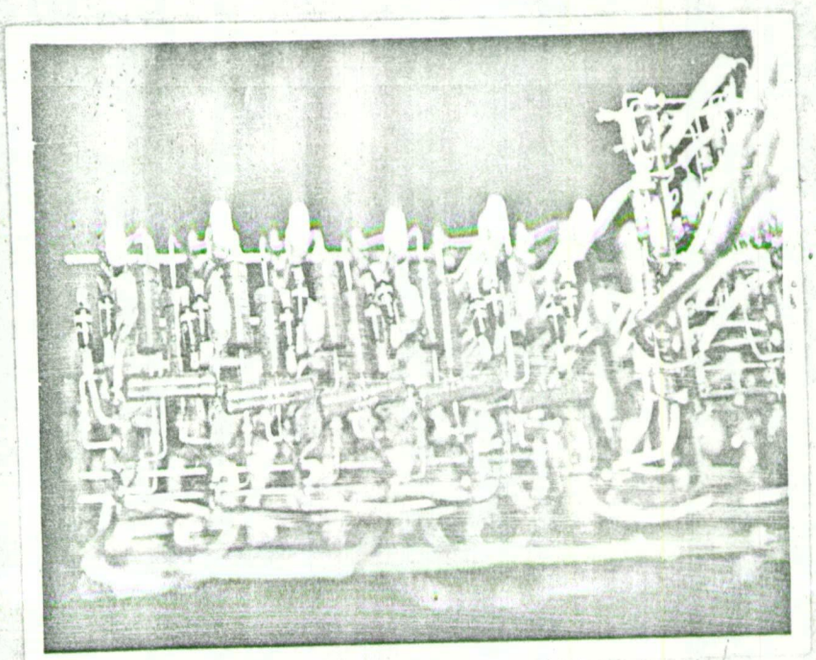

FIGURE 3-46

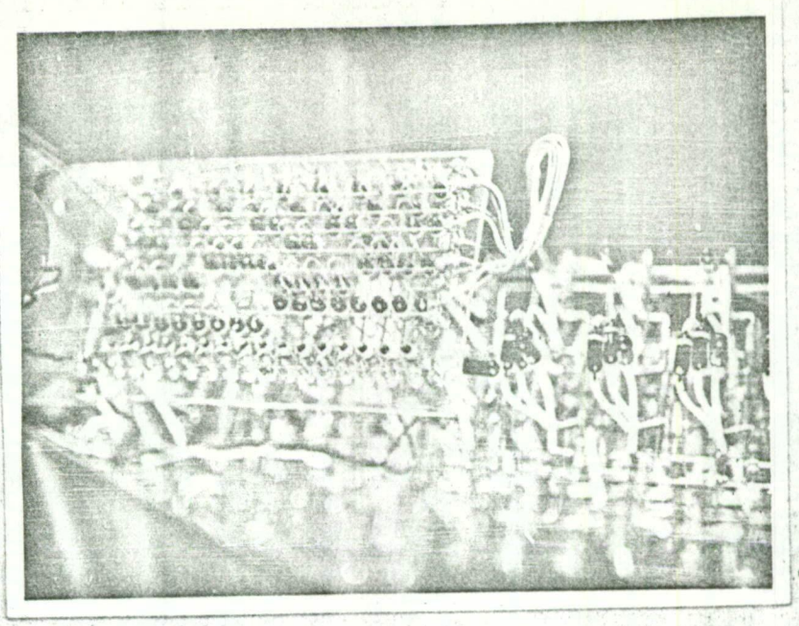

FIGURE 3-47

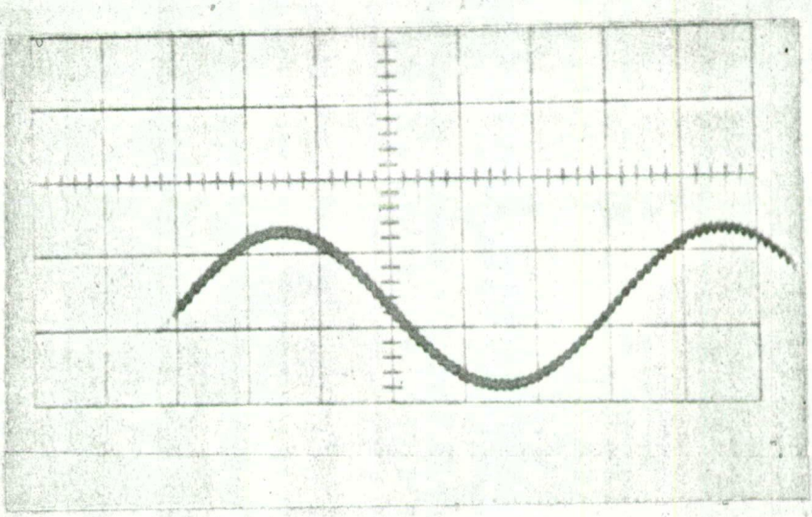

FIGURE 3-48

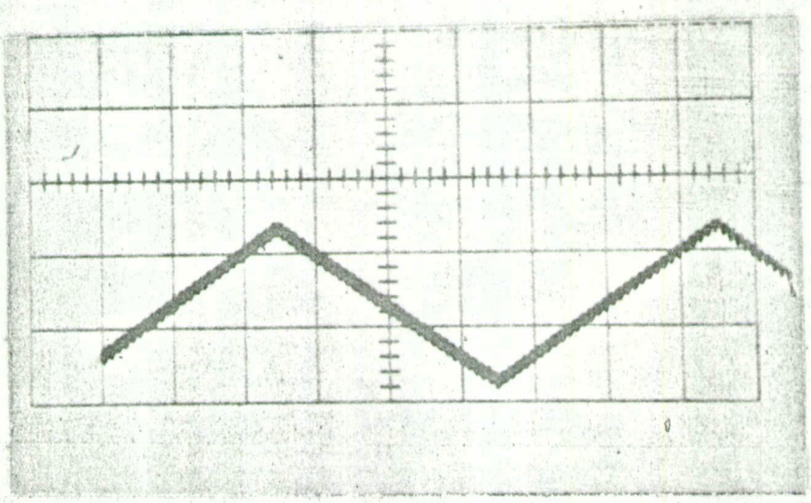

FIGURE 3-49

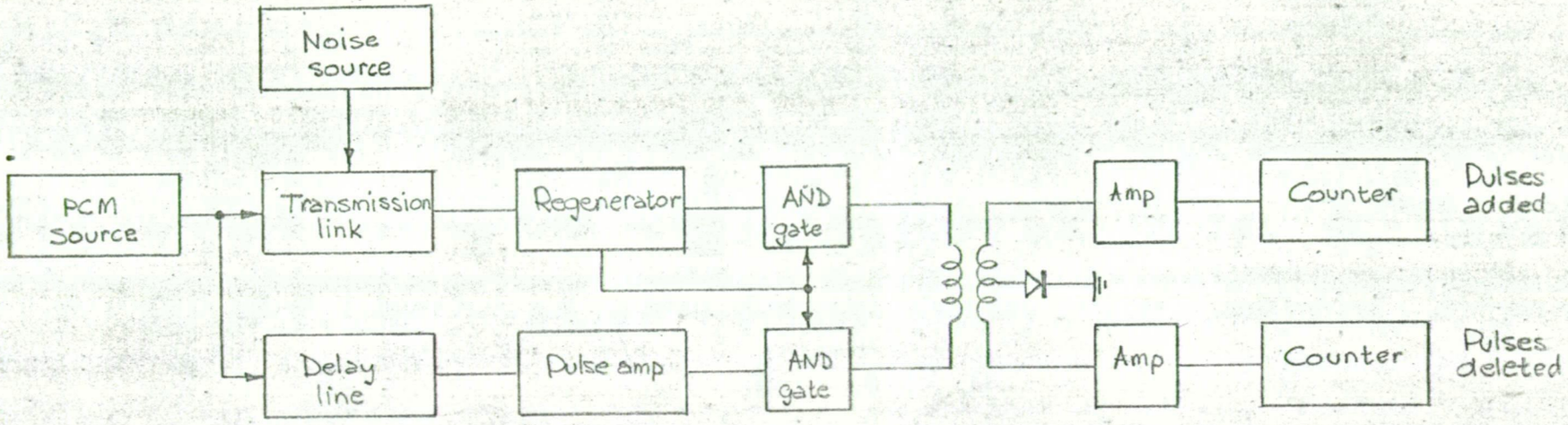
Noise source
PCM Source
Transmission link
Regenerator
AND gate
Amp
Counter
Pulses added
Delay line
Pulse amp
AND gate
Amp
Counter
Pulses deleted

FIGURE 3-50

4. SAMPLING PHENOMENA

The result of failing to sample a signal at a sufficient rate has been illustrated in Section 1.3. Overlapping of the sidebands in the sampled signal occurs, and the demodulation filter cannot separate the spurious components which have been introduced into its bandwidth.

The nature of these components will be investigated both theoretically and experimentally by letting the input signal bandwidth exceed half the sampling rate.

4.1 The spurious frequencies

Let the input signal be a sinusoid of frequency f c/s: $f(t) = A \sin 2\pi ft$, and let the sampling rate be f_c per sec. Then the nth sample, taken at $t_n = \frac{n}{fc}$, will be $f(t_n) = A \sin \left(2\pi n \frac{f}{fc} + \theta\right)$.

Letting f be greater than $\frac{1}{2}$ fc, write

$$f = mf_c \pm f^1$$

where m is an integer and $f^1 < \frac{1}{2} fc$.

Making this substitution, the sample is

$$f(t_n) = A \sin \left\{ 2\pi n \left(\frac{mfc \pm f^1}{fc}\right) + \theta^1 \right\}$$

$$= A \sin \left\{ 2\pi n\, m \pm 2\pi n \frac{f^1}{f_c} + \theta^1 \right\}$$

$$= A \sin \left(\pm 2\pi n \frac{f^1}{fc} + \theta^1 \right) \text{ for all } n .$$

This sample is the same as would be obtained from a properly bandlimited signal of frequency f^1. Thus every input frequency f, greater than $\frac{1}{2}$ fc, contributes power to the base-band zero to $\frac{1}{2}$ fc, and at a frequency $f - mf_c$, where

$$(m + \tfrac{1}{2})\, f_c > f > (m - \tfrac{1}{2})\, f_c .$$

This effect can be described as a concertina-folding of the input signal spectrum at the harmonics of the sampling frequency, and this is illustrated in Figure 4.1.

4.2 Evidence of the Spurious Frequencies

As a general result of the foldback effect, all harmonically-related frequencies give rise to a line-spectrum set in the band zero to $\frac{f_c}{2}$. If the input has only an harmonic line spectrum itself - as will any repetitive waveform - the foldback spectrum can be made into sets of harmonic line spectra by making the input frequencies lie one to each "fold", that is, one to each band $f_c\ (m \pm \frac{1}{2})$, as far as possible. It is not possible to put only one in every such band because there exists an m, however large, for which an input harmonic and the corresponding mf_c differ by more than $\frac{1}{2}f_c$. When this occurs, one harmonic set is complete and another starts, and unless the above difference is exactly $\frac{1}{2}f_c$ the new set is not related to the previous one. If the input fundamental frequency f is situated in the first fold, that is, $f = f_c \pm f'$, where $f' < \frac{1}{2}f_c$, then the set of the first $\frac{f_c}{2f}$, harmonics folds back as the first set and has the same shape of amplitude distribution as the input. The set of the next $\frac{f_c}{2f}$, harmonics also folds back, but has a reversed amplitude distribution. Subsequent sets behave alternately as the first two, until eventually the remaining harmonics contain negligible power. If the first set can be given sufficient harmonics to contain most of the power of the input signal (by making $f' \to 0$, for example) this set forms a good replica of the input with a fundamental of f', and it can be separated from the input and sampling signals simply by the $\frac{1}{2}f_c$ lowpass filter. That good replicas of several useful waveforms can be generated in this way is shown by a novel analysis in Appendix C. This technique therefore provides a simple way of separating and observing the spurious components caused by too low a sampling rate.

It is interesting to note that as the input fundamental frequency is decreased through f_c, the replica fundamental frequency passes from positive through zero to negative values. If the input is an odd function of time the replica, being likewise odd, must change sign as its frequency passes through zero. This follows because an odd function has a Fourier expansion of the form: $A_n \sin 2\pi nft$, and its replica is consequently of the

form: $B_n \sin 2\pi nf't$, each term of which changes sign with f'. On the other hand, an even function gives as a replica a series in $\cos 2\pi nf't$, which does not change sign with f'.

An experimental investigation of the foldback effect was made by applying to the modulator input signals with repetition rates close to the sampling frequency, and observing the filtered output from the demodulator. Although the experiment required only a sampler and a filter the intervening analogue-to-digital and digital-to-analogue conversions were retained because they did not affect the result and the existing equipment could beused with little modification. The only change made was to the output filter which was given a cutoff just below the minimum input frequency so that it would have little influence on the foldback signals.

The odd-function signal used was a sawtooth wave, and the even-function was a triangular wave; these two are analysed in Appendix C. Figures 4.2 and 4.3 show the replica waveform resulting from the sawtooth when the input frequency is above and below the sampling frequency, respectively, while Figure 4.4 shows the replica obtained from the triangular wave in either case. The shape of the waveform is easily recognizable despite the presence of only a few harmonics and of considerable mains-frequency pickup. The triangular replica is particularly good because about 90% of its amplitude is first harmonic. The predicted reversal of the sawtooth slope is quite obvious in Figures 4.2 and 4.3.

The results of the experiment are taken as satisfactory verification of the foldback effect theory developed in Section 4.1. A graphical method for constructing replicas is given in Appendix C. The sawtooth and triangular waves are drawn as examples, and similarity between these and the experimental results is very distinct. This provides proof of a satisfactory experimental technique.

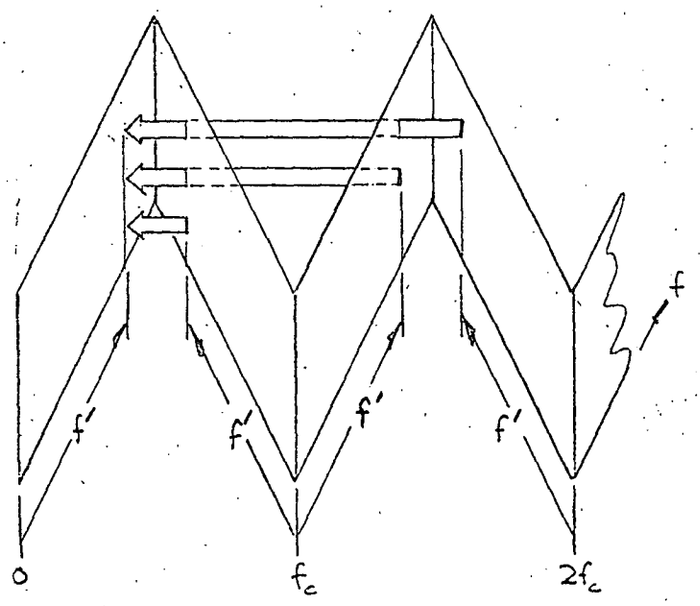

FIGURE 4-1

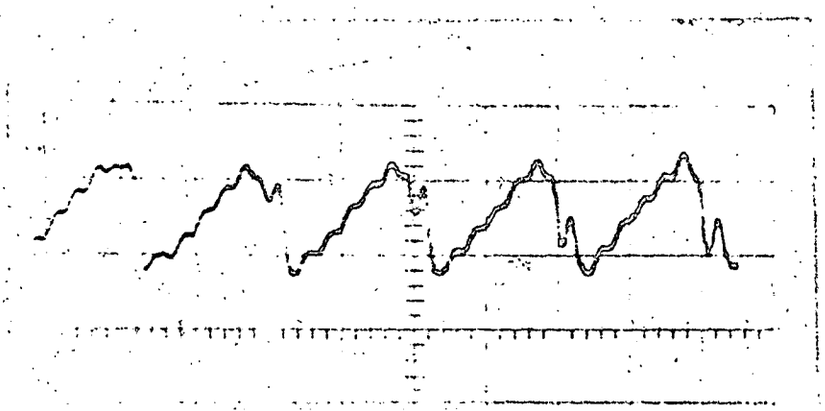

FIGURE 4-2

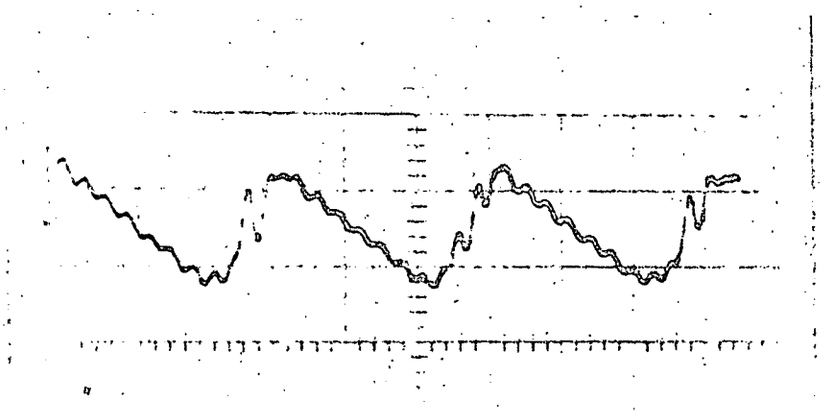

FIGURE 4-3

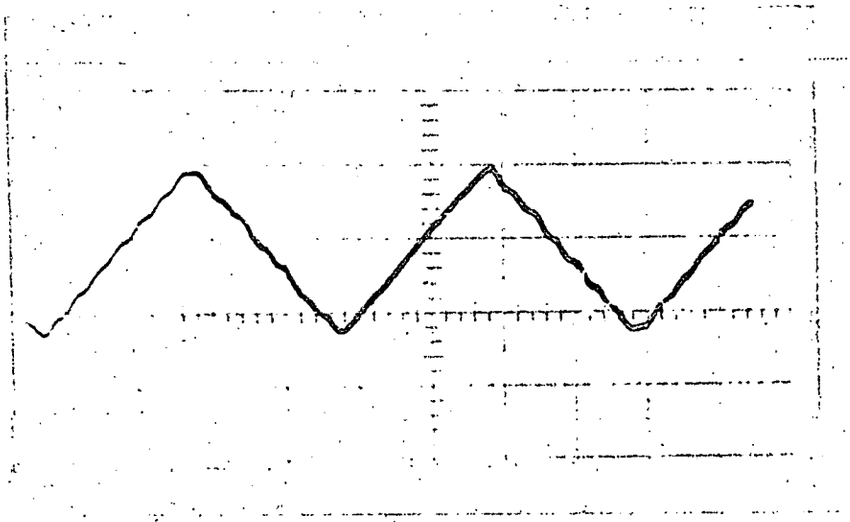

FIGURE 4-4

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APPENDIX A

Theorem 1

A signal f(t) bandlimited to B c/s is uniquely specified by amplitude samples taken every $\frac{1}{2B}$ seconds.

Proof

Let the transform of f(t) be $F(p) = \int_{-\infty}^{\infty} f(t)e^{-pt}dt$.

Then although F(p) = 0 for $|w| > 2\pi B$ because f(t) is bandlimited, it can be made arbitrarily periodic with period $4\pi B$ and expanded in a Fourier series of this period if its use is always restricted to the interval $|w| \leq 2\pi B$.

Hence
$$F(p) = \frac{1}{4\pi B} \sum_{-\infty}^{\infty} c_n e^{j2\pi n \frac{w}{4\pi B}} \qquad \ldots 1)$$
$$= \frac{1}{4\pi B} \sum_{-\infty}^{\infty} c_n e^{j \frac{n}{2B} w} \quad \text{for } |w| < 2\pi B,$$
and
$$= 0 \qquad \text{for } |w| > 2\pi B,$$

where the c_n are defined by
$$c_n = \int_{-2\pi B}^{2\pi B} F(p) e^{-j\frac{n}{2B}w} \, dw \qquad \ldots 2)$$

But, by definition of F(p),
$$f(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} F(p) e^{pt} dw$$
$$= \frac{1}{2\pi} \int_{-\infty}^{\infty} F(p) e^{pt} dw, \qquad \ldots 3)$$

so that at the particular time
$$t = -\frac{n}{2B},$$
$$f\left(\frac{-n}{2B}\right) = \frac{1}{2\pi} \int_{-2\pi B}^{2\pi B} F(p) e^{-j\frac{n}{2B}w} \, dw$$
$$= \frac{c_n}{2\pi} \text{ from 2).} \qquad \ldots 4)$$

Thus the expansion coefficients of F(p) may be obtained from amplitude samples taken every $\frac{1}{2B}$ seconds. Then, since equation 3) defines f(t) in terms of F(p), it also defines f(t) by these 2B samples per second. This completes the proof.

If the substitution for c_n is made in equation 1),
$$F(p) = \frac{1}{4\pi B} \sum_{-\infty}^{\infty} 2\pi f\left(-\frac{n}{2B}\right) e^{j \frac{n}{2B} w}$$
$$\text{for } |w| < 2\pi B \qquad \ldots 5)$$

Therefore from equation 3),
$$f(t) = \frac{1}{4\pi B} \int_{-2\pi B}^{2\pi B} \sum_{-\infty}^{\infty} f\left(-\frac{n}{2B}\right) e^{jw\left(t+\frac{n}{2B}\right)} dw \ldots 6)$$
$$= \frac{1}{4\pi B} \sum_{-\infty}^{\infty} f\left(-\frac{n}{2B}\right) \int_{-2\pi B}^{2\pi B} e^{jw\left(t+\frac{n}{2B}\right)} dw,$$

since the integral must be finite, and $f\left(-\frac{n}{2B}\right) \to 0$ as $n \to \infty$

for a real signal. Therefore,

$$f(t) = \sum_{n=-\infty}^{\infty} f(-\frac{n}{2B}) \frac{\sin 2\pi B(t + \frac{n}{2B})}{2\pi B (t + \frac{n}{2B})} \quad \ldots 7)$$

This shows that at any instant f(t) is made up of the sum of all samples weighted by a factor centred on the time of taking that sample.

Theorem 2

A lowpass filter is sufficient to reconstruct f(t) from amplitude samples taken at a uniform rate of 2B per second if f(t) has been bandlimited to B c/s before being sampled.

Proof

The samples $f(\frac{n}{2B})$ may be either constant-amplitude pulses of width τ seconds, or impulses of amplitude $\tau f(\frac{n}{2B})$, because the Fourier transform of either is

$F(jw) = f(\frac{n}{2B})\tau e^{-jwt_1}$, where t_1 is the time of occurrence of the pulse. ...8)

The response of an ideal lowpass filter of bandwidth B, unity gain, and linear phase-shift is

$$\left.\begin{aligned} G(jw) &= 1.e^{-jwt_o} \quad \text{for } |w| \leq 2\pi B \\ &= 0 \quad \text{for } |w| > 2\pi B \end{aligned}\right\} \quad \ldots 9)$$

Hence the output of such a filter in response to the input pulse is

$$\begin{aligned} g(t) &= \frac{1}{2\pi} \int_{-\infty}^{\infty} F(jw)G(jw)e^{jwt}dw \\ &= \frac{1}{2\pi} \int_{-2\pi B}^{2\pi B} f(\frac{n}{2B})\tau e^{-jw(t - t_o)}dw \\ &= 2Bf(\frac{n}{2B})\tau \frac{\sin 2\pi B\{t - (t_o + t_1)\}}{2\pi B\{t - (t_o + t_1)\}}, \end{aligned} \quad \ldots 10)$$

which, by comparison with equation 7), shows that the lowpass filter applies the desired weighting factor to the pulse.

Now this factor is unity for $t = (t_o + t_1)$, and zero for $t = (t_o + t_1) + \frac{m}{2B}$, where $m = \pm 1, \pm 2, \pm 3, \ldots\ldots$ Therefore, if other pulses are applied at intervals of $\frac{1}{2B}$ they will not interact because at the instant of application the weighting factors for all other pulses are zero, while the factor for the applied pulse is unity. For such a pulse train, the filter output at any instant is simply the superposition of all the outputs given by equation 10),

$$g(t) = \sum_{}^{\infty} 2B\tau f(\frac{n}{2B}) \frac{\sin 2\pi B(t - \frac{n}{2B})}{} \quad \ldots 11)$$

Hence, from equation 7),

$$g(t) = 2B\tau\, f(t).$$

A lowpass filter is therefore sufficient to reconstruct $f(t)$ from the sample pulses.

APPENDIX B

BISTABLE MULTIVIBRATOR DESIGN

B.1 D-C DESIGN

The basic bistable multivibrator, or flipflop, is shown in Figure B-1. It comprises two common-emitter amplifiers connected in a positive feedback loop to produce two stable states: the left-hand transistor fully conducting and the right-hand transistor cut off, and vice versa.

A d-c design is satisfactory if these two states are maintained despite component tolerances and temperature variation, and the following analysis is made to determine whether a solution is possible. The conducting and non-conducting states are considered separately to find a range of values for the base resistors which satisfies both requirements.

ON condition: In Figure B-2(a), which shows the drive requirements of the saturated transistor,

$$I_B = \frac{V_{cc} - V_{B\,on}}{R_L + R_D} - \frac{V_{BB} + V_{B\,on}}{R_B} \quad \text{.....1)}$$

(neglects I_{co} from OFF collector)

From Figure B-2(b) the collector current may be found as

$$I_c = \frac{V_{cc} - V_{CES}}{R_L} - \frac{V_{BB} + V_{CES}}{R_B + R_D}$$

(neglects I_{cBo} into OFF base)

$$\doteq \frac{V_{cc} - V_{CES}}{R_L}, \quad \text{...2)}$$

to be justified later.

Now the base current which will saturate all transistors is $\frac{I_c}{h_{FE\,min}}$; therefore, for guaranteed saturation, $I_B \geqslant \frac{I_c}{h_{FE\,min}}$,

that is, from 1), 2), $\frac{V_{cc} - V_{B\,on}}{R_L + R_D} - \frac{V_{BB} + V_{B\,on}}{R_B} \geqslant \frac{V_{cc} - V_{CES}}{R_L\, h_{FE\,min}}$

therefore, $$R_B \geqslant \frac{V_{BB} + V_{B\,on}}{\frac{V_{cc} - V_{B\,on}}{R_L + R_D} - \frac{V_{cc} - V_{CES}}{R_L h_{FE\,min}}} \quad \text{...3)}$$

OFF condition: Figure B-3 shows the base conditions for the nonconducting transistor.

$$I_{B\,off} = \frac{V_{BB} - V_{B\,off}}{R_B} - \frac{V_{B\,off} + V_{CES}}{R_D} \quad \ldots\ldots 4)$$

To ensure cutoff $I_{B\,off}$ must be $\geqslant I_{cBo\,max}$ at the highest temperature of operation. Therefore,

$$I_{cBo} \leqslant \frac{V_{BB} - V_{B\,off}}{R_B} - \frac{V_{B\,off} + V_{CES}}{R_D}$$

that is,

$$R_B \leqslant \frac{R_D\,(V_{BB} - V_{B\,off})}{R_D\,I_{cBo\,max} + V_{B\,off} \mp V_{CES}} \quad \ldots\ldots 5)$$

Equations 3) and 5) define permissible values of R_B and R_D for chosen values of supply voltages and transistor characteristics. If R_B is plotted as a function of R_D for the two cases, a region should be defined in which both equations are satisfied, so that a choice can be made of a set of values for R_B and R_D.

The transistor type is OC44, for which $h_{FE\,min} = 20$ at $I_c = 5$ mA, and $I_{cBo\,max} = 100\,\mu$A at 55°C with $V_{B\,off} = 0.5$V. A typical $V_{B\,on} = 0.3$V, and $V_{CES} = 0.2$V. The supply rails are at $\pm$ 12V, which fixes the load resistor as approximately $R_L = \frac{12V}{5mA} = 2.2K\Omega$.

The resulting plots of R_B as a function of R_D are given in Figure B-4. The set of values, $R_D = 12K\Omega$, $R_B = 47K\Omega$, is chosen in the centre of the large regionof permissible solutions in order to ensure high reliability, in the face of adverse component and voltage tolerances. A more economical solution is obtained towards the top of the region, but at the expense of reliability and switching speed. It is now necessary to check the assumption made in the simplification of equation 2). Substituting,

$$\frac{V_{cc} - V_{CES}}{R_L} = 5.37 \text{ mA},$$

which is much greater than

$$\frac{V_{BB} + V_{CES}}{R_B + R_D} = 0.21 \text{ mA},$$

so that the assumption is justified to sufficient accuracy for this analysis.

B.2 Transient Analysis

By use of capacitors across the base drive resistors in Figure B-1 it is possible to improve the switching-time of the flipflop. The drive circuit is then analogous to the phase-advance network in a

linear amplifier, although it is better considered as a transient overdrive source for the base. The switching-time improvement follows a law of diminishing return as the capacitors are increased, and the maximum triggering rate also decreases.

In Figure B-6 consider the instant at which transistor T1 is switched on. The capacitor C_D must discharge through the parallel paths of R_D and $R_B + R_{sat}$ where R_{sat} is the saturated collector resistance of T1. This time-constant is therefore

$$t_1 = \frac{C_D R_D (R_B + R_{sat})}{R_D + R_B + R_{sat}} .$$

Now consider the instant at which T1 is switched off. The charging paths for C_D are now through R_D and through R_L in series with the parallel paths R_B and r_{in}, where r_{in} is the common emitter input impedance of T1. This time-constant is therefore

$$t_2 = \frac{C_D R_D \left(R_L + \frac{r_{in} R_B}{r_{in}+R_B}\right)}{R_D + R_L + \frac{r_{in} R_B}{r_{in}+R_B}} .$$

In this design, $t_1 > t_2$, so that the maximum triggering frequency is of the order of

$$f_{max} \doteq \frac{R_D + R_B}{C_D R_D R_B}$$

$$= \frac{(12+47) \times 10^3}{12 \times 47 \times 10^6 \times 1.2 \times 10^{-9}} \text{ c/s}$$

$$= 80 \text{ Kc/s},$$

which is certainly satisfactory in this application.

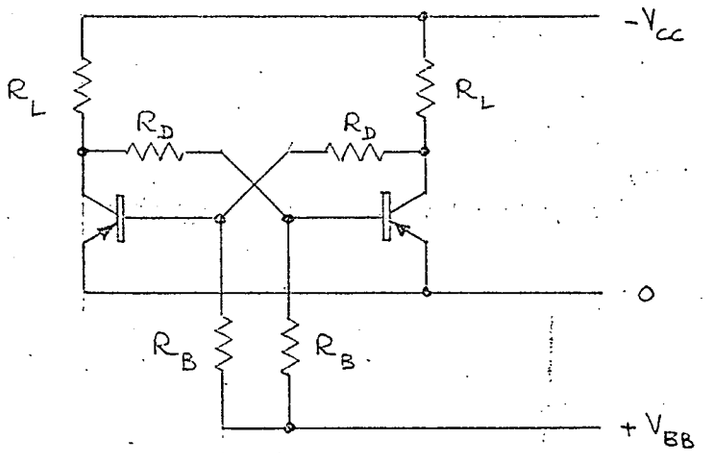
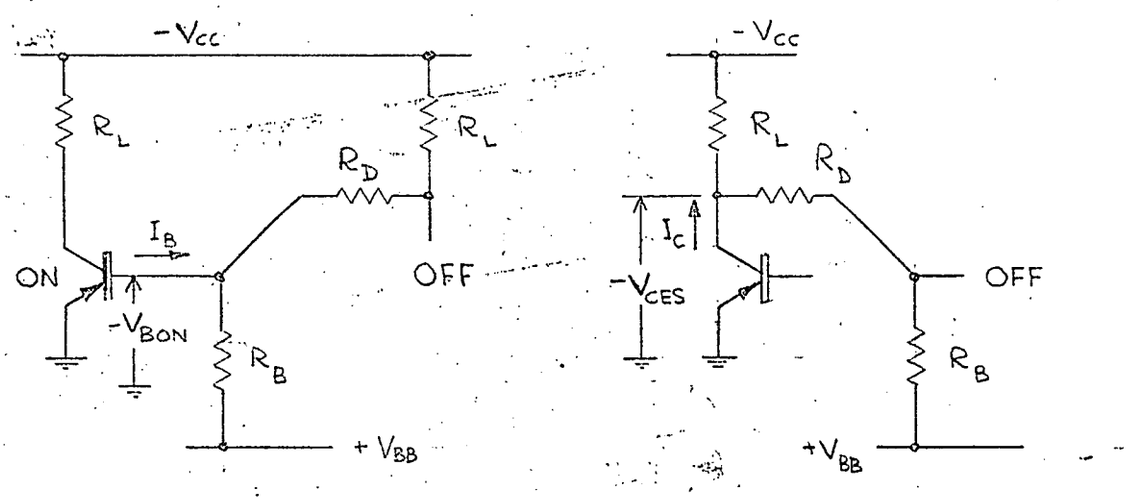


FIGURE B-1



(a) FIGURE B-2 (b)

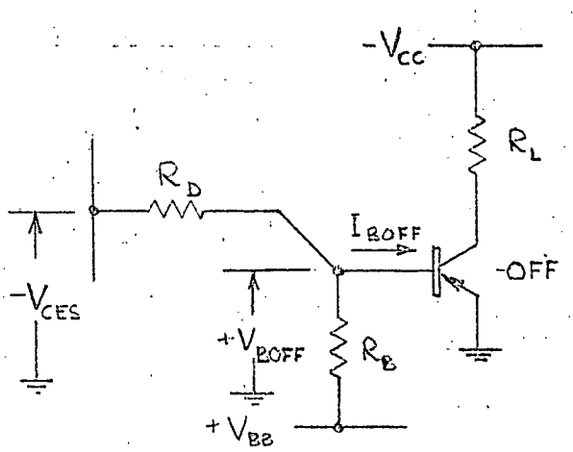


FIGURE B-3

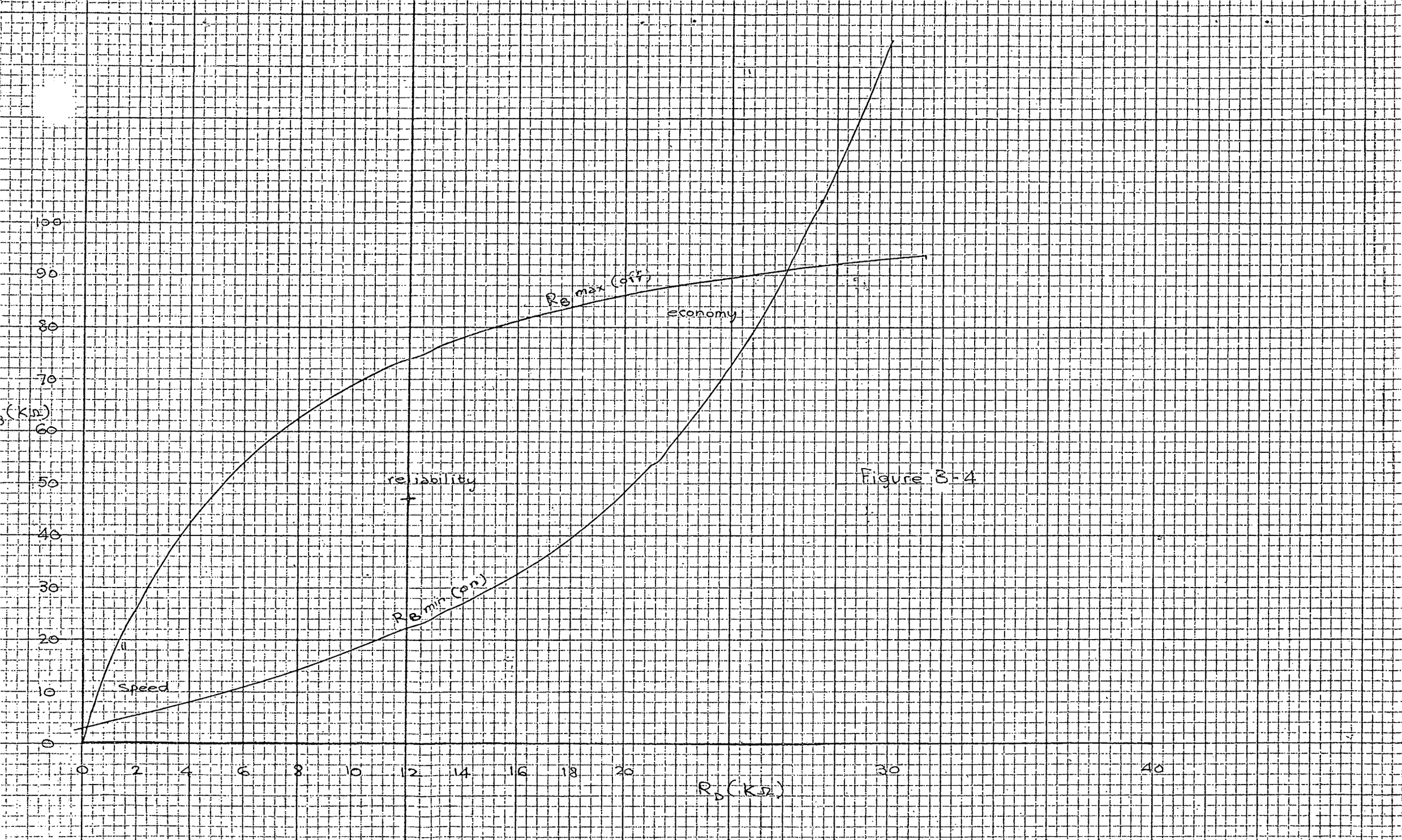

100
90
80
70
60
50
40
30
20
10
0
(KΩ)
0
2
4
6
8
10
12
14
16
18
20
30
40
R_D(KΩ)
R_B max (off)
economy
reliability
R_B min (on)
Speed

Figure 3-4

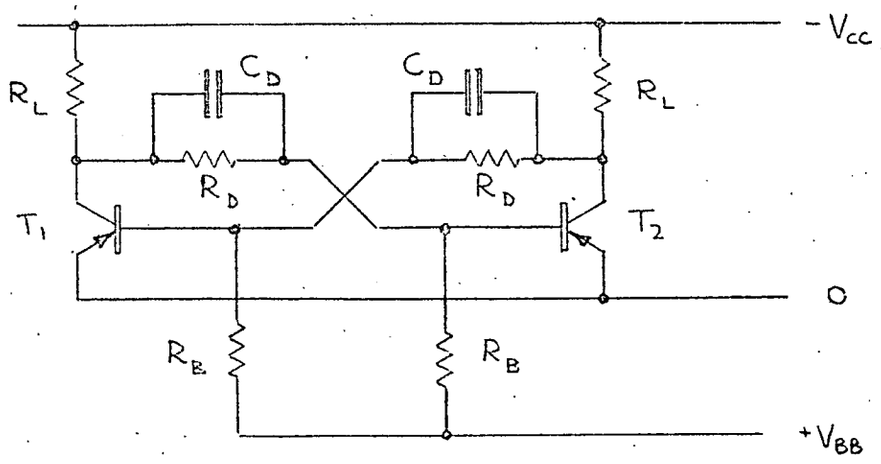


FIGURE B-5

APPENDIX C

Construction of replica waveforms from harmonic sets derived by foldback can be performed graphically.

In this analysis f' is chosen for convenience so that the harmonic sets coincide and so that only a few harmonics are formed. To maintain close relation with the experimental results, twelve harmonics are used by putting $\frac{f_c}{2f'} = 12.5$, corresponding to $f_c = 62.5$ c/s and $f = 65$ c/s.

The two waveforms constructed are a sawtooth and a triangular wave, whose Fourier series expansions are:-

sawtooth: $$y_1 = \frac{2E}{\pi} \sum_{n=1}^{\infty} \frac{(-1)}{n} \sin n\theta$$

triangle: $$y_2 = \frac{8E}{\pi^2} \sum_{n=1}^{\infty} \frac{1}{n^2} \cos n\theta$$

Table C.1 shows the method of performing the construction of the replica, and its explanation is as follows:

Line 1: The frequencies of the first 12 harmonics of f.

Line 2: The corresponding values of f' found from $f' = f - nf_c < \frac{1}{2}f_c$. Because of the choice of $\frac{f_c}{2f'} = 12.5$ there are only 12 possible values.

Line 3: The coefficients of the appropriate harmonics in the Fourier series for y_1 (say), written from left to right.

Line 4: The coefficients of the next 12 harmonics of y_1, written from right to left.

Line 5: The coefficients of the next 12 harmonics of y_1, written from left to right.

L The last two steps are repeated until the coefficients becomes sufficiently small compared with unity. Lines 3, 4 and 5 are the coefficients of the first three harmonics sets folded back.

Line 6: The sum of the coefficients for each harmonic of f'. These are the coefficients of the harmonic expansion of the replica.

Line 7: The Fourier coefficients of the first 12 harmonics of f, for comparison with Line 6.

A graphical construction is then used to draw the replica function from the coefficients in Line 6.

The two replicas constructed from the calculations in Table C.1 are given in Figures C.2 and C.3. They show that the foldback effect can generate excellent replicas from a few harmonics. The similarity to the experimental results given in Figures 4.2 and 4.4 is most marked.

nf	65	130	195	260	325	390	455	520	585	650	715	780
$f'(f_c=12.5)$	2·5	5	7·5	10	12·5	15	17·5	20	22·5	25	27·5	30
	+1·000	−·500	+·333	−·250	+·200	−·167	+·143	−·125	+·111	−·100	+·091	−·083
	+·043	−·044	+·047	−·050	+·053	−·056	+·059	−·062	+·067	−·071	+·077	
	−·042	+·040	−·038	+·037	−·036	+·034	−·033	+·032	−·031	+·030	−·029	+·028
	+1·001	−·504	+·342	−·263	+·217	−·189	+·169	−·155	+·147	−·141	+·139	−·055
	+1·000	−·500	+·333	−·250	+·200	−·167	+·143	−·125	+·111	−·100	+·091	−·083
	+·100		+·111		+·0400		+·0204		+·0134		+·0083	
	+·0019		+·0023		+·0028		+·0035		+·0045		+·0059	
	+1·002		+·113		+·043		+·024		+·018		+·014	
	+1·000		+·111		+·0400		+·0204		+·0134		+·0083	

TABLE C-1

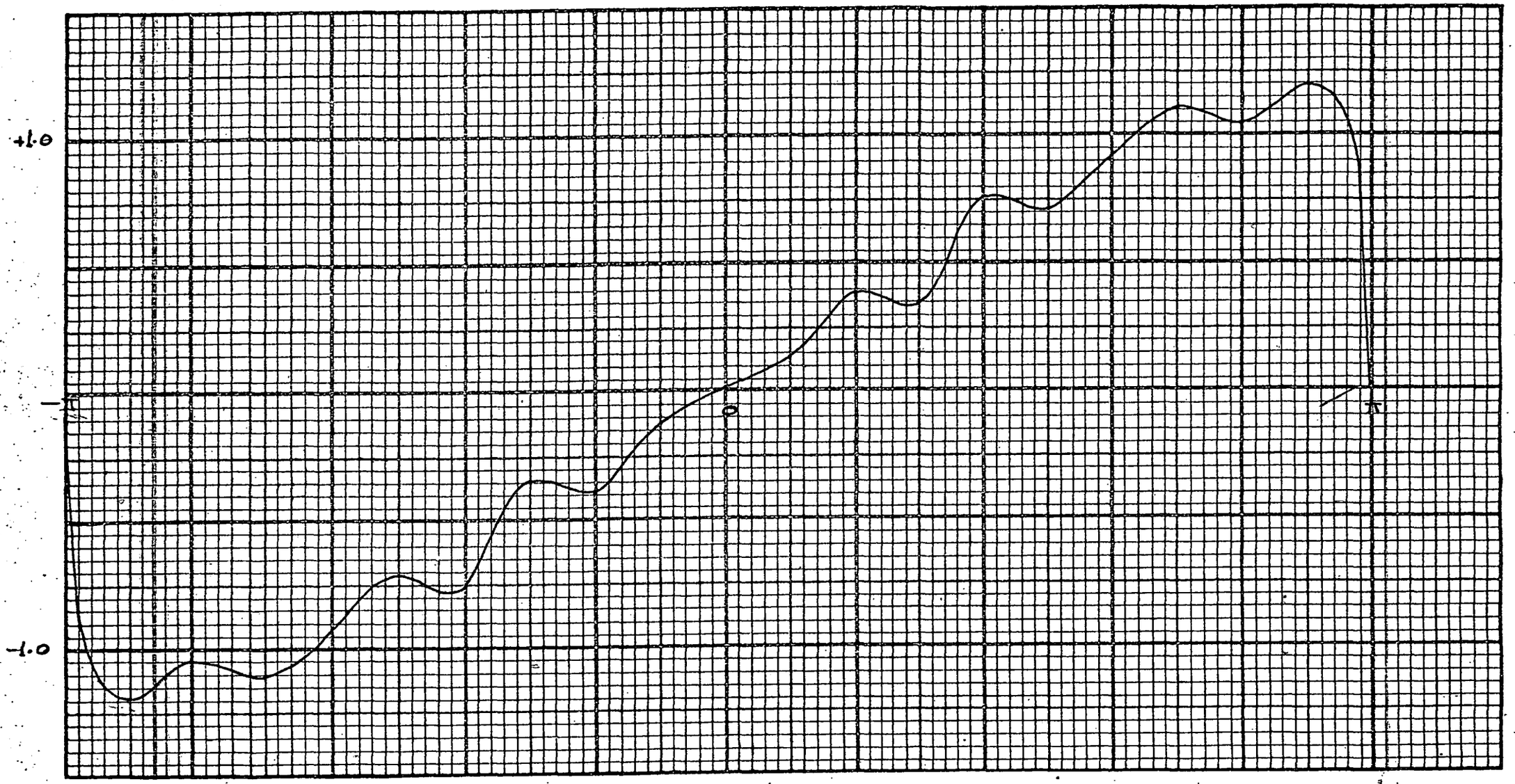


FIGURE C-2

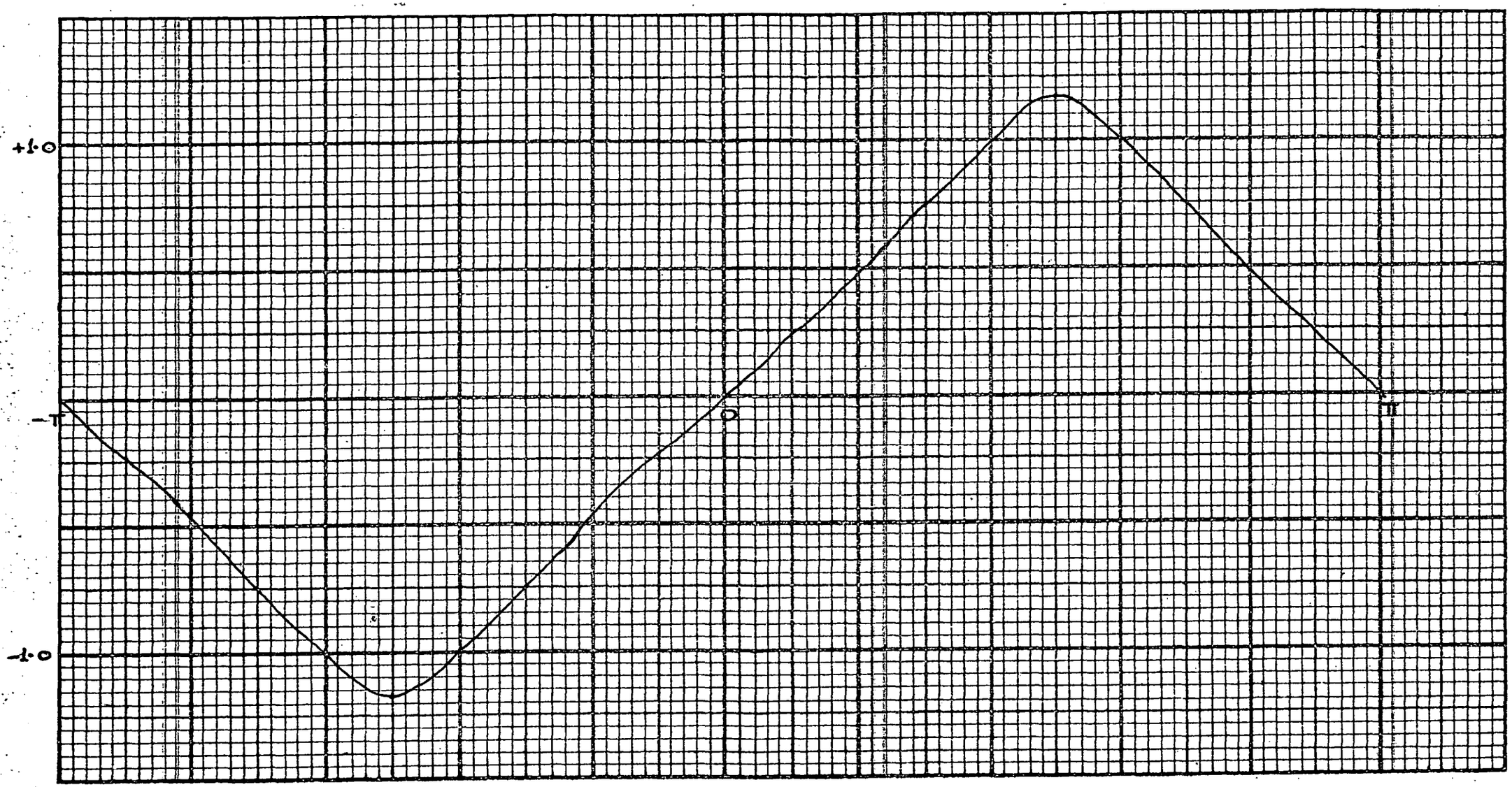


FIGURE C-3

APPENDIX D

Other Applications of Synch Detector

The modified clamp circuit described in Section 2.2.3 has several interesting applications resulting from its unusual two-level output.

Reference to Figure 2-18 shows that if the repetition rate of A is an integral multiple of that of B, then as long as the negative part of B is narrower than the positive part of A the clamp action will be the same, and the phase response will be similar, although there will be an integral number of phasings of B with respect to A which yield the same output. This response is sketched in Figure D-1 for a frequency ratio of two.

If B is considered as the synch pulse, this means that a flywheel oscillator can be synchronized to any integral multiple of the synch frequency, although the phase will be ambiguous. The significant feature is that the two detector output levels are independent of the frequency ratio.

It is also possible with this synch detector to lock an oscillator to a frequency lower than the synch frequency. If B has a repetition rate which is an integral multiple of A's, as in Figure D-2, the phase response will again be a pattern repeating every $\omega\tau_3$ where ω is the slip angular frequency. There is a further restriction that $\tau_1 < \frac{\tau_3}{n}$ in this case, so that the negative part of A can span n successive synch pulses and thereby be unaffected by all but the first. This incidentally gives the output a greater average amplitude per slip cycle, but again it can have only two possible values regardless of the frequency ratio.

Although the analysis have been given for signals with zero risetimes, this is not essential: a sinusoidal flywheel oscillator will give an approximately sinusoidal phase response with a narrow synch pulse.

The two techniques described are noteworthy for giving a flywheel control which is independent of the frequency ratio, and a phase-lock which is as tight as the waveform risetimes are short. It could be expected that, in applications of this circuit to locked-oscillator frequency dividers and multipliers, ratios as high as 100

could be easily maintained, for ratios of 20 have been achieved in very simple experiments. The only difficulty arises in first establishing the correct ratio, and this is merely a setting-up procedure. With appropriate flywheel filter and oscillator design, a frequency multiplier or divider could be constructed which would be capable of tracking a frequency modulated input.

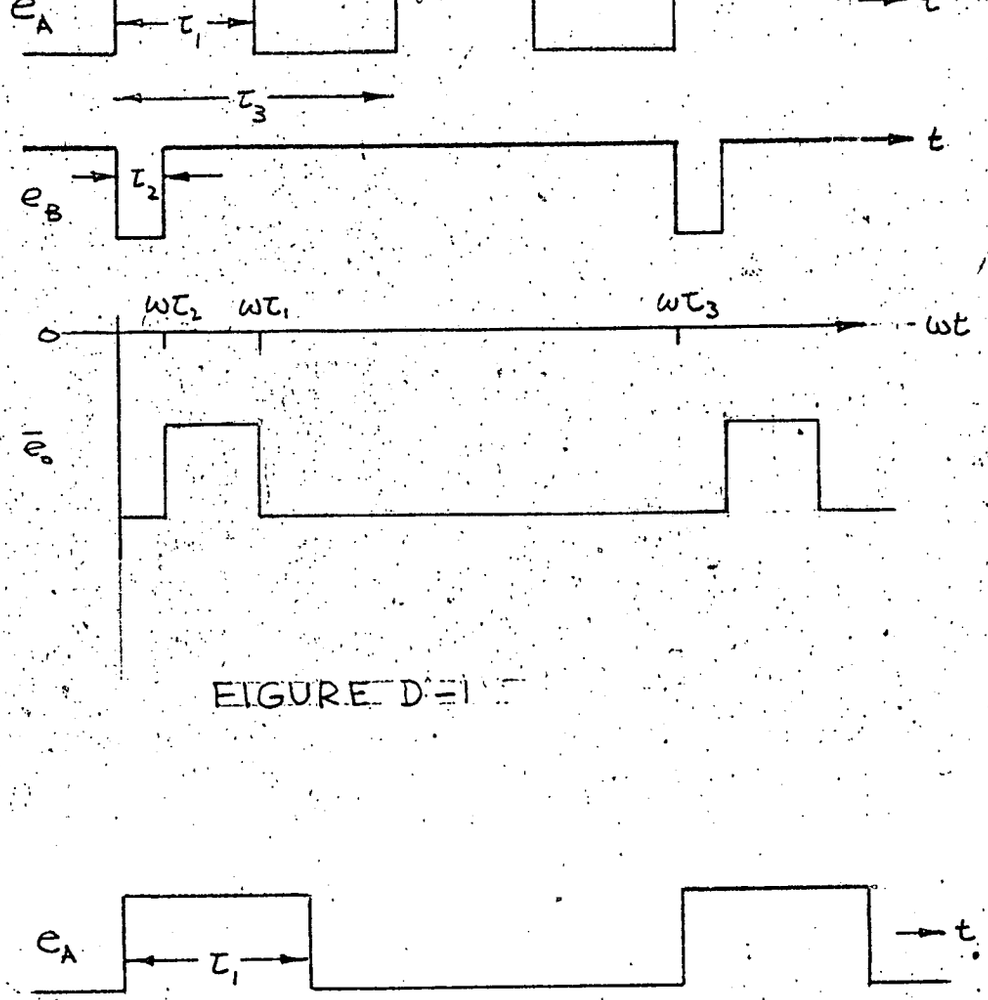


FIGURE D-1

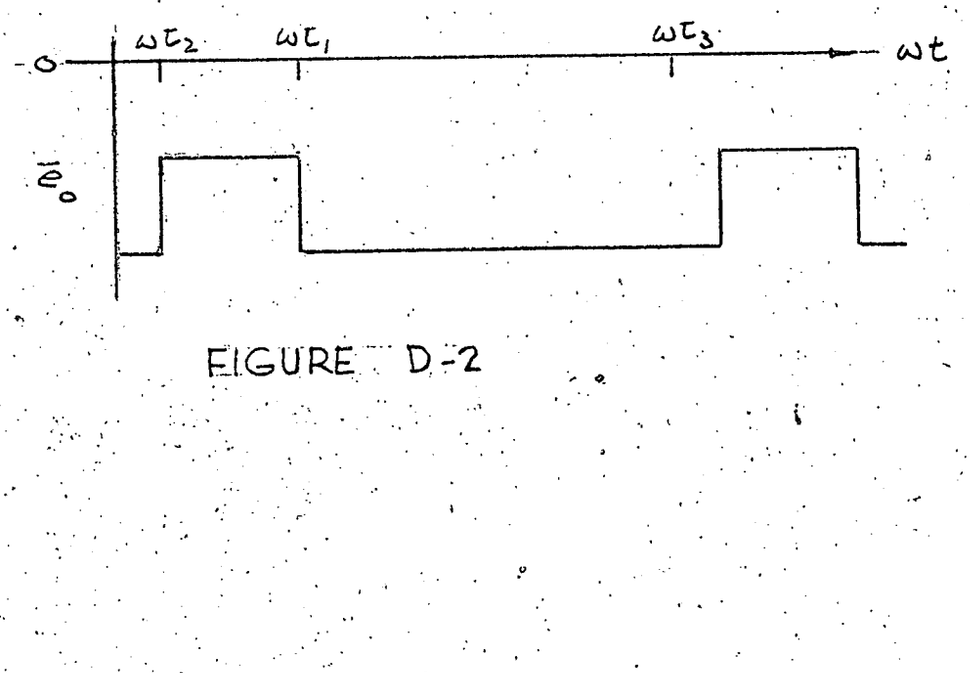


FIGURE D-2

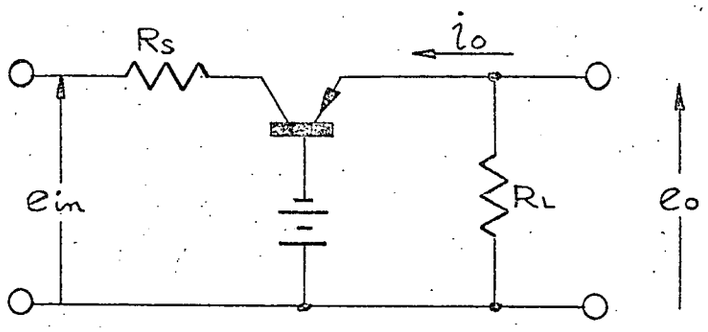


FIGURE 1 - 1

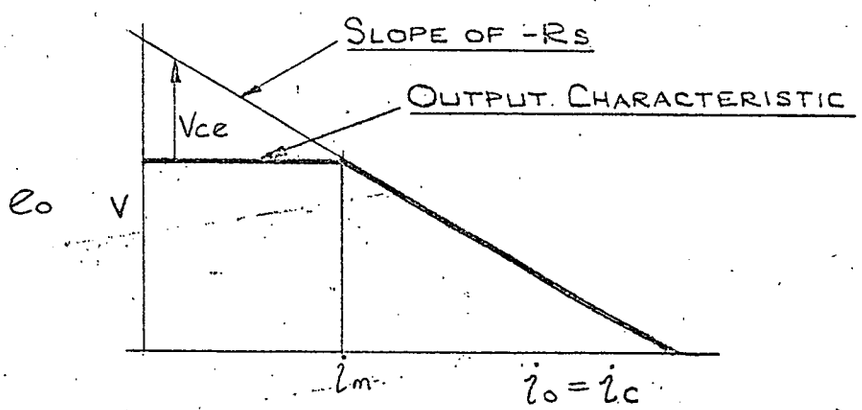


FIGURE 1 - 2

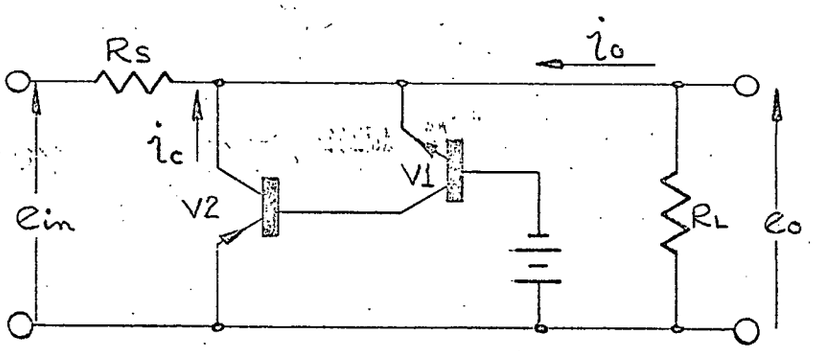


FIGURE 1-3

DIVERSE EQUIPMENT

INTRODUCTION:

Miscellaneous design tasks, undertaken to assist the instrumentation of geological research, yielded some novel circuit techniques. Pieces of such equipment are described in the following Sections.

The first Section contains a description and analysis of two improvements to low-tension high-current regulated power supplies, and gives a circuit of a general purpose unit which is protected against short-circuit faults.

In the second Section, the design of a portable unit for measuring bore-hole temperatures to better than 0.01°C is described. This unit is a modification to an earlier design using the same bridge technique but having improved circuits.

Equipment which was designed and built to provide timing signals for a seismic research laboratory is described in Section 3. This comprises a digital "clock" which marks data recordings with a ruler time-scale, and a modulator and detector which enable timing signals to be transmitted to a remote station via a telephone line which is simultaneously used for transmitting data.

1. REGULATED TRANSISTOR POWER SUPPLIES

1.1 Introduction

For equipment being developed in the laboratory it is highly desirable to have power supplies which are not damaged by being short-circuited. Fusing is not satisfactory because permanent damage can be done to semiconductors during the time taken for a series fuse to blow. The protection must therefore be built into the overload characteristics of the regulator.

The series regulator is regarded as the least lossy type for constant-voltage applications because the series transistor can operate with only a small voltage drop across it, but it becomes seriously inefficient when short-circuit protection is incorporated. The shunt regulator, on the other hand, is inherently safe under short-circuit conditions but it is lossy and this power is dissipated in the control transistor.

Only one reference to the use of a transistor shunt regulator has been found[72] but attention is directed there not to protection aspects but rather to the achievement of a high loop gain for low output impedance.

This report describes one improvement to the basic shunt regulator which reduces the maximum control element dissipation by a factor of nearly four, and another improvement which permits simple control of the output resistance of such a regulator to zero or negative values.

1.2 Series Regulator Protection

The basic series regulator shown in Figure 1-1 is an emitter follower with the load as its emitter resistance and current-limiter. When the load is short-circuited the emitter current is limited only by the resistance of the unregulated source, and the voltage across the series element is equal to the unregulated voltage at that current. The simultaneous

states of high collector current and high collector-emitter voltage (and therefore the condition of high dissipation) can therefore be avoided by inclusion of a resistance R_s to pad the output resistance of the unregulated supply. R_s is chosen so that the series transistor is almost bottomed at the highest normal load current; at higher load currents, the regulator acts as a source of resistance R_s, as shown in Figure 1-2. Unfortunately the peak current which the series transistor must handle is $i_m + \frac{V}{R_s}$, where i_m is the maximum load current required at a regulated voltage V, and unless R_s is high a transistor rated well above i_m is necessary. If R_s is chosen large, the input voltage at no-load must also be large, and the series transistor power dissipation during normal regulation is increased, necessitating improved cooling or again a larger transistor.

1.3 Shunt Regulator Dissipation

The simple shunt regulator shown in Figure 1-3 contains a shunt load V2 controlled by an error amplifier V1. As the load decreases, current is diverted into V2 by the drop in the base-emitter voltage of V1. By keeping the voltage constant across the shunt paths V2 and R_L, this regulator maintains a constant current through the series resistance R_s (for a constant input voltage). For example, as the load current decreases, more current is diverted into V2 because the increase inthe base-emitter voltage of V1 increases the collector current in both transistors. During a short-circuit condition no current flows in the shunt path V2, and the load current is limited by R_s. The most stringent operating conditions for V2 occur at no-load, when it must withstand simultaneously the full-load current and the regulated output voltage.

1.4 Modification To Shunt Regulator

The high-dissipation condition in the shunt regulator can be improved with no loss in regulator performance by the inclusion of a resistance R_c in series with V2, as shown in Figure 1.4. R_c is chosen to be approximately equal to the minimum load resistance under normal conditions. In this way, the resistance

of the shunt path via V2 has a minimum value of $R_{L\ min.}$, occurring at no-load; nearly allthe output voltage is dropped across this resistor, leaving V2 with a low collector-emitter voltage. The shunt transistor power dissipation is now zero (ideally) at no-load and full-load, and maximum at half-load, when it is $\frac{V}{2} \cdot \frac{i_m}{2}$ - an improvement of four times. The shunt resistor R_c is chosen slightly lower than the minimum load resistance so that V2 is not bottomed near no-load. This allows the ripple voltage to be developed at the collector of V2 without clipping.

1.5 Output Resistance

The output resistance R_o of the shunt regulator may be calculated from Figure 1.5. The voltage error ε between the output e_o and the reference V controls an amplifier of transfer conductance g. Neglecting the current drawn by the amplifier V1,

$$\frac{e_{in} - e_o}{R_s} - i_o = g\varepsilon, \qquad \ldots 1)$$

and

$$\varepsilon = e_o - V \qquad \ldots 2)$$

therefore

$$e_o\left(g + \frac{1}{R_s}\right) = -i_o + \frac{e_{in}}{R_s} + gV,$$

therefore

$$R_o = -\frac{\Delta e_o}{\Delta i_o} = \frac{1}{g + \frac{1}{R_s}} \qquad \ldots 3)$$

This can never be made zero, and a simple amplifier might have $g = 10$ amp/volt, giving an output resistance of about 0.1 ohm.

1.6 Load Compensation

It is not necessary to resort to a more elaborate amplifier to reduce the output resistance if use is made of load compensation. The circuit in Figure 1.6 shows a simple way in which to incorporate load compensation by using the presence of the limiting resistor R_c: a fraction α of the shunt transistor collector voltage e_c is added to the reference voltage V.

Then, neglecting the currents in V1 and R1, for simplicity, but assuming the source resistance of the voltage αe_c to be very low

$$\frac{e_{in} - e_o}{R_s} - i_o = g\varepsilon, \qquad \ldots 4)$$

$$\varepsilon = e_o - V - \alpha e_c, \qquad \ldots 5)$$

and

$$e_c = e_o - \left(\frac{e_{in} - e_o}{R_s} - i_o\right) R_c. \qquad \ldots 6)$$

Substituting 5) in 4),

$$\frac{e_{in} - e_o}{R_s} - i_o = g(e_o - V - \alpha e_c), \qquad \ldots 7)$$

and substituting 6) in 7), and regrouping terms,

$$-i_o (1 - \alpha g R_c) = e_o \left\{ g + \frac{1}{R_s} - \alpha g \left(1 + \frac{R_c}{R_s}\right) \right\} - gV + \frac{e_{in}}{R_s} (\alpha g R_c - 1). \qquad \ldots 8)$$

Therefore $$R_o = -\frac{\Delta e_o}{\Delta i_o} = \frac{1 - \alpha g R_c}{g + \frac{1}{R_s} - \alpha g \left(1 + \frac{R_c}{R_s}\right)}. \qquad \ldots 9)$$

This reduces to the result in 3) if $\alpha = 0$, but the more important case, which makes $R_o = 0$, is

$$\alpha = \frac{1}{g R_c}. \qquad \ldots 10)$$

When typical values of g and R_c are inserted in 10), it is seen that α is very small. The potentiometer R1 may therefore be chosen tojustify the earlier assumption that αR1 is of the order of ohms even though R1 $\gg R_c$.

Use of a value of α greater than $\frac{1}{g R_c}$ results in a stable negative output resistance.

It is also interesting to note the effect of α on the stabilization factor $\frac{\Delta e_o}{\Delta e_{in}}$. From 8),

$$s = \frac{\Delta e_o}{\Delta e_{in}} \qquad \frac{1 - \alpha g R_c}{R_s \left(g + \frac{1}{R_s} - \alpha g \left(1 + \frac{R_c}{R_s}\right) \right)} = \frac{R_o}{R_s} \qquad \ldots 11)$$

Hence the value of α which makes $R_o = 0$ also makes $s = 0$.

1.7 Regulator Circuit and Performance

The complete circuit of the ±12V 1 amp supplies is given in Figure 1-7. Each unregulated supply is obtained from a full-wave rectifier and a capacitor-input filter, and feeds the regulator through a series resistance which is also employed as a ripple filter. The regulator differs slightly from the basic circuit of Figure 1-6 by the inclusion of a 9 volt Zener diode in the emitter of V1 to reduce the power dissipated in that transistor. The two Zener diodes in series comprise the reference voltage, and no adjustment is provided for the output voltage.

The load compensation factor α is made adjustable over a small range from zero to 0.03, so that the output resistance can be set finely. Since the amplifier has a transconductance of about

10 amp/volt, the critical value of α is about 0.01, and the output resistance can therefore be made negative to about -0.1 Ω. The amplifier gain is a function of the load current, since the transistor current gain varies with the collector current, and consequently the critical value of α cannot be maintained over the full load range. Nevertheless, the compensation technique holds the output voltage variation, including ripple, to less than 2 mV during a full-load change and an AC input voltage change of $\pm$ 15%.

1.8 Conclusions:

Two techniques have been developed which can be applied easily to any shunt regulator and offer easing of transistor dissipation and improved performance with no penalty. These techniques are believed to be novel.

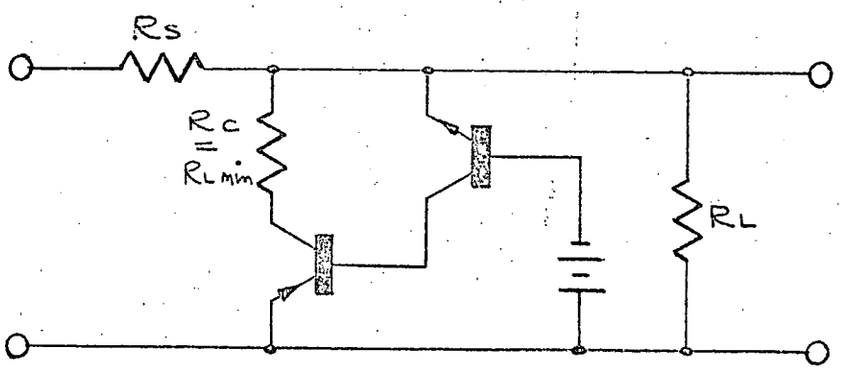


FIGURE 1-4

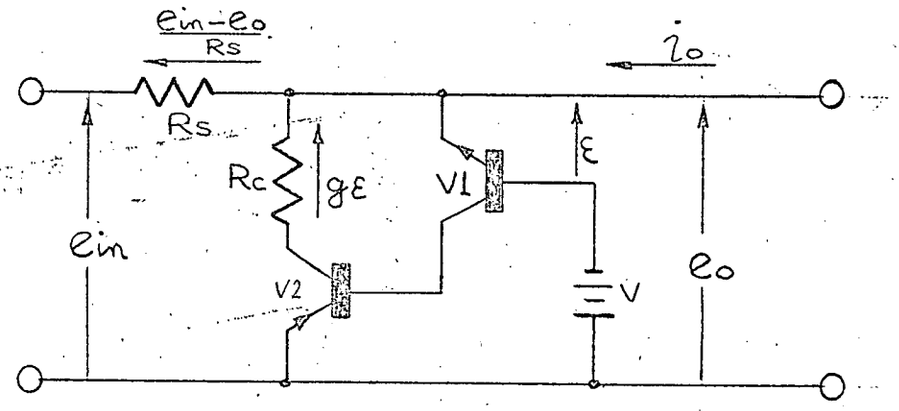


FIGURE 1-5

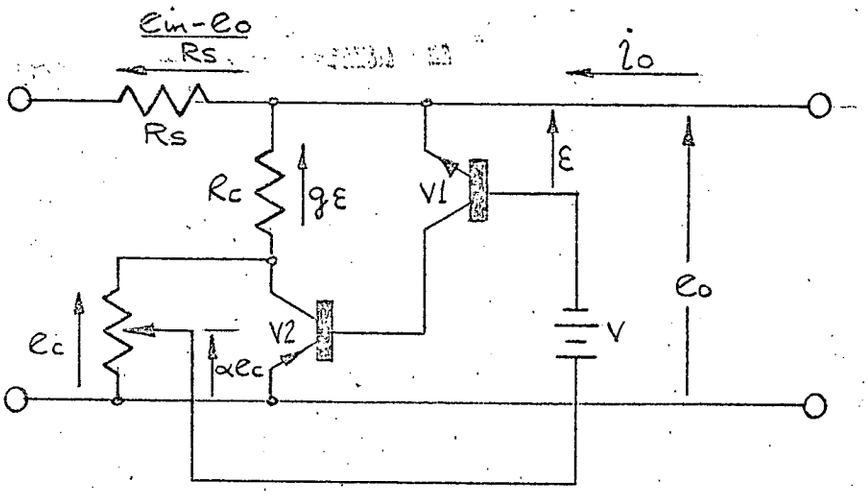


FIGURE 1-6

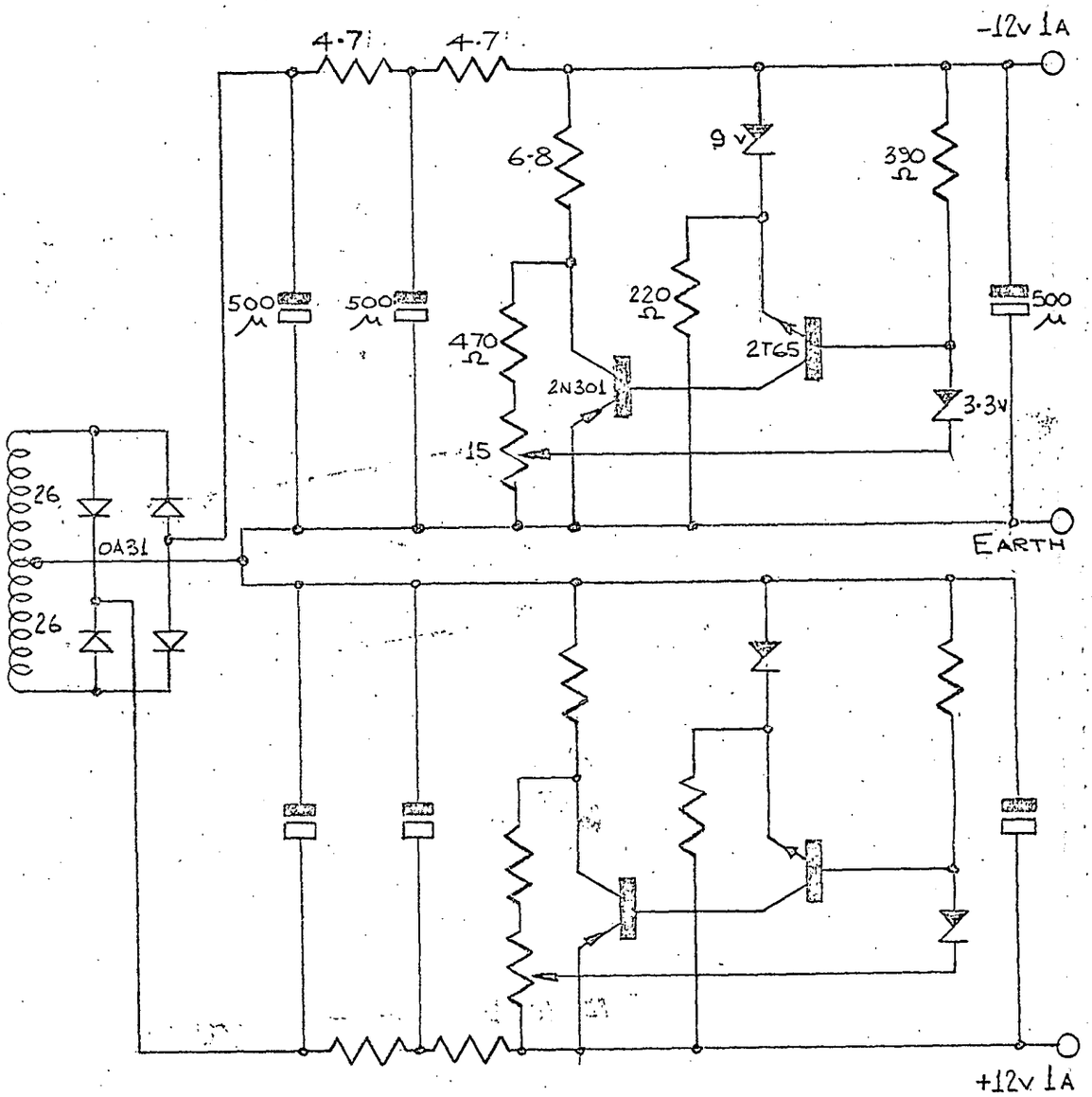

-12v 1A
4·7
4·7
6·8
9v
390 Ω
500 μ
500 μ
220 Ω
2TG5
500 μ
470 Ω
2N301
3·3v
15
26
OA31
26
EARTH
+12v 1A

FIGURE 1-7

2. PORTABLE BRIDGE FOR BOREHOLE TEMPERATURE MEASUREMENT

2.1 Introduction

An earlier design† of a transistorized unit for measurement of borehole temperatures was found to be inconvenient in operation due to its having a long settling time after switching transients.

The principle of operation of this unit was to match the resistance of a calibrated thermistor in an a-c bridge, balance being detected by a transistor amplifier and a phase-sensitive rectifier, and indicated by ameter. The fault lay in the capacitive-coupling of the bridge amplifier, and this part of the unit was re-designed. As a result, it was found that the heavy phase-detector transformer could be eliminated, and the whole amplifier, rectifier and meter amplifier was integrated in a new design.

This report describes the bridge technique and the new null-detection system.

2.2 Bridge Technique

The bridge consists of two equal oscillator-fed transformer arms, the thermistor, and the ratio arm. Bridge unbalance due to inequality of the two resistive arms produces a square wave voltage at the exciting frequency between the centre of the transformer arms and the centre of the resistive arms. If the unbalance is also capacitive or inductive, a transient analysis will give the modified square wave which isproduced. The sign of the output voltage with respect to the exciting voltage differs either side of resistive balance, the amplitude passing through zero at balance. However, since the excitation waveform is symmetrical, a change of sign through zero is the same as a discrete change of phase of 180°, and a phase-detector provides a very sensitive unbalance detector.

† G.H. Newstead: "A Portable Light Weight Bridge for Use in Borehole Temperature Measurements", University of Tasmania, February, 1958.

2.3 Bridge Amplifier

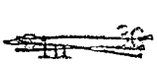
The phase detector is preceded by a high-gain amplifier and followed by a low-gain d-c amplifier to drive the indicating meter.

The redesigned preamplifier is direct coupled, and by use of a balanced amplifier it is possible both to reduce temperature drift effects to insignificance and to incorporate a simple phase detector not requiring a bulky and heavy transformer. The meter amplifier also uses a balanced circuit, and is direct-coupled to the phase detector.

Consequently the amplifier and phase detector circuits are inseparable and not easily recognised inthe schematic diagram, Figure 2.1.

The amplifier will be described first, and the action of the phase detector can then be more easily explained.

In Figure 2-2, the basic amplifier circuit can be seen as a three-stage balanced amplifier. The first stage is a common-emitter difference amplifier provided with common-mode feedback equivalent to a long tail in order to stabilize the stage against temperature unbalances in the two transistors. It drives balanced emitter followers which provide a low impedance source for the final common-emitter difference amplifier driving the meter. The resistances in the collector circuits of the emitter followers are used only to establish the desired d-c conditions, and a small amount of emitter feedback is used in the final stage. The amplifier has a very low input impedance and a balanced input, which are ideal features for a bridge balance detector. The amplifier has a differential input impedance of 30Ω, an output voltage swing of 2.5 volts for maximum input, and a voltage gain of about 5000.



In this application it is necessary only to obtain the maximum gain before the phase detector, and minimum drift in the subsequent d-c amplifier. However, the amplifier must be stabilized so that it always operates in its linear range. To achieve this, transistors selected primarily for equality of leakage current and secondarily for current gain are used in each pair, and each transistor pair is mounted in an aluminium block which acts as a thermal short-circuit, to reduce the zero-drift resulting from differences in

base-emitter junction temperatures. Provision is made for balancing the circuit by trimming the collector currents of the first stage while the input is short-circuited.

2.4 Phase Detector

The phase detector acts as a synchronous shunt gate, as shown in Figure 2.3, by switching the input to earth via diodes. Both input potentials always have the same (negative) sign, and the output voltage e_o is equal to their difference unless the switch is closed, when e_o is zero. The switch is operated in alternate half-cycles, being driven in phase with the bridge excitation, and a phase-sensitive output is obtained when the phase of both input signals changes with respect to this excitation. This is shown in Figure 2.4(a) and 2.4(b).

The input points A and B both have a negative d-c component greater than the signal amplitude, but both are returned to earth when the switch is closed. The output voltage is therefore zero for every alternate half-cycle, but otherwise equal to the difference of the input voltages, which is the bridge output. It is immaterial that each of the output terminals carries a negative pedestal because this pedestal is a common-mode voltage, and does not appear in the difference voltage.

Use of a delayed gating voltage permits a significant improvement in rendering the bridge insenstive to reactive unbalance. The thermistor cable capacitance produces ~~insensitive~~ transients in the bridge output as shown in Figure 2.5(a), which, with the syncrhonous gating described above, produces a phase-detector output as in Figure 2.5(b). The initial amplitude of the transient depends largely on the amount of capacitive unbalance, and the final amplitude is largely dependent on the resistive unbalance. The bridge is provided with several switched capacitances on the ratio arm to decrease the capacitive unbalance, but the transient peaks still contribute significantly to the average detector output voltage. They can be removed to some extent by holding the phase gate closed longer than one half-cycle until the transient has decreased to a tolerably small amplitude, as shown in Figure 2.5(c). A combination of capacitance balancing and gate delay satisfactorily overcomes the cable effects. Delayed gating decreases the average detector output even in the case

of capacitive balance, but the gain of the preamplifier is easily sufficient to permit full drive of the output amplifier.

2.5 Gating Circuit

The phase-gating is done at the output of the emitter followers which provide low impedance sources of the balanced phase-detector inputs. This circuit is shown in Figure 2-6. The shunt switch consists simply of a common-emitter transistor which is driven by a gating pulse. The collector resistances in the emitter followers not only set the standing d-c level at the emitters, but also limit the current drawn through the gating transistor. A small potentiometer, P1, permits balancing of the gate circuit.

The gating pulse is derived from the bridge excitation, and delayed by a monostable multivibrator, which is triggered at the beginning of every cycle, and whose time-constant is chosen so that the output returns to its stable state approximately 1.3 half-cycles later. An emitter follower is used to drive the multivibrator output into the gate, as shown in Figure 2-7.

2.6 Output Amplifiers

The output meter used inthe original equipment was a 25 - 0 - 25μA movement, and is retained. When the bridge is well of balance, the amplifier output current could damage the meter; a "coarse and fine balance" attenuator is therefore used. The amplifier saturates if the input voltage exceeds 500μv, and the coarse meter attenuator is chosen so that the meter gives FSD when this condition is reached. The fine attenuator is included since the sensitivity of the bridge is excessive. A non-polarized 100μf capacitor filters the amplifier output to d-c. Provision is made for operation of an external 2.5KΩ pen-recorder at a lower sensitivity.

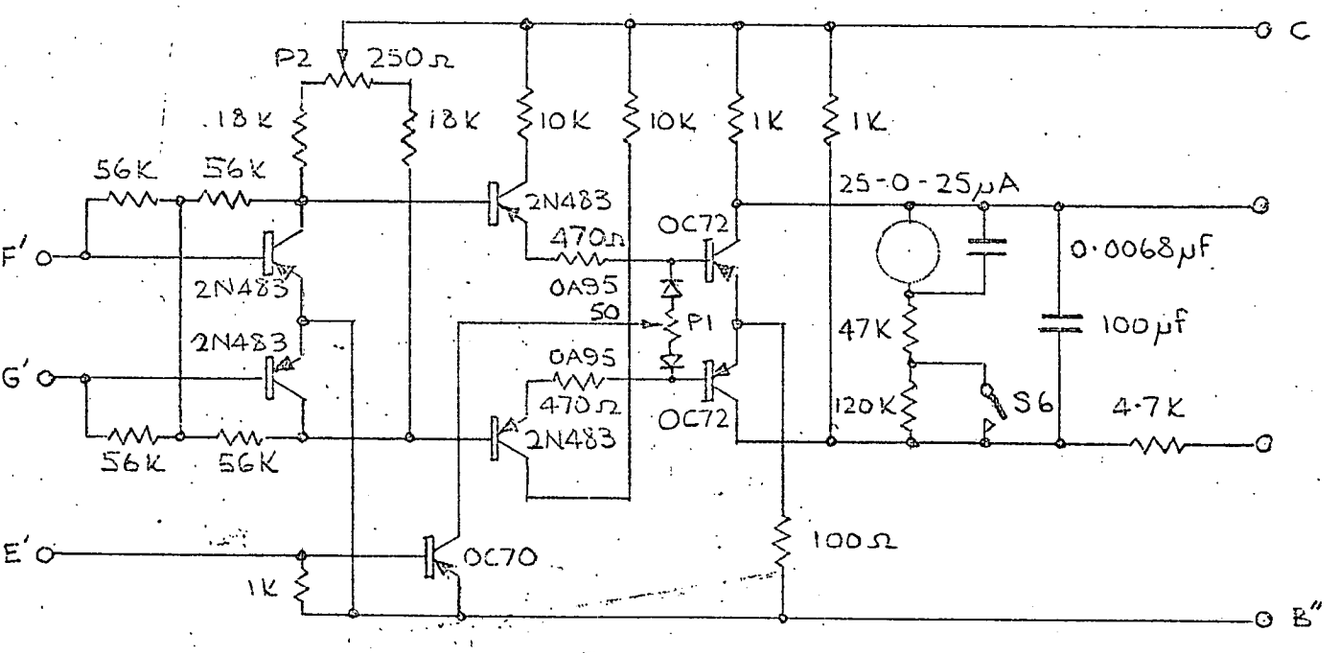
2.7 Results

It has been found that the zero stability of the amplifier and phase detector system is equivalent to about 5Ω bridge unbalance. For the thermistor used during temperature measurement, this corresponds to about 0.001^{9}C, which is an improvement of one

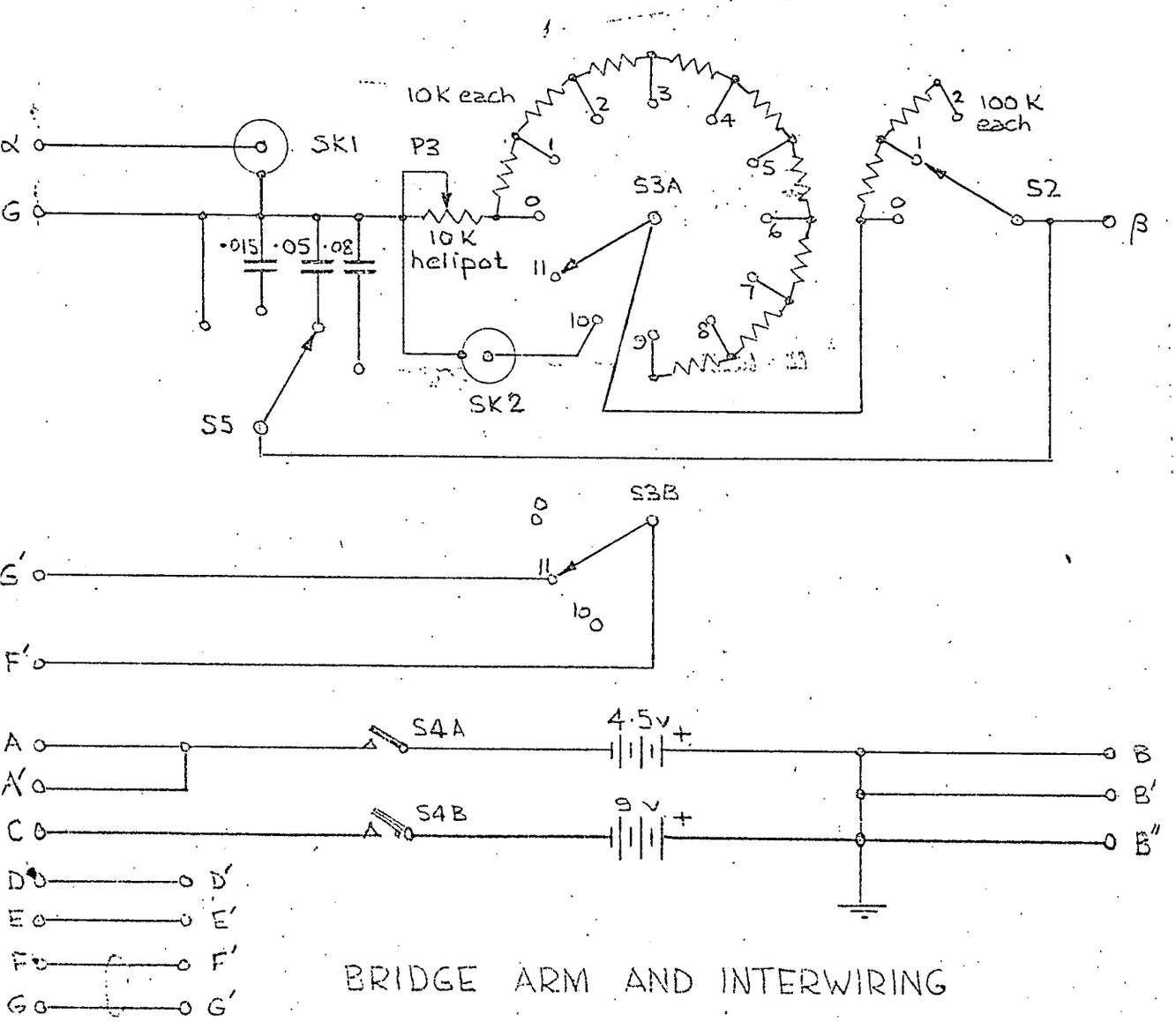
order on the zero stability of the previous design, and makes the amplifier the least source of error in temperature measurement.

2.8 Comments

The excellent stability of the bridge and amplifier makes this device ideal for the measurement of resistances by matching with a standard decade resistance box. Its present sensitivity is about 5Ω in 100 KΩ, or 0.005%. An increase in the bridge oscillator power would be necessary for bridge arms less than about 1000 ohms.



AMPLIFIER AND PHASE DETECTOR



BRIDGE ARM AND INTERWIRING

FIGURE 2-1

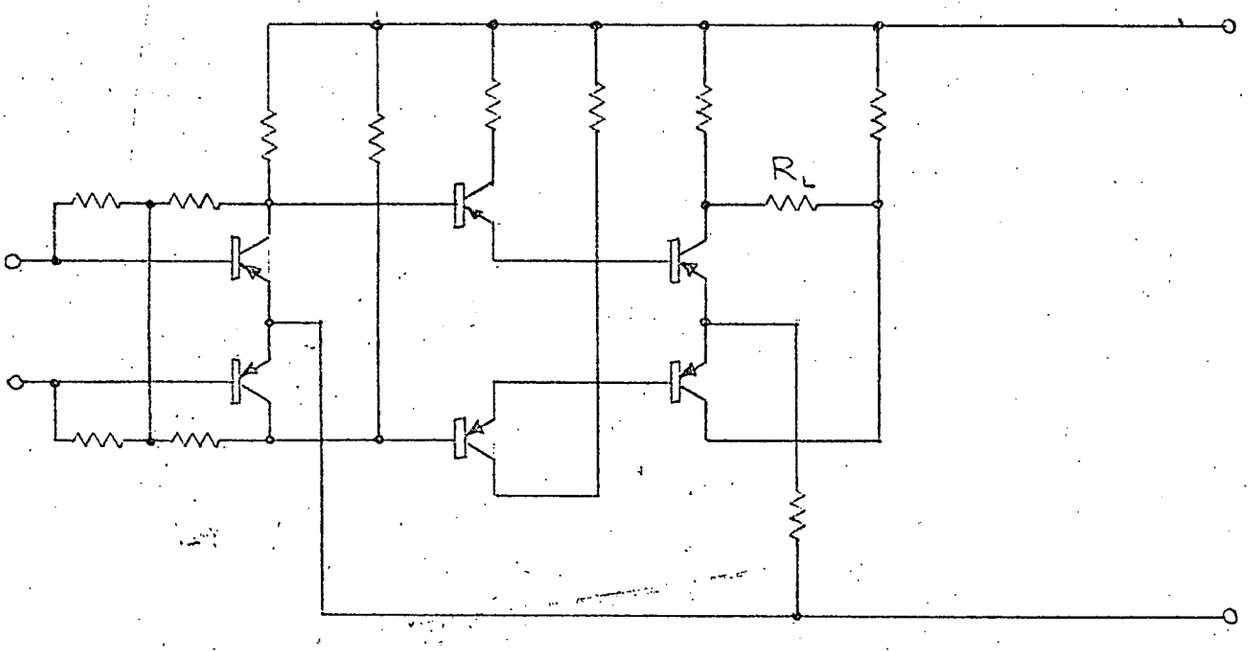


FIGURE 2-2

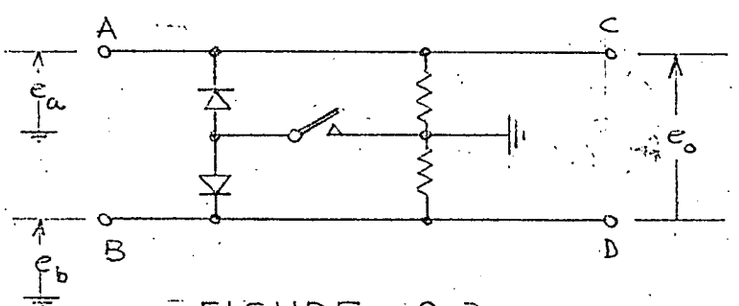


FIGURE 2-3

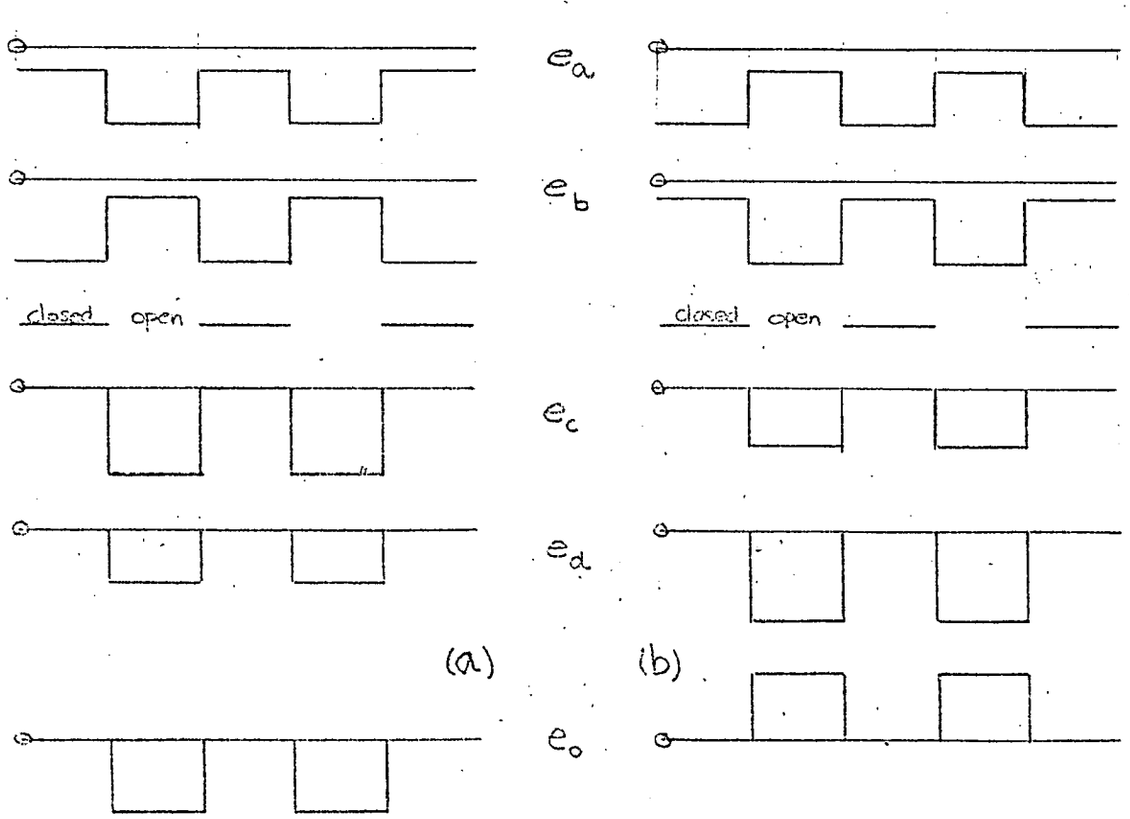


FIGURE 2-4

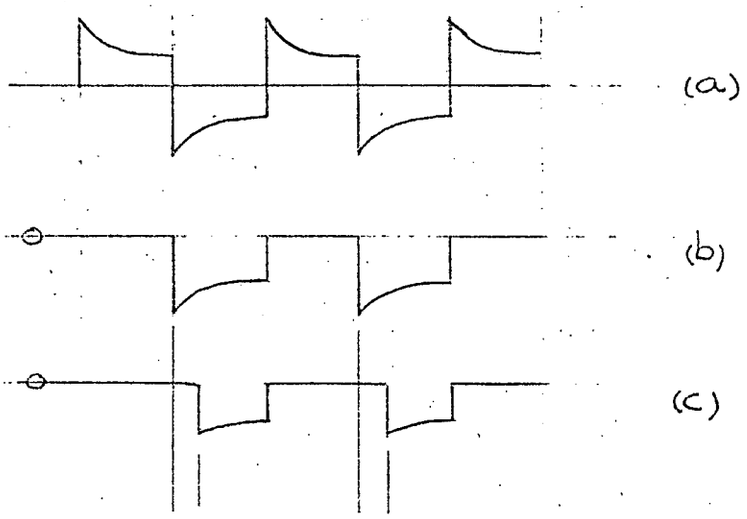


FIGURE 2·5

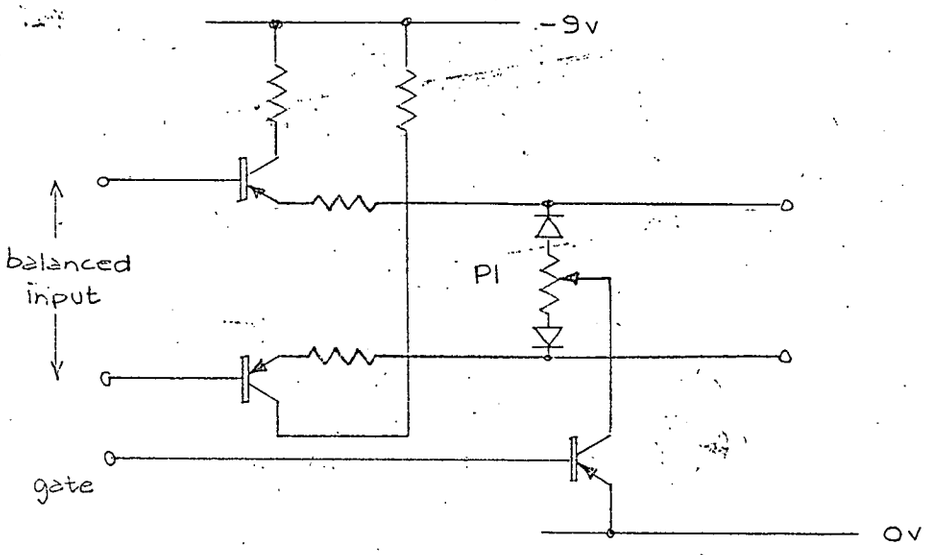


FIGURE 2·6

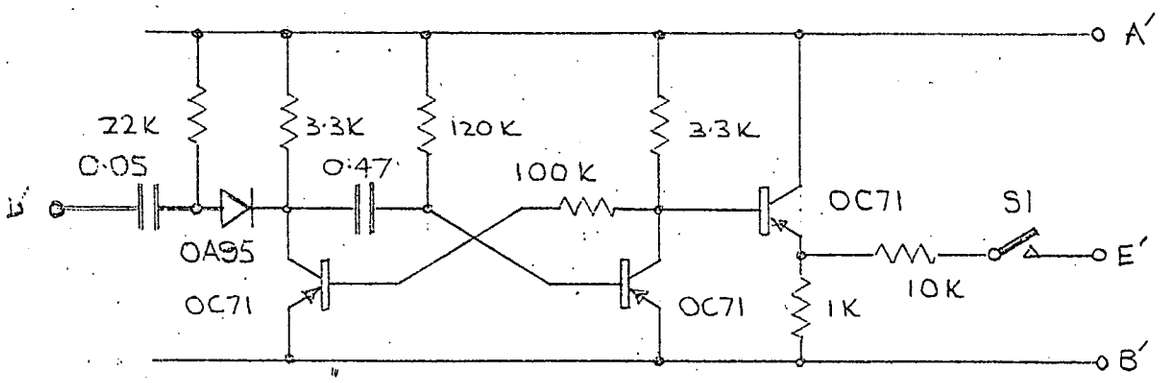
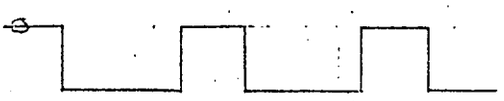


FIGURE 2·7



3. RULER TIME-SCALE UNIT

3.1 General Description

This equipment is operated by a clock contact actuated every second, and provides a 5 millisec pulse every second, minute, 5 minutes, and hour. These pulses may be varied in amplitude from zero to +6 volts, and may be distinguished on a record by being given different heights in the manner of ruler graduations. A gating voltage is also provided consisting of +6 volts available for aperiod lasting from one minute before the hour to one minute after. The output voltage s are all supplied from impedance of 100Ω and are short-circuitproof. A further facility provided is a changeover relay contact actuated for one second after every minute pulse, and for two seconds after every hour pulse. The make contact is used to switch a 1 Kc/s signal into a telephone line which is also employed at lower frequencies for data telemetry. A separate unit, for use at a remote station, demodulates the high-frequency signal and operates a relay. All circuits have been designed to operate in ambient temperatures between 10°C and 55°C, The current drawn from the clock contacts is limited to a peak of 0.4 mA to ensure long life.

3.2 Block Diagram of Unit

The block diagram of the equipment is shown in Figure 3-1. The clock contact operates a pulse shaper which removes the contact bounce and generates a standard pulse suitable for triggering the frequency dividers and pulse generators. These generators produce the 6 volt 5 millisec positive pulses at the appropriate times, and are followed by attenuators to change the relative heights to the desired format of a ruler time-scale. An OR gate then passes the largest of these appearing at any second, and feeds the drive amplifier which produces the low output impedance and short-circuit protection suitable for cabling the signals to a recorder. AND gates connected to the frequency dividers select the appropriate instants when the gating voltage and relay operation are to be made available, and these gates feed drive amplifiers to provide these functions.

3.3 Circuit Details

3.3.1 Pulse Shaper

The Pulse Shaper shown in Figure 3-2 is an amplifier

consisting of a common-collector common-base pair of transistors, whose static input is derived from a fixed divider across the supply rails. The input diode is normally biassed off by an integrating capacitor charged from the negative rail, and closing of the clock contact discharges the capacitor towards the positive rail. When the diode becomes biassed on, a step of + 1.9 volts occurs at the base of the first transistor, turning it off, and causing a +6 volts step at the output of the second transistor. While the clock contact is closed, the input voltage remains positive, and when it opens the voltage falls instantaneously to the initial negative bias, a negative output step being generated. Contact bounce on the closing contact is overcome by the integrating capacitor, the time-constant being chosen so that the positive output step isused to trigger the Pulse Generator, while the negative output step has no effect upon it.

3.3.2 Pulse Generator and Attenuator

The Pulse Generator, Figure 3-3, is a monostable multi-vibrator with a relaxation period of 5 millisec. It is base-triggered by the positive edge of the Pulse Shaper output, and once triggered it is independent of external conditions until it has returned to its stable state. The output is taken from the collector of the triggered transistor, and is a negative 6 volt 5 millisec pulse. An NPN inverting amplifier returns this to a +6 volt pulse, and an attenuator permits selection of any fraction of this amplitude for the output drive amplifier.

3.3.3 OR Gate

The 4-input OR gate, Figure 3-4, employs NPN transistors with a common emitter resistor. This multiple emitter follower gives an output of the largest of the four positive inputs, and presents high impedance loads to the four attenuators.

3.3.4 Drive Amplifier

Capacitive loads may be driven from the complementary emitter follower shown in Figure 3-5, since load current

may flow in either direction. A series resistance is included in the output so that short-circuiting of the output to earth does not damage the output transistors. The output impedance of the amplifier is composed largely of this resistance.

3.3.5 Frequency Dividers

Frequency division is obtained with cascaded bistable multivibrators using gated resetting to give the desired count.

For a count of n, AND gates identify a count of n-1, and operate gates for the input to the appropriate binary stages so that the next input pulse resets the chain. Positive-going waveforms represent "1" in the convention adopted and are used throughout the unit for triggering. Resetting to "1's" ensures that no pulses are transmitted from one stage to the next during resetting, for this would cause a false count. The output from the chain of binaries is obtained from another AND gate which identifies the count n, which is the same as the reset state.

Division ratios of 60, 12 and 5 are required, and these are provided as follows:

$$12 = 2 \times 2 \times 3$$

$$60 = 5 \times 12 = 5 \times (2 \times 2 \times 3).$$

By breaking down the ratios into prime factors the simplest combinations of binary stages may be found. In this case only two prime factors other than 2 are required, viz. 3 and 5, and these are made up from binary stages with feedback resets. A typical bistable multivibrator is shown in Figure 3-6, and the complete ÷ 3 and ÷ 5 circuits are given in Figures 3-7 and 3-8. It is possible to economize on components in the ÷3 section, so that the essential action of this circuit is not obvious, but the ÷ 5 section contains the typical elements of the gated-reset method. Input pulses base-trigger the first binary via steering diode AND gates which are normally open and the third binary on the "1" side via a diode AND gate which is normally closed. The first binary output feeds the

second binary, and this feeds the third, in the usual way, the connections being via gates to provide a steering action which is conveniently available (but not essential). The input pulses trigger the binary cascade normally until the gates on the input change. The transistor AND gate is operated by the three coincident inputs, A, B, $\bar{C}$, which, according to the table accompanying the circuit, corresponds to a count of 4 input pulses. This then opens the gate from the input to the third binary, and closes the gate to the first binary so that the next input pulse goes directly to the third binary and resets it to "1". Since the other two binaries are already in the state "1" and receive no triggering pulse, the whole circuit is reset by this fifth pulse. This reset action closes the transistor AND gate, restoring the gates on the input to their original conditions. The fifth pulse causes a "1" to appear on the third binary, and as this is the only time during the count that this occurs, it is taken as the output of the $\div$ 5 circuit.

The counters may be reset to zero count at any time for synchronization with local time signals.

The complete circuits of the three dividers in the unit are given in Figure 3-9.

3.3.6 Gating-voltage AND Gates

To obtain an output from 1 minute before each hour until 1 minute after, it is necessary only to select counts of 59 and 0 in the minute counters. A count of 59 is recognized as the 4th minute in the 11th 5-minute period, that is, a count of 4 in the minute counter and simultaneously of 11 in the 5-minute counter. A count of 0 minutes is given by counts of zero in both these counters, since the whole unit recycles hourly. The states of the appropriate binaries on these counts are given by

$$59 = HJ\bar{K}LMNP = HJ\bar{K}LMP$$

$$0 = \bar{H}\bar{J}KLMNP = \bar{H}\bar{J}KLMP$$

Since 4 of the 6 inputs to these two gates are the same,

these are combined first, and the complete gates are shown in Figure 3-10.

3.3.7 Minute-and-Hour Relay Operation

To produce a 2 second gating voltage after each hour, the 1 minute-after-the-hour voltage already available in the unit is combined in an AND gate with a 1 second voltage beginning 1 second after the minute voltage. Another AND gate produces a 1 second-every-minute output. These two outputs are then put through an OR gate so that either may operate the relay. The gating is calculated as follows;

from 0 seconds to 1 second-after-every-minute

= seconds counter 0

= ABDG,

and from 1 second to 2 seconds-after-every-hour

= 1 in seconds counter,
zero in minutes counter, and
zero in 5-minutes counter,

= $\overline{\text{ABCEFKLMP}}$

KLMP is already available as 1 minute-after-every-hour, labelled "0 mins" in Figure 3-10, so that an AND combination of this and $\overline{\text{ABCEF}}$ gives an output from 1 to 2 seconds-after-every-hour. This and ABDG as inputs to an OR gate give 0-1 second-after-every-minute, and 0-2 second-after-every-hour. The circuit is given in Figure 3-11.

3.4 Time-Marker Telemetry System

The relay function incorporated inthe ruler time-scale unit may be used to provide time markers at a remote station connected by a telemetry link. An existing link uses a telephone pair for 0-30 c/s seismic signals, and the time markers are transmitted by on-off modulation of a 1 Kc/s signal applied to the telephone line. At the receiving end, a tuned 1 Kc/s amplifier drives a demodulator which operates a relay to provide a marker on a recording instrument.

The block diagram is shown in Figure 3.12.

3.4.1 Transmitting Unit

The 1 Kc/s signal derived from the crystal clock is switched by the Time Scale Unit relay onto the line, as shown

in Figure 3-13, via an unbalance-to-balance transformer and isolating capacitors.

3.4.2 Receiving Unit

A balance-to-unbalance transformer d-c isolated from the line feeds a twin-T tuned amplifier. This is followed by a non-linear amplifier and low-pass filter to detect the modulation, and then by a d-c amplifier, which drives the relay. The circuit is shown in Figure 3-14.

The frequency response of the complete receiving unit is given in Figure 3-15. The gain of the detector-amplifier may be varied by control of the hold-on bias; the setting chosen gives an overall Q of about 10 so that a generous tolerance can be placed on the frequency-determining network in the tuned amplifier. A simple low-pass filter is included in the coupling between the tuned amplifier and the detector to eliminate high frequency line noise which passes through the isolation circuit, and overloads the tuned amplifier.

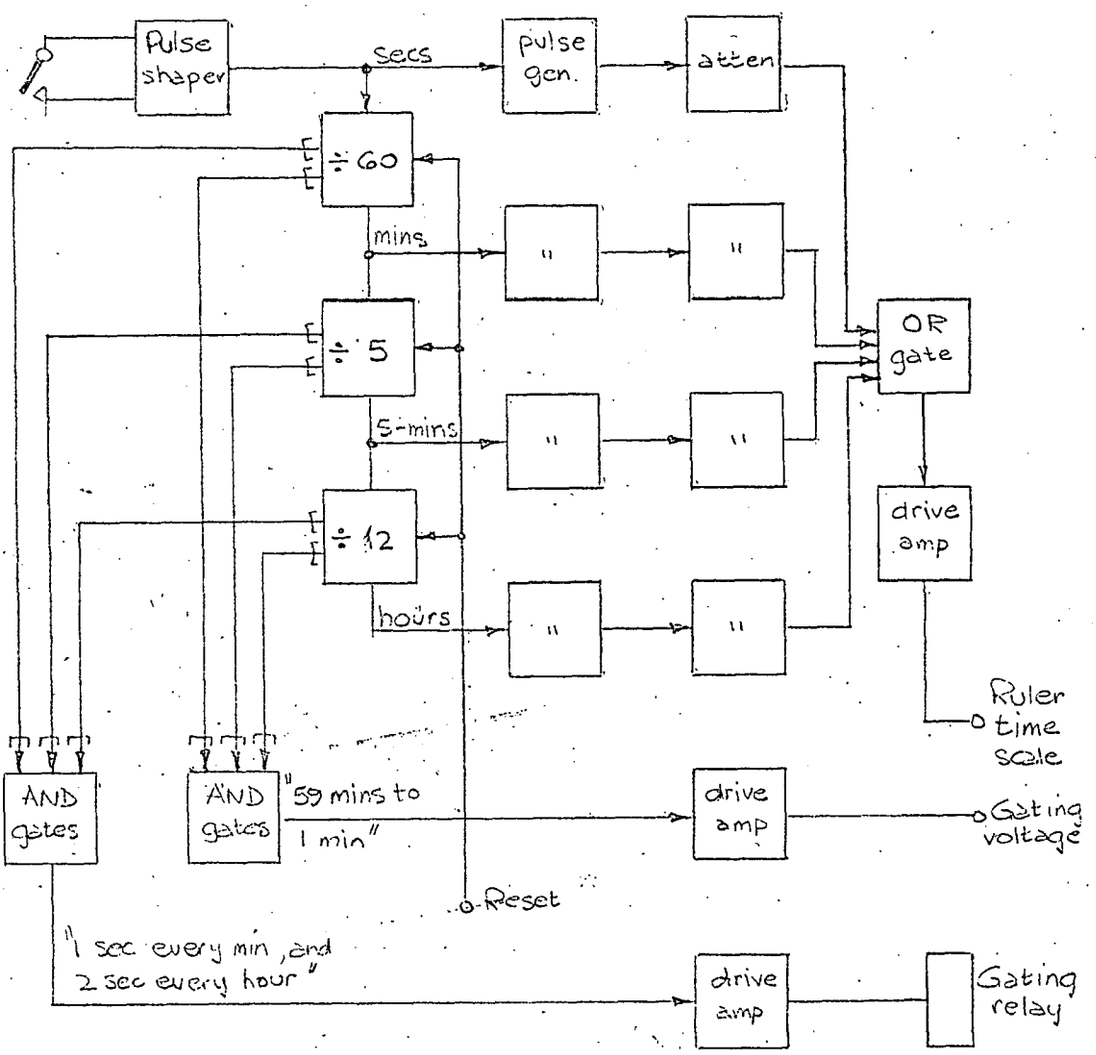


FIGURE 3-1

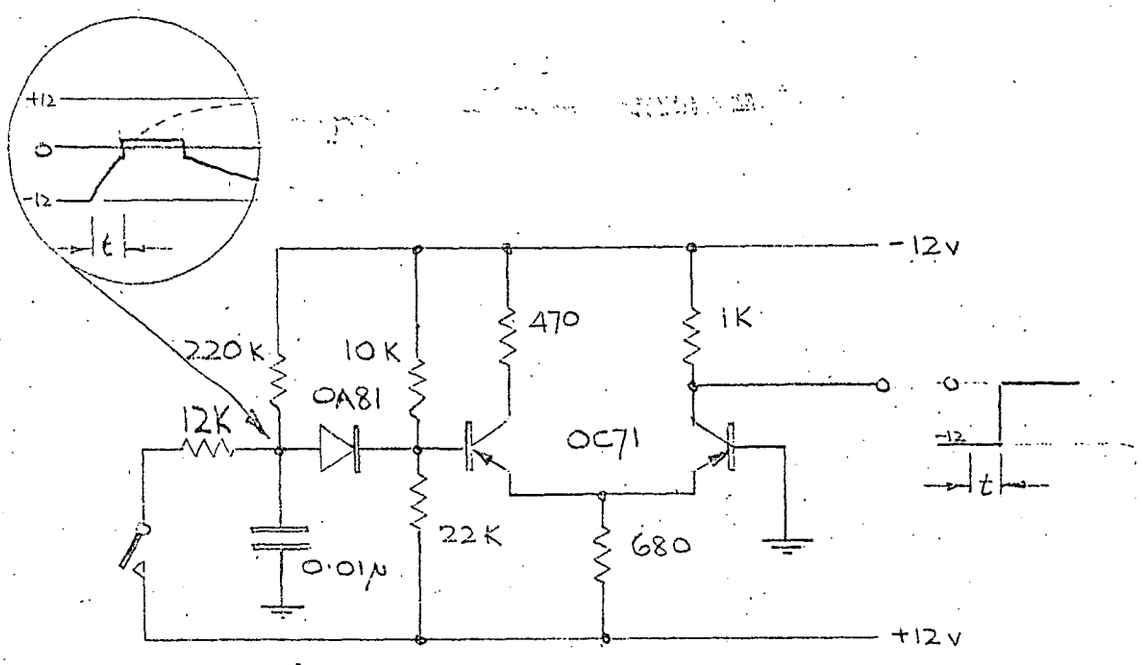


FIGURE 3-2

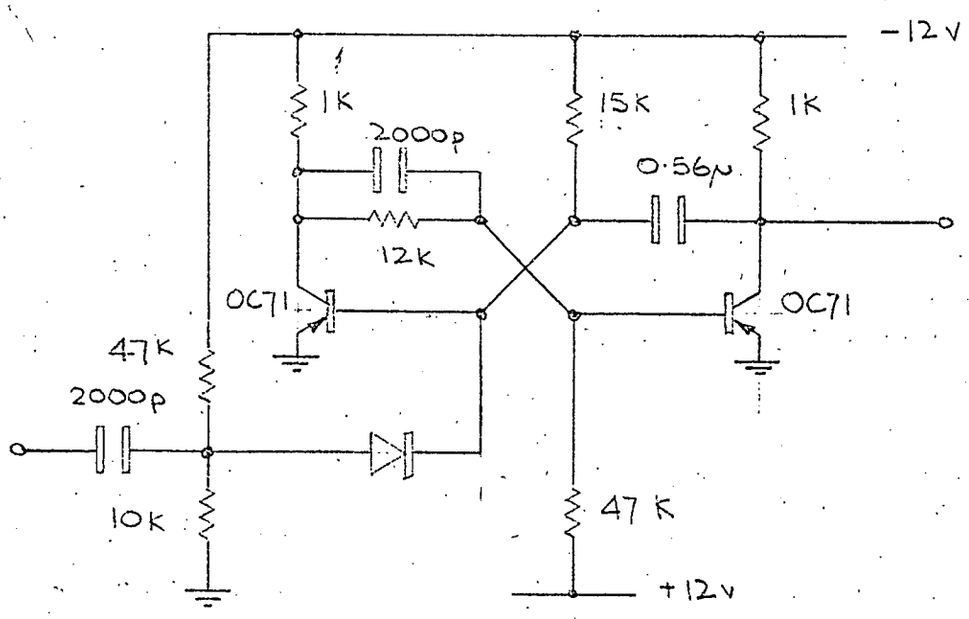


FIGURE 3-3

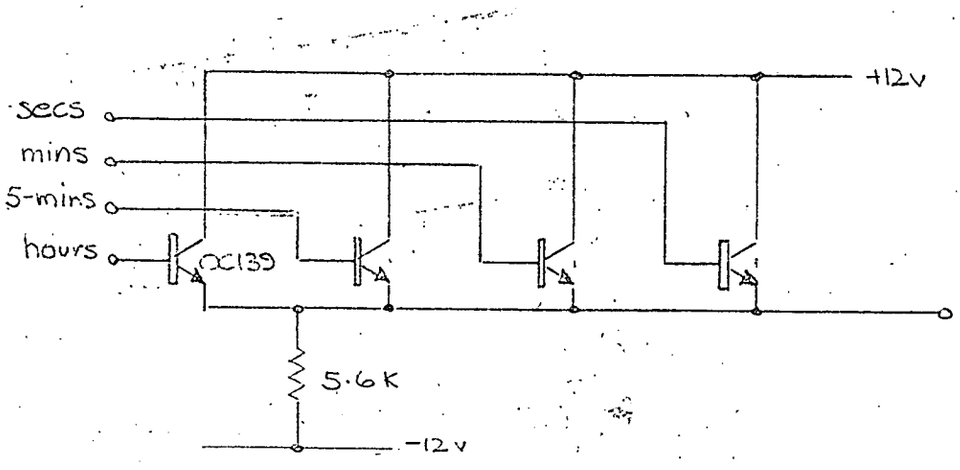


FIGURE 3-4

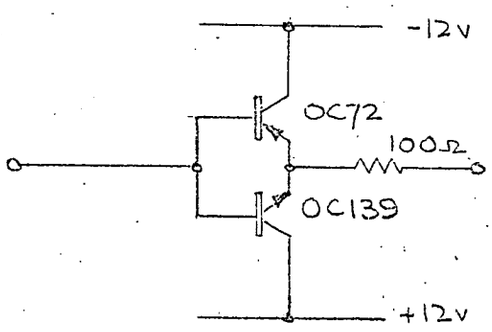


FIGURE 3-5

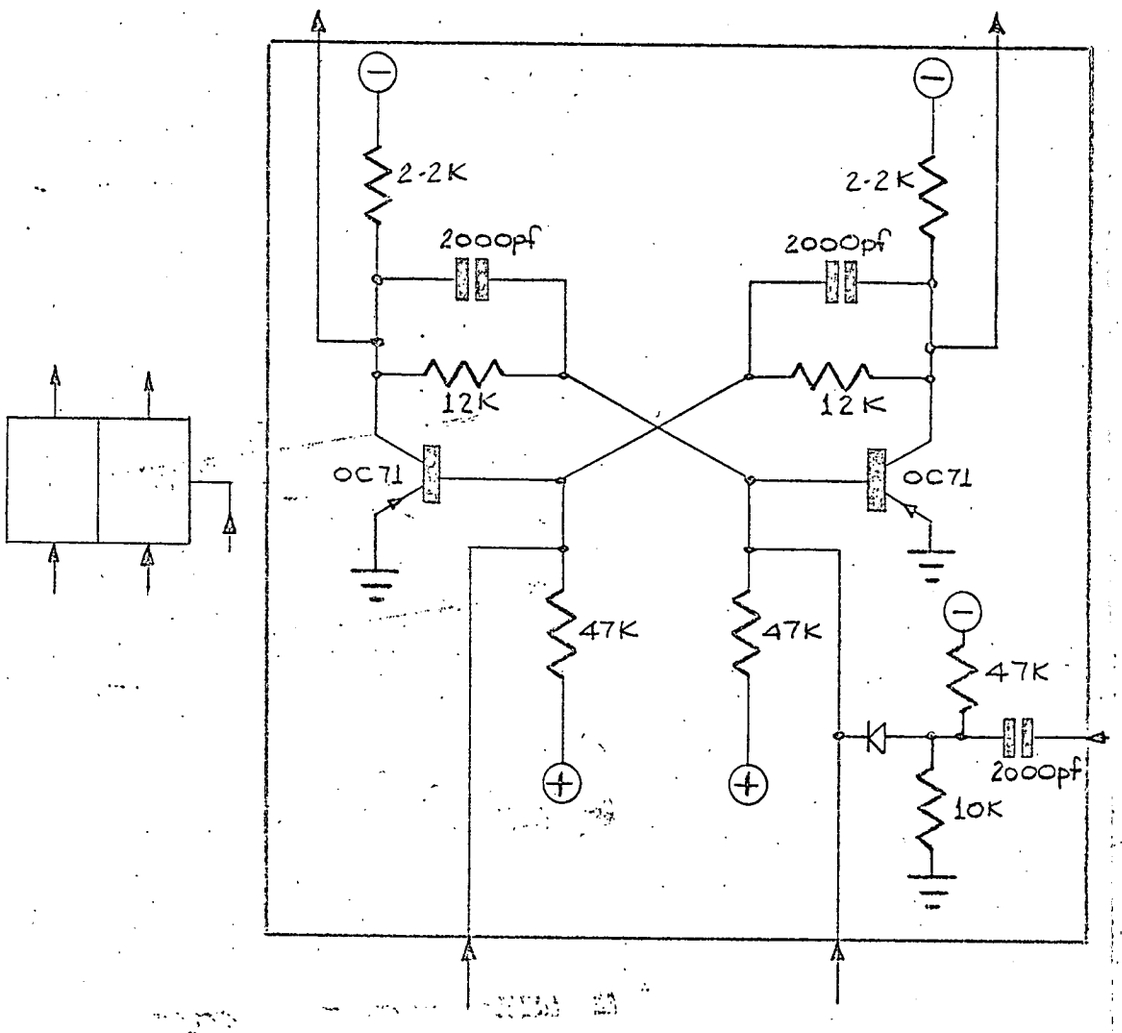
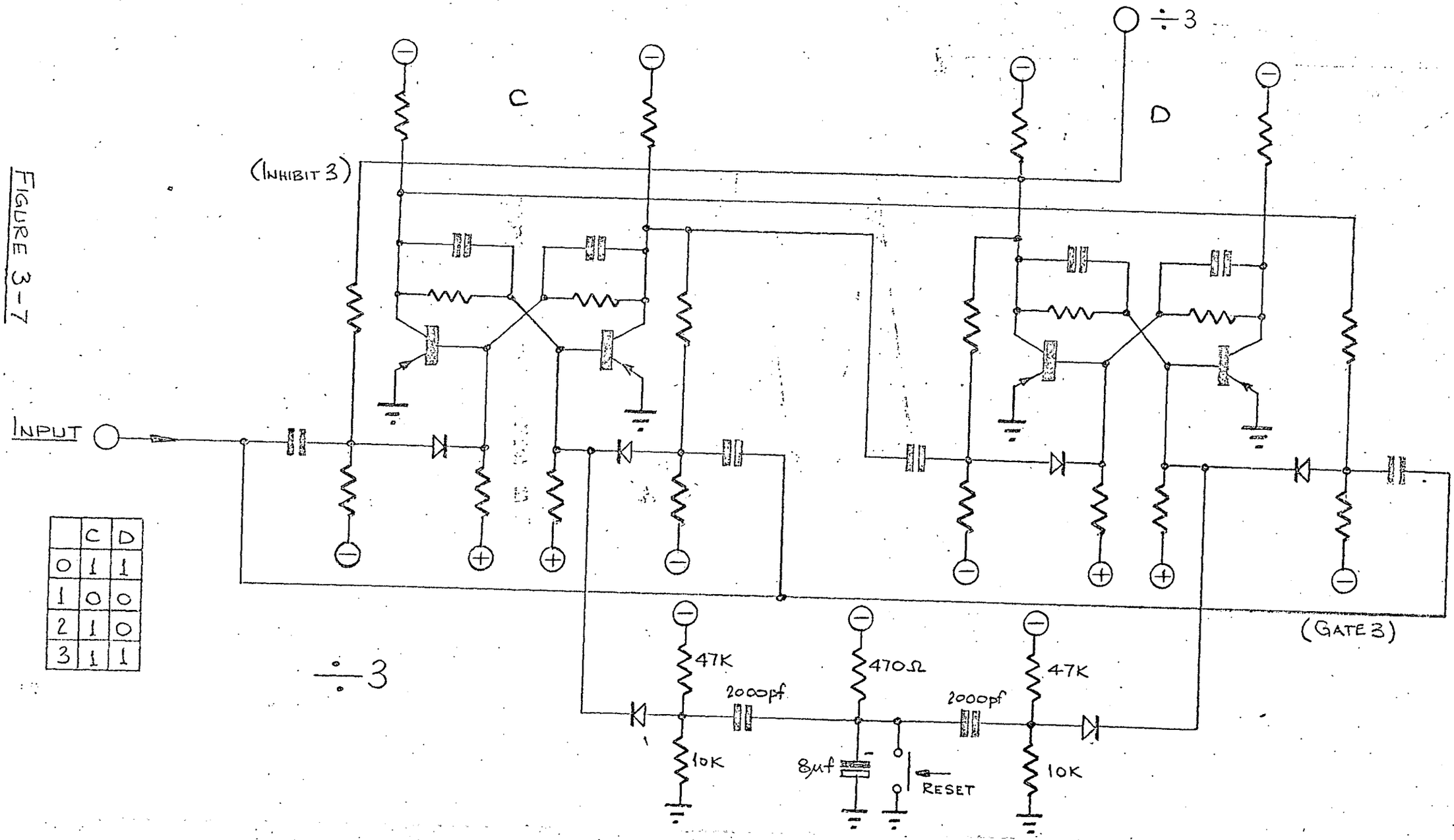

2-2K
2000pf
12K
OC71
47K
2-2K
2000pf
12K
OC71
47K
47K
2000pf
10K

FIGURE 3-6



	C	D
0	1	1
1	0	0
2	1	0
3	1	1

FIGURE 3-7

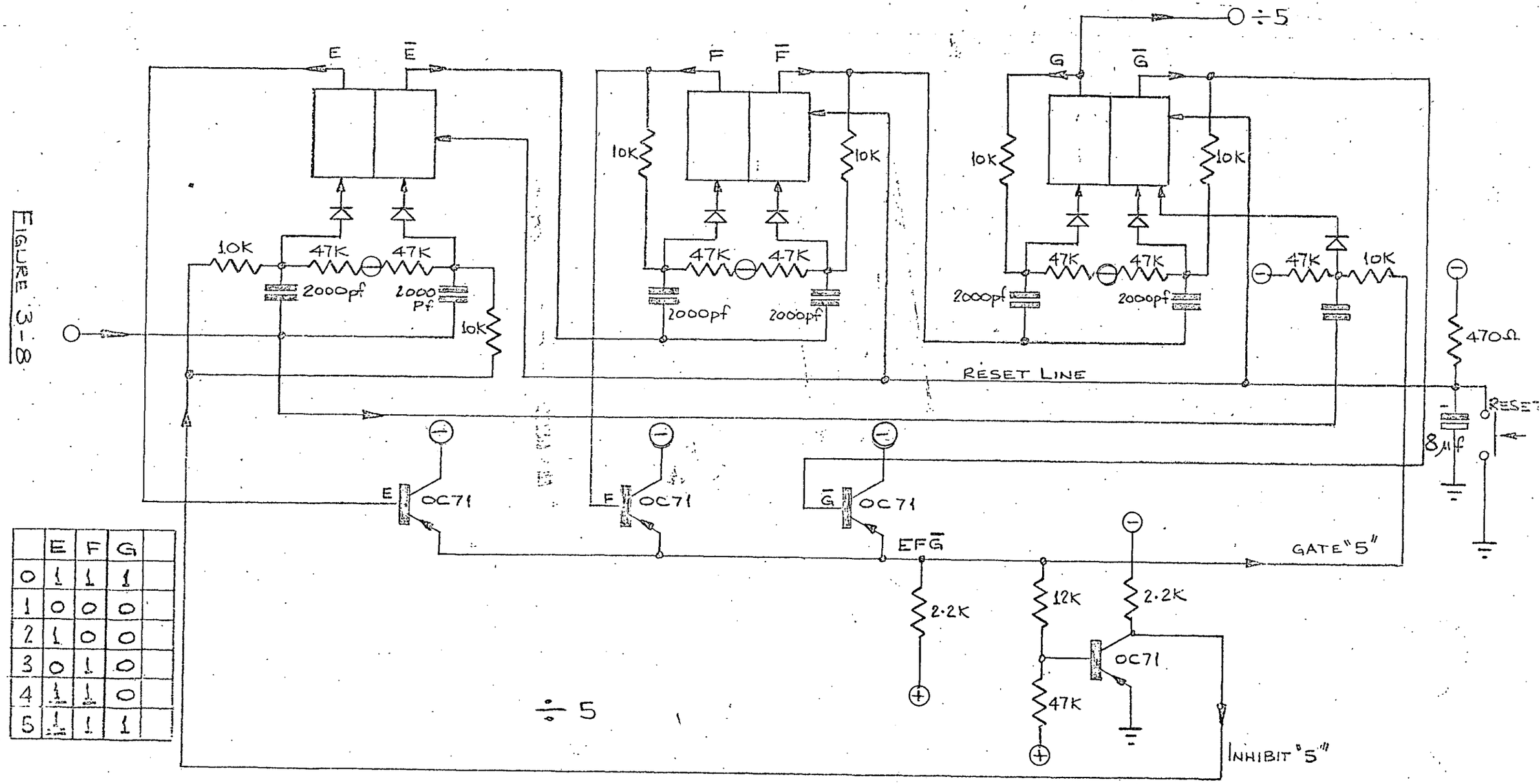


FIGURE 3-8

	E	F	G	
0	1	1	1	
1	0	0	0	
2	1	0	0	
3	0	1	0	
4	1	1	0	
5	1	1	1	

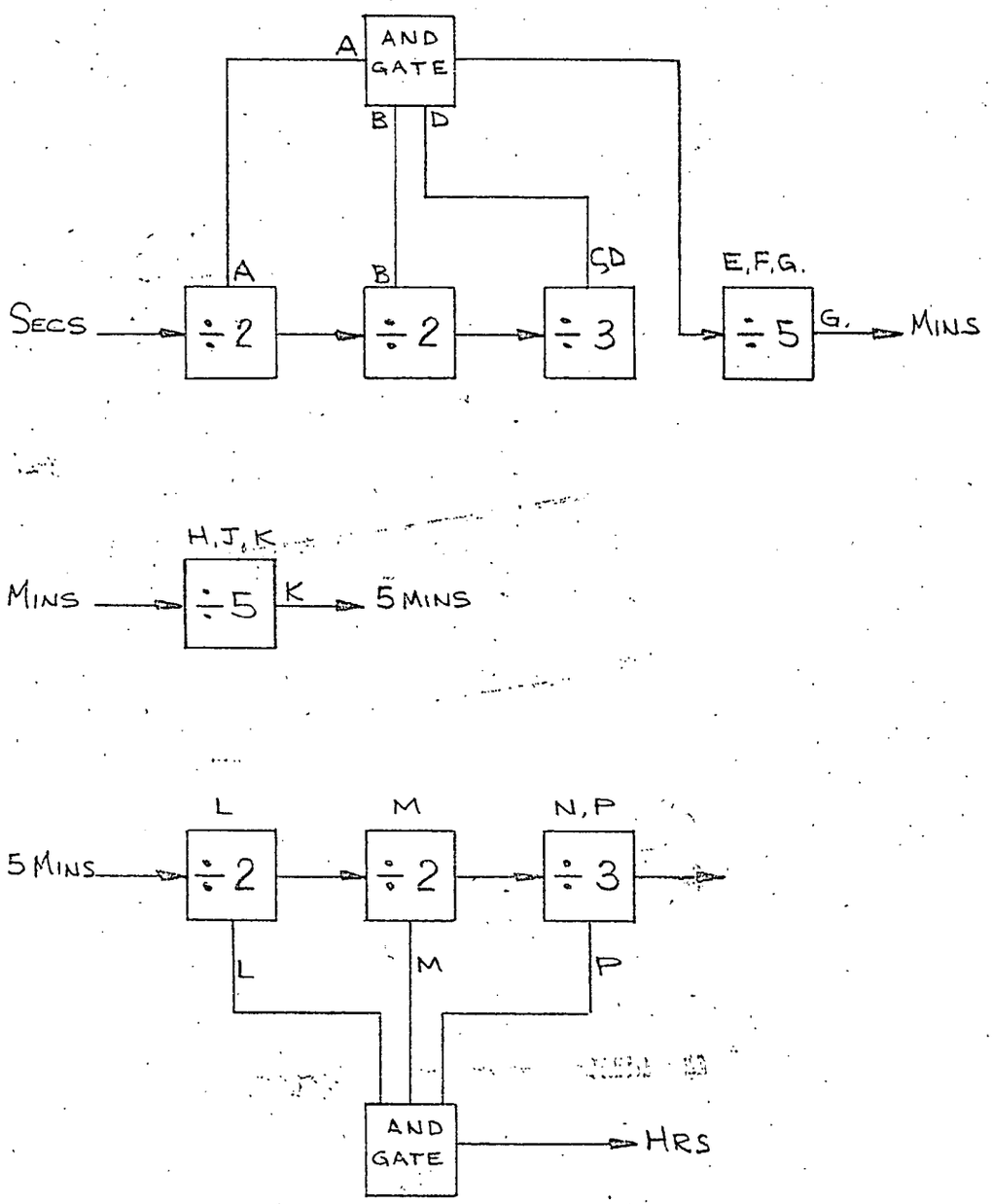

A
AND
GATE
B
D
A
B
C,D
E,F,G.
SECS
÷ 2
÷ 2
÷ 3
÷ 5
G.
MINS
H,J,K
MINS
÷ 5
K
5 MINS
L
M
N,P
5 MINS
÷ 2
÷ 2
÷ 3
L
M
P
AND
GATE
HRS

FIGURE 3-9

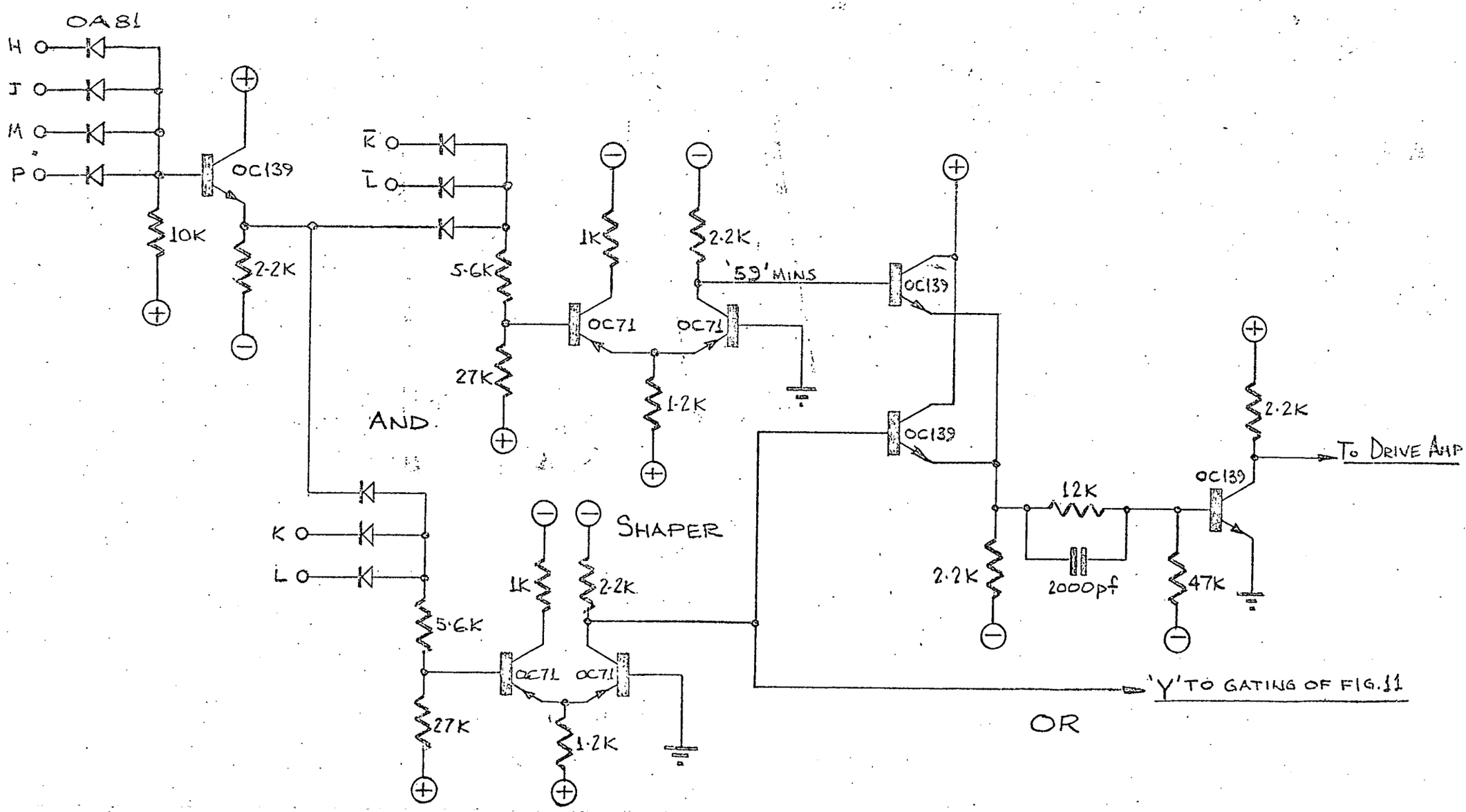

OA81
H
J
M
P
OC139
10K
2·2K
K̄
L̄
5·6K
27K
1K
2·2K
OC71
OC71
1·2K
'59' MINS
OC139
AND
K
L
5·6K
27K
1K
2·2K
SHAPER
OC71
OC71
1·2K
OC139
OC139
2·2K
12K
2·2K
2000pf
47K
OC139
2·2K
To Drive Amp
'Y' TO GATING OF FIG. 11
OR

FIGURE 3-10

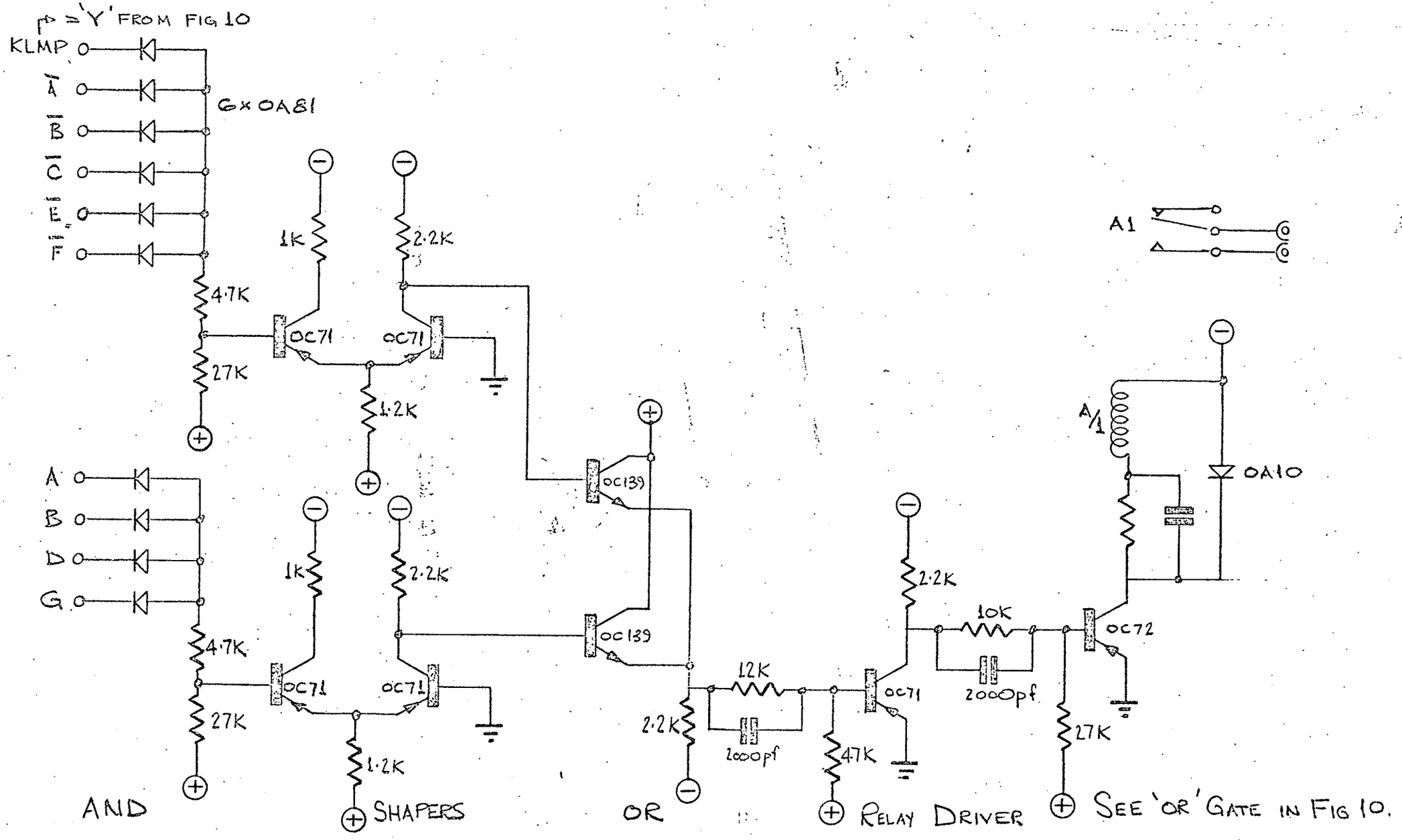

P = 'Y' FROM FIG 10
KLMP
A
B
C
D
E
F
6 x OA81
4·7K
27K
1K
2·2K
OC71
OC71
1·2K
A
B
D
G
4·7K
27K
1K
2·2K
OC71
OC71
1·2K
AND
SHAPERS
OC139
OC139
OR
12K
2·2K
2000pf
47K
OC71
2·2K
10K
2000pf
OC72
27K
RELAY DRIVER
A1
A/1
OA10
SEE 'OR' GATE IN FIG 10.

FIGURE 3-11

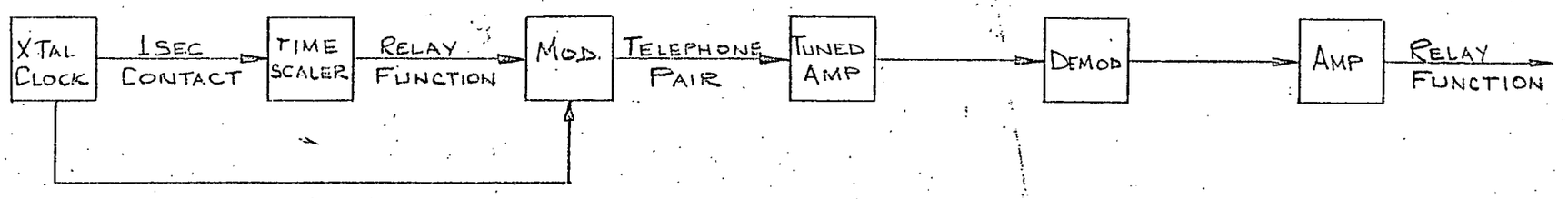


FIGURE 3-12

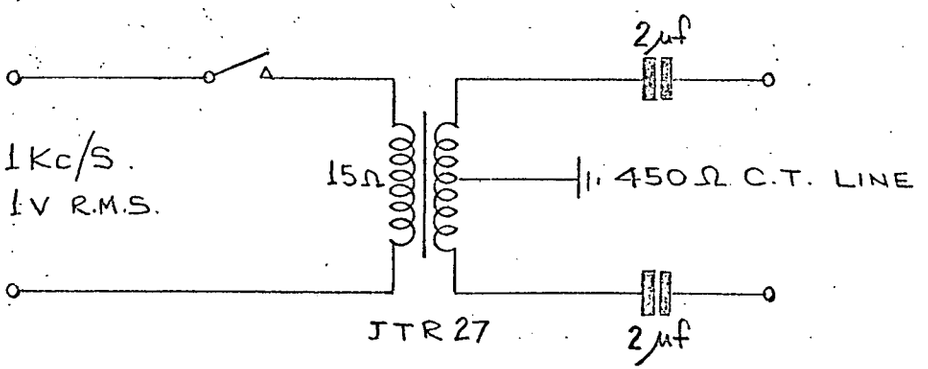
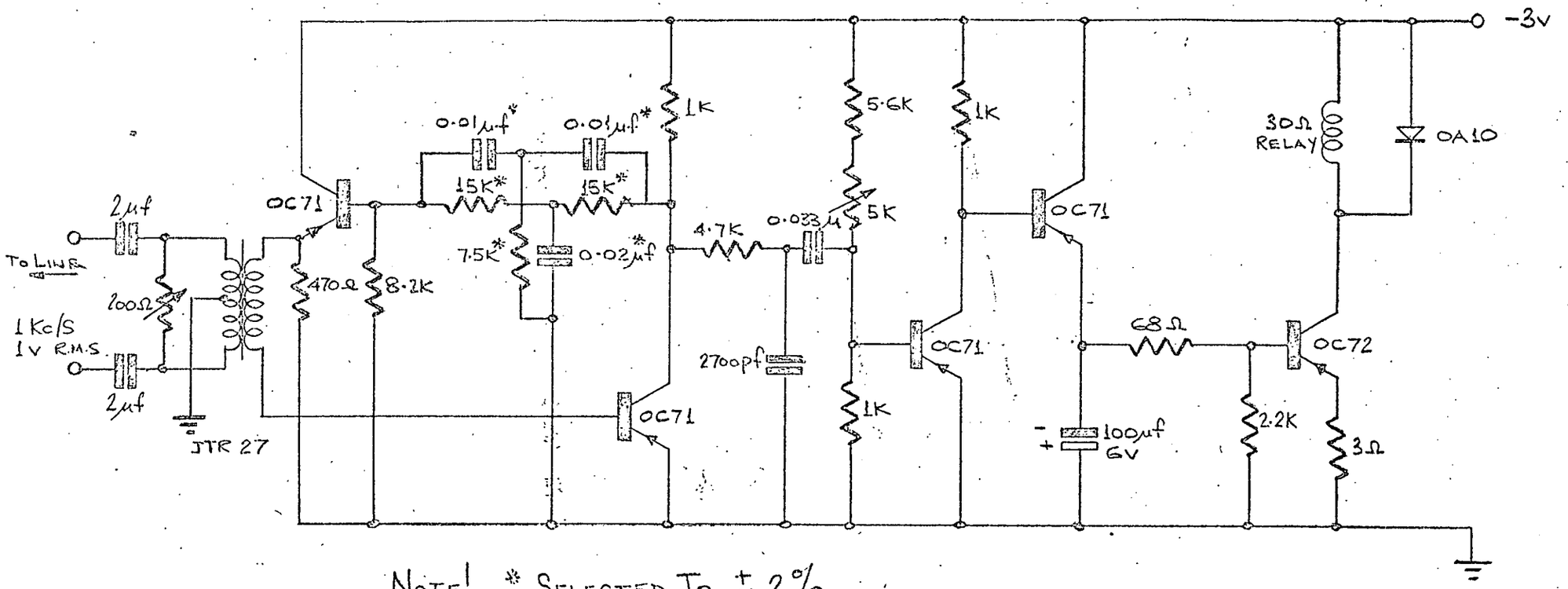


FIGURE 3-13



NOTE! * SELECTED TO ± 2%

FIGURE 3-14

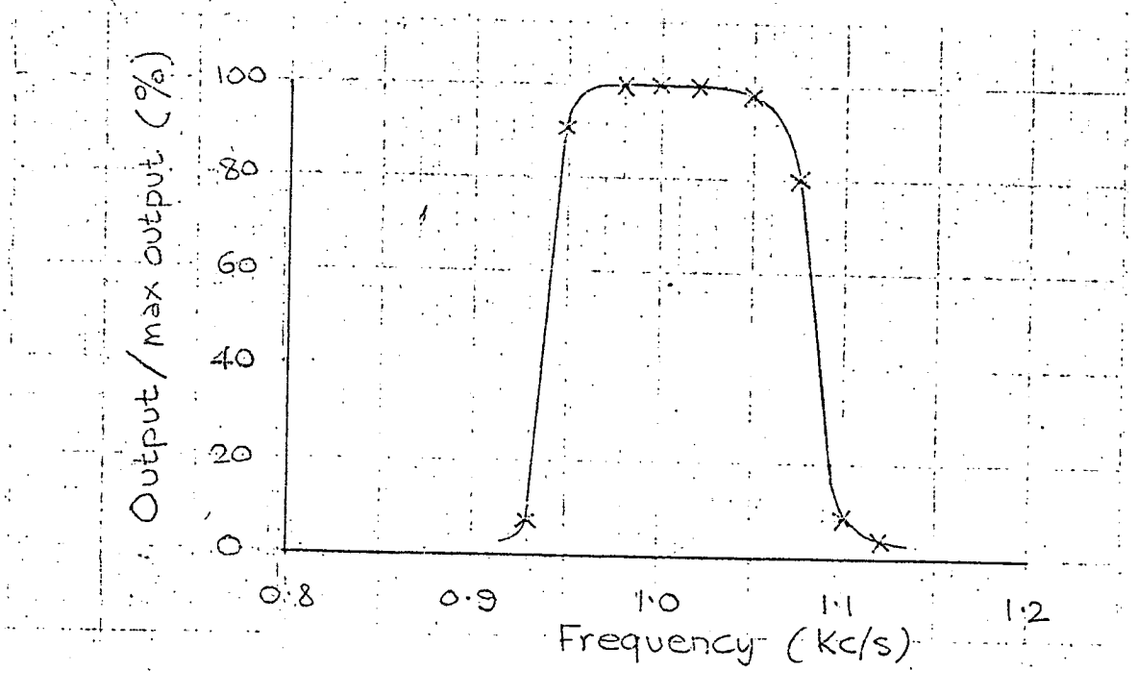


FIGURE 3-15