SWITCHED-CAPACITOR FILTER DESIGN

by

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I hereby declare that, except as stated herein, this thesis contains no material which has been accepted for the award of any other degree or diploma in any university, and that, to the best of my knowledge and belief, this thesis contains no copy or paraphrase of material previously published or written by another person except where due reference is made in the text of the thesis.

(Mohd Alauddin Bin Mohd Ali)

SUMMARY

The switched-capacitor (SC) technique is a very attractive method for implementing fully integrated filters in MOS technology. The filters, consisting only of switches, capacitors and operational amplifiers, can be realised through a number of design procedures. This thesis describes these design techniques and their applications.

Many of the suitable designs use SC integrators which can be easily derived from the analogue active integrators. Parasitic-insensitive implementation is possible realising either the lossless discrete integrator (LDI) or the bilinear transformation. The effects of noise and other non-idealities of the switches and operational amplifiers on these integrators are described. A general biquadratic structure based on the SC integrators is given from which a circuit capable of realising bandpass transfer functions is derived. The SC biquads are cascaded or coupled for the design of higher order filters.

Higher order SC filters are also designed by simulating doubly-terminated LC ladder networks with integrators using the LDI transformation. Other methods of simulating the ladder network include using voltage-controlled current sources, the impedance simulation method and voltage inverter switches. These methods mostly produce circuits which are sensitive to parasitic capacitances and are only briefly described.

These design techniques are used to design SC filters which meet the one-third octave bandpass filter specification required for the analysis of acoustic noise and vibration. The midband frequencies of

the resulting SC bandpass filters can be varied from 10Hz to 20kHz. The designs are made using clock frequency at a minimum value possible and another at 48 times the midband frequency. The suitable circuits are compared with regard to their requirements and performances.

The antialiasing problem due to the wide range of required midband frequencies is overcome with the use of an SC decimator circuit. This allows the antialiasing filter, the decimator and other accessories to be implemented on a single chip with the SC bandpass filter.

The SC circuits are analysed using their z-transform relations. The nodal analysis technique and the equivalent circuit method are described and used for deriving z-transform transfer functions of the SC filters. These are then used to predict the frequency responses of the filters and their sensitivity as to variation of one single capacitor value.

CONTENTS

CHAPTER ONE

INTRODUCTION

Filters for frequency selective filtering are among the most common circuits in electronic systems. With the advent of integrated circuit technology, it has also been desirable to produce filters in monolithic form. Towards this end, filters have been successfully reduced in size and cost with the replacement of RLC networks by active-RC circuits. Avoiding the bulky and costly inductors, thin-film resistors and capacitors can be realised with silicon integrated circuit operational amplifiers. This hybrid integrated circuit can be fitted into a small 16-pin dual-in-line package.

Further reduction by realising resistors and capacitors on the silicon chip together with the operational amplifier (OA) transistors has been found to be unsuitable for implementing precision filters. In order to define accurately the RC product, the absolute values of R and C have to be well controlled which are difficult in current integrated circuit (IC) technology. Integrated resistors have poor linearity and temperature characteristics and they do not track with those of the capacitors on the same chip. However, tracking in variations of the same components allows the possibility of defining resistor or capacitor ratios accurately. Active-R filters have been implemented, which use the OA as integrators with their filter parameters established via resistor ratios.[1]

In metal-oxide-semiconductor (MOS) technology, however, it is more accurate to implement capacitor ratios since high quality capacitors can be conveniently realised in MOS IC. Furthermore, they are less prone to drift and use less silicon area than resistor ratios. Thus active-C filters, which are readily obtained by replacing the resistors in active-R filters

with capacitors, provide a better possibility for full integration of analogue filters.[2]

Another approach for full integration of filters has also been possible due to accurate capacitor ratios and another unique property of MOS IC. The MOS IC offers the ability to store charge on a node for several milliseconds and to sense this stored charge continuously and non-destructively. This feature enables the implementation of analogue sampled-data filters such as the bucket brigade filters [3], the charge-coupled device (CCD) filters [4], the direct-form recursive filters [5] and the switched-capacitor filters (SCFs).[6]

Thus a number of ways have been attempted for the reduction in size and cost of filters. Among these, the switched-capacitor (SC) technique seems to be the most attractive for the implementation of precise fully integrated filters especially in the voice-frequency range. The SCF consists only of capacitors, OAs and analogue switches which are all easily implemented in MOS IC. The filter parameters are determined by capacitor ratios and the frequency at which the switches are clocked. The input signal to the SCF is sampled in time thus it should be bandlimited as dictated by the sampling theorem. Hence an antialiasing filter is required. However, a simple continuous-time filter with no stringent requirement can be easily implemented on the same chip and is usually sufficient for this purpose.

Fully integrated filters have now been implemented in a number of applications using the SC technique. Transmit and Receive Filters for a Pulse-code-modulation (PCM) coder-decoder (CODEC) system have been fabricated together with the CODEC and other interface circuits on the same chip.[7] A Dual Tone Multifrequency (DTMF) receiver can now be

fabricated on a single chip including all its required filter circuits.[8] Programmable SCFs with applications such as in adaptive filters, and speech and music synthesisers, can also be easily implemented due to the filter parameter dependence only on capacitor ratios and clock frequency.[9]

The parameter dependence on the clock frequency allows the possibility of implementing an integrated bandpass filter with fixed capacitor ratios but having its centre frequency tracking the clock frequency. This SC bandpass filter may then be used in applications such as in acoustic noise measurement which involves measuring the level of noise components in different bands of the audio spectrum.[10] The different filters required from the set are obtained by only adjusting the clock frequency of the SC bandpass filter instead of altering the component values as had to be done when using active-RC filters.

This thesis describes the development in SCF designs, their advantages and limitations when compared to active-RC filters or other ways of implementing monolithic filters. A number of techniques have been proposed for the design of SCFs.[11] These techniques are described and applied here for the design of the bandpass filter required for acoustic noise measurement. The requirements and performance of the resulting SCFs are then compared to determine their suitability for integrated circuit implementation.

1.1 Switched-capacitor circuit principle

The above discussions have shown that in order to implement filters in MOS technology, it is desirable for resistors to be avoided. In switched-capacitor (SC) technique, the resistors are replaced by utilising capacitors and switches. Current flow in resistors is simulated by charge transfer

on rapidly switched capacitors. This can be illustrated by the switched-capacitor circuit in fig. 1:1.

Assume the switch is initially at position e, then the capacitor C is charged to voltage v_1. When the switch is thrown to position o, the capacitor C is discharged (or charged) to voltage v_2. The amount of charge that flows into (or from) the voltage source v_2 is $C(v_1 - v_2)$. If the switch is thrown back and forth every T seconds, then the current flow, on the average, is

$$i = \frac{C(v_1 - v_2)}{T} \qquad (1:1)$$

If the switching rate, $f_c = {}^1/_T$ is much larger than the signal frequencies of interest, the sampling time of the signal which occurs in the circuit of fig. 1:1 can be ignored, thus the circuit is equivalent to a resistor of value

$$R = {}^T/_C = {}^1/_{(f_c C)} \qquad (1:2)$$

The MOS implementation of the SC circuit in fig. 1:1 is given in fig. 1:2(a). The two MOSFETs are operated as ideal switches which are controlled by a two-phase non-overlapping clock at the frequency, fc as shown in fig. 1:2(b). The even (e) and odd (o) clock phases, denoted by ϕ_e and ϕ_o respectively, close the switches when they are high. In practice, slightly less than 50% duty cycle is required to ensure the two switches never close simultaneously. However, for simplicity, 50% duty cycle is assumed in subsequent analyses of biphase SCFs.

The SC circuit shown in fig. 1:3 also simulates a resistor as in (1:2). These circuits can thus replace resistors in any active-RC filters to form the SCFs if the assumptions in the above illustration are all satisfied. [12] [13]

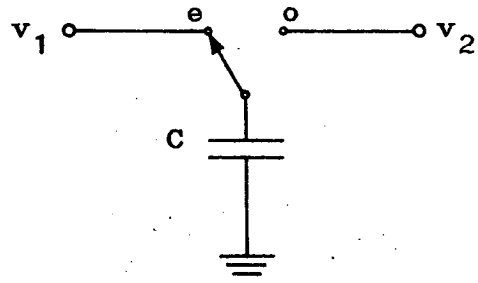

Fig. 1:1 A switched-capacitor circuit simulating a resistor.

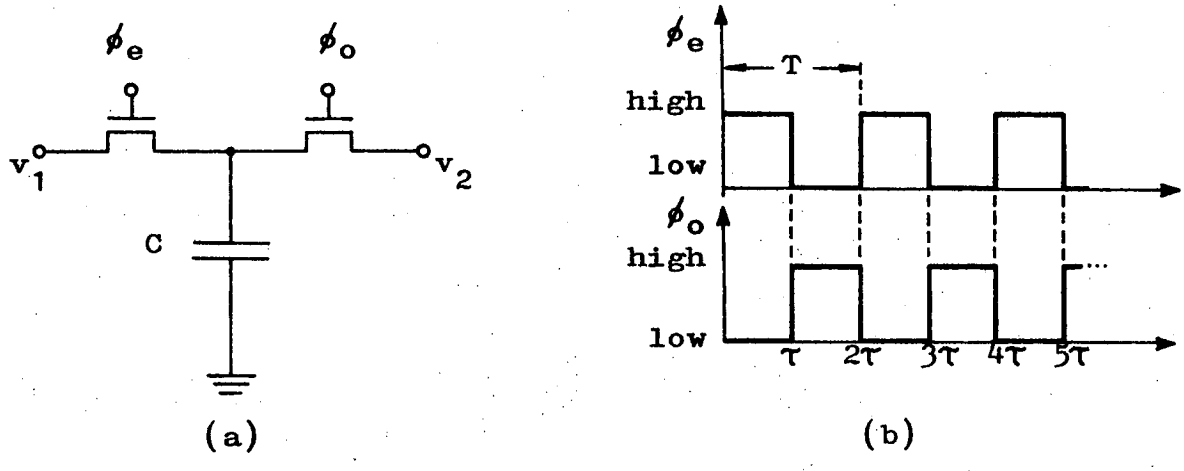

Fig. 1:2 (a) An MOS implementation of circuit in fig. 1:1.
(b) Timing diagram.

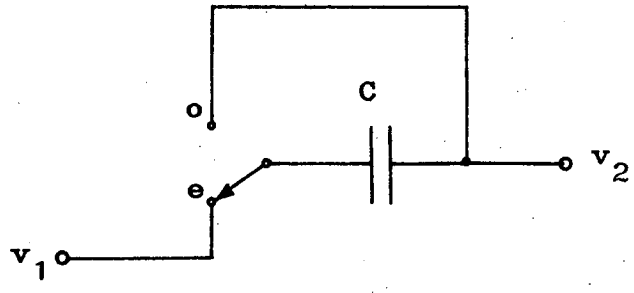

Fig. 1:3 A series switched-capacitor.

Inductors can also be simulated using the simulated resistors, capacitors and OAs, hence passive filter response can also be obtained by an SCF. There are, however, a number of other considerations to be taken into account to ensure that high performance filters are achieved. These are discussed in detail in the following sections.

1.2 Properties of MOS components

As have been mentioned, it is relatively easy to implement capacitors, switches and OAs in the MOS technology. These high quality MOS elements have made the implementation of precise SCF possible. However certain properties of these components do impose some limitations on the range of realisable filters. In this section the properties of these components, produced through the CMOS or NMOS processes, are described.

(a) MOS capacitors

In the NMOS and CMOS processes, capacitor plates can be made of metal (usually aluminium), or polycrystalline silicon (polysilicon), or heavily-doped crystalline silicon. For examples, a heavily doped region in the silicon substrate can be made the bottom plate with the interconnect metallisation made the top plate or both plates can be formed by two polysilicon layers. These materials are very conductive. The dielectric material is SiO_2, an excellent insulator, which can be thermally grown from the silicon layer. These capacitors exhibit good ratio accuracy and low voltage and temperature coefficients.

The value of the capacitors is determined by the dielectric constant, the thickness of the dielectric and the area of the capacitor. Assuming that the dielectric constant and thickness do not vary, the ratio of two capacitors, made within the same integrated circuit, will depend only on

their area ratio. This is primarily determined by the geometrical shape of the capacitors defined by the photolithographic mask used to make the integrated circuit.

Error in the ratio can thus result from uncertainties in the photolithographic edge definition. The possible variation of the dielectric thickness with distance across the integrated circuit can also contribute to errors. These effects can be overcome by careful layout of the components. The errors generally get smaller as the capacitor dimensions are made larger. The achievable ratio accuracies range from 1 - 2% for small capacitor geometries (~ 400μm^2) to about 0.1% for capacitor geometries which approach the limit of economical size (40,000μm^2).[6] This implies that as the capacitor ratio increases the accuracy decreases since the smaller of the two capacitors must be decreasing.

Voltage coefficients of MOS capacitors are in the range of 10 to 100 ppm/V. Temperature coefficients are generally in the range of 20 to 50 ppm/^{o}C. These variations are much lower for the value of a ratio and can be considered insignificant in almost all applications.

The manner in which the capacitor is constructed, as described above, renders parasitic capacitance unavoidable. The bottom plate, which is in the substrate or close to it, is coupled to the substrate by a parasitic capacitance with a value of 5 to 20% of the MOS capacitor itself. The interconnecting lines connected to the top plate causes a parasitic capacitance to be present from the top plate to the substrate. This has a value ranging from 0.1 to 5% of the capacitor. Hence sizeable parasitic capacitances are present and they are non-linear, thus, cannot be neglected if high performance filters are required.[6]

(b) MOS switches

The MOS transistors can operate as good switches. When the transistor is in the off-mode, the off-resistance is, for practical purposes, infinite. The on-resistance depends on the area allowed for the MOS transistor. In NMOS silicon gate technology, switch device with a channel length of 5μm can be achieved. In this case, for a width-to-length ratio of unity, the on-resistance is 5kΩ if the gate drive voltage is 5V with respect to the source. However, in a larger area, 1kΩ on-resistance can readily be attained.

The 5μm device has a leakage current from source and drain to substrate on the order of 10^{-14}A at 70°C. The parasitic capacitances from source and drain to substrate is about 0.020pF each. The overlap capacitance from drain to gate and source to gate is about 0.005pF. The charge induced in the channel, when the gate potential is 5V more positive than the source and drain, is approximately 0.03pC.[6] These properties need to be considered in applications where the switches cannot be assumed ideal.

(c) MOS operational amplifiers

The recent trend towards higher level of integration on MOS Large Scale Integration (LSI) chips has led to considerable works being done in realising CMOS and NMOS OAs. A number of high performance OAs have been designed to date. Operational Amplifiers with up to 90dB open loop gain, unity-gain bandwidth of 10MHz or power dissipation of 2mW are now practical. [11][17]

Typical values, which are easily achievable in both CMOS and NMOS technologies for OAs with ±5V supplies, are 70dB open loop gain, unity-

gain bandwidth of 2MHz and power dissipation of about 3 to 6 mw. The common mode and power supply rejection ratios are about 70dB. The OAs have 0.1% settling time of about 2μs for 1 V step with a 20 pF load and slew rate of about 3V/μs.[14][15] MOS OAs have higher offset voltage and $1/f$ noise than bipolar OAs. The MOS OA dc offset is usually less than 15mv. In the overall filter, this adds up according to the filter configuration and the number of OAs used. A typical input noise versus frequency characteristic of an MOS OA is shown in fig. 1:4.[14]

The MOS OA occupies about as much space as a 50pF capacitor, that is about 0.1 to 0.2 mm^2 of silicon area. It does not require large capacitive and/or resistive loads driving capabilities since OAs used in SCFs are only required to drive small capacitors. Output buffer stage is, however, required for an OA to be used for driving off-chip loads.

1.3 Practical considerations for MOS implementation

The above properties of the MOS elements placed some constraints on the type of SC networks which can be used. A number of circuit conditions have to be avoided in the MOS implementations of precision filters. The guidelines which must be observed for practical SCF configurations are listed below.

(i) Closing the OA feedback path. The OA feedback path should at least be closed by an unswitched capacitor to provide the continuous-time feedback necessary to stabilise the OA. The switched-capacitor alone cannot be used since the OA will be left open-loop during part of the clock cycle. The switched-capacitor can, however, be used in parallel with the unswitched capacitor. It can provide the dc feedback path to prevent latch-up of the OA.

(ii) No capacitor only nodes. All capacitor plates are subject to charge

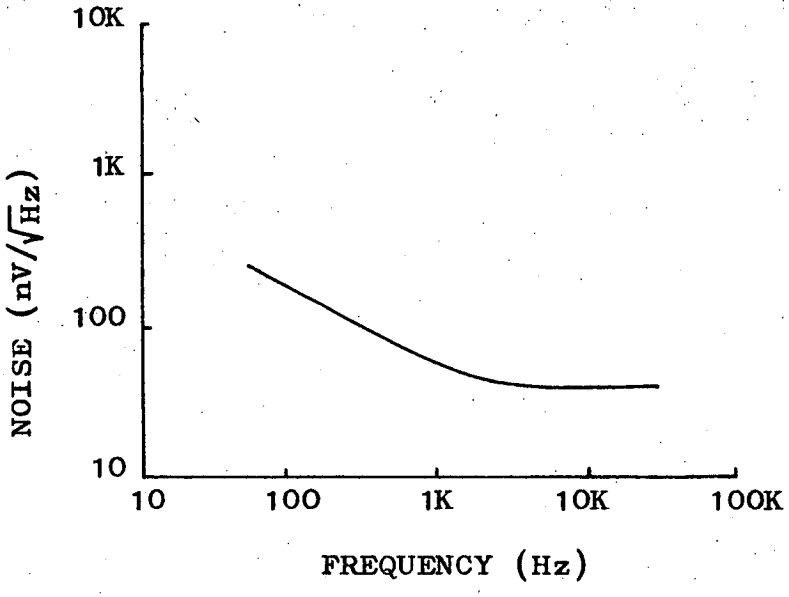

Fig. 1:4 Typical input noise vs frequency characteristic of an MOS operational amplifier.

accumulation from a variety of parasitic sources. In order to insure stability of the circuit there must be a path either directly or through a switched-capacitor from every node to a voltage source or ground.

(iii) Connection of capacitor bottom plate. This plate should be connected to a voltage source/ground or switched between voltage sources/ground. The large non-linear parasitic capacitance between this plate and the substrate will then be charged and discharged, but will not affect the filter response.

(iv) Connection of OA positive input. This input should be connected to a constant voltage. If it is connected to a signal voltage, then the filter response is sensitive to all the parasitic capacitances due to switches, bus lines and substrate that are connected to the negative input of the OA. In addition, increased common-mode performance is required of the OA. [6]

1.4 Further considerations in designing switched-capacitor filters

Despite the above limitations, there are still a variety of possible active filter organisations which can be used for monolithic implementation. These can be arrived at through a number of design procedures starting with an LC ladder or an active-RC filter as a model. These design approaches and the resulting SC circuits differ widely. Certain practical considerations make some of these useful networks preferable to others. The features listed below are among the considerations which can be used to compare the various SCF circuits achievable for a particular specification. [16]

(1) The sensitivity of the transfer function to parasitic capacitances.

(2) The sensitivity to changes of the capacitor values, e.g. caused by fabrication inaccuracies. The tolerance scheme for the filter will

not be violated if a capacitor value, Cj lies between its upper limit, Cjmax and the lower limit, Cjmin. The value

$$\lambda = \frac{Cjmax - Cjmin}{Cj} \times 100\% \qquad (1:3)$$

is used as a measure of the sensitivity of the filter to deviation of one single-capacitor value.

(3) The total capacitance required which reflects on the substrate area needed.

(4) The number of OAs in a circuit which determines the power consumption and the generation of noise. The OA is also a major factor in determining the silicon area required for an SCF.

(5) The spread of the capacitor values which affect the accuracy of capacitor ratio definition in monolithic implementation.

(6) The number of switches.

(7) The number of clock phases required.

(8) The allowable clock frequencies.

Prior to designing the filters, chapter 2 gives two basic analysis techniques which can be used for obtaining z-transform transfer functions of the SCFs. Chapter 3 deals with the SC integrators which are used in many realisable SCFs. Then the specification for the one-third octave bandpass filter is given with some preliminary design steps in chapter 4. Using this specification, SCF designs using SC biquads are done in chapter 5. Designs by simulating the doubly terminated LC ladder networks are done in chapters 6 and 7. Finally, in chapter 8, some aspects for the implementation of the SCFs are discussed.

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CHAPTER TWO

ANALYSIS OF SWITCHED-CAPACITOR NETWORKS

In chapter one, it was shown that a switched-capacitor can approximate a resistor under the assumptions that the sampling frequency is much greater than the signal frequencies and that the resistor is voltage driven at both ends. In this case, the SCF can be considered equivalent to the active-RC filter it replaces and analysed as such. However, such assumptions are not always practical in the analysis of SC networks. For example, it is desirable for the signal frequencies to be as high as half the sampling frequency, thus the time delay through the switched capacitor has to be accounted for.

A more exact analysis can be obtained by applying the z-transform techniques, if the voltage sources and internal voltages of the SC networks are assumed to be sampled at times $k\tau$ (where k is an integer, see fig. 1:2(b)) and held over one-half clock period. The resistor/switched-capacitor correspondence is still useful for deriving topologies of SC networks from the active-RC circuits. Then the SC networks are considered to be pure sampled-data systems and analysed using the z-transform techniques. For this analysis to be exact, the SCF has to be preceded by a sample-and-hold (S/H) stage. However, in many SC networks, this is not necessary since the S/H operations are inherently performed by the SCF.

Without the above assumptions, the SC networks can still be analysed for arbitrary input signals and arbitrary switching patterns where both frequency domain and time domain information can be derived.[1] The analysis, however, is considerably more complex. For convenience or for practical reasons, most SC network designs are based on S/H input signal.

Thus this chapter only deals with the analysis of biphase SC network assuming sampled-and-held inputs. For this class of circuits, simple and fast analysis techniques are available but they only provide for the analytical evaluation of transfer functions and frequency responses of the SC circuits.

2.1 Analysis Techniques

The use of the z-transform in the analysis of SC network is first illustrated here for the SC circuit in fig. 2:1(b) which corresponds to the simple RC circuit of fig. 2:1(a). The resistor of the RC circuit is replaced by the switched-capacitor of fig. 1:1. The SC circuit is assumed to comprise of ideal switches and capacitors. The switches are controlled by clock phases as shown in fig. 1:2(b).

The topology of the SC network is thus changed periodically between two states as shown in fig. 2:1(c) and (d). The port variables can be characterised in terms of discrete time voltages, $v_x(k\tau)$ and discrete time charge variation, $\Delta q_x(k\tau)$, where x represents nodes in the circuit. At the switching time, $k\tau$, when k is even, the SC network becomes that of fig. 2:1(c), and charges are instantaneously redistributed with the principle of charge conservation maintained at every node. Using this principle, nodal charge equations can be written at each node for the even sampling instants. These are

$$\Delta q_1^{e}(k\tau) = C_1 v_1^{e}(k\tau) - C_1 v_2^{o}[(k-1)\tau] \qquad (2:1a)$$

$$\Delta q_2^{e}(k\tau) = C_2 v_2^{e}(k\tau) - C_2 v_2^{o}[(k-1)\tau] \qquad (2:1b)$$

The superscripts e and o differentiate the variables of the two states.

At the switching time, $k\tau$, when k is odd, the network becomes that of fig. 2:1(d) and the nodal charge equations for this instant are

$$\Delta q_1^{\,o}(k\tau) = 0 \qquad (2:1c)$$

$$\Delta q_2^{\,o}(k\tau) = C_1 v_2^{\,o}(k\tau) + C_2 v_2^{\,o}(k\tau) - C_1 v_1^{\,e}[(k-1)\tau] - C_2 v_2^{\,e}[(k-1)\tau] \qquad (2:1d)$$

Applying the z-transform, where $z = \exp(sT)$ in which s is the complex analogue frequency variable and $T = 2\tau$, eqns (2:1) becomes

$$\Delta Q_1^{\,e}(z) = C_1 V_1^{\,e}(z) - z^{-\frac{1}{2}} C_1 V_2^{\,o}(z) \qquad (2:2a)$$

$$\Delta Q_2^{\,e}(z) = C_2 V_2^{\,e}(z) - z^{-\frac{1}{2}} C_2 V_2^{\,o}(z) \qquad (2:2b)$$

$$\Delta Q_1^{\,o}(z) = 0 \qquad (2:2c)$$

$$\Delta Q_2^{\,o}(z) = C_1 V_2^{\,o}(z) + C_2 V_2^{\,o}(z) - z^{-\frac{1}{2}} C_1 V_1^{\,e}(z) - z^{-\frac{1}{2}} C_2 V_2^{\,e}(z) \qquad (2:2d)$$

where $\Delta Q(z)$ and $V(z)$ are z-transforms of $\Delta q(k\tau)$ and $v(k\tau)$ respectively.

Thus at a particular node of the SC network of fig. 2:1(b), two distinct, but coupled, nodal charge equations are required to characterise the charge conservation. Eqn (2:2) can be written in matrix form as follows

$$\begin{bmatrix} \Delta Q_1^{\,e} \\ \Delta Q_2^{\,e} \\ \Delta Q_1^{\,o} \\ \Delta Q_2^{\,o} \end{bmatrix} = \begin{bmatrix} C_1 & 0 & 0 & -z^{-\frac{1}{2}} C_1 \\ 0 & C_2 & 0 & -z^{-\frac{1}{2}} C_2 \\ 0 & 0 & 0 & 0 \\ -z^{-\frac{1}{2}} C_1 & -z^{-\frac{1}{2}} C_2 & 0 & C_1 + C_2 \end{bmatrix} \begin{bmatrix} V_1^{\,e} \\ V_2^{\,e} \\ V_1^{\,o} \\ V_2^{\,o} \end{bmatrix} \qquad (2:3)$$

The transfer functions describing the circuit can be obtained from (2:3) using cofactor techniques. Let [Y] represent the matrix, these transfer functions are

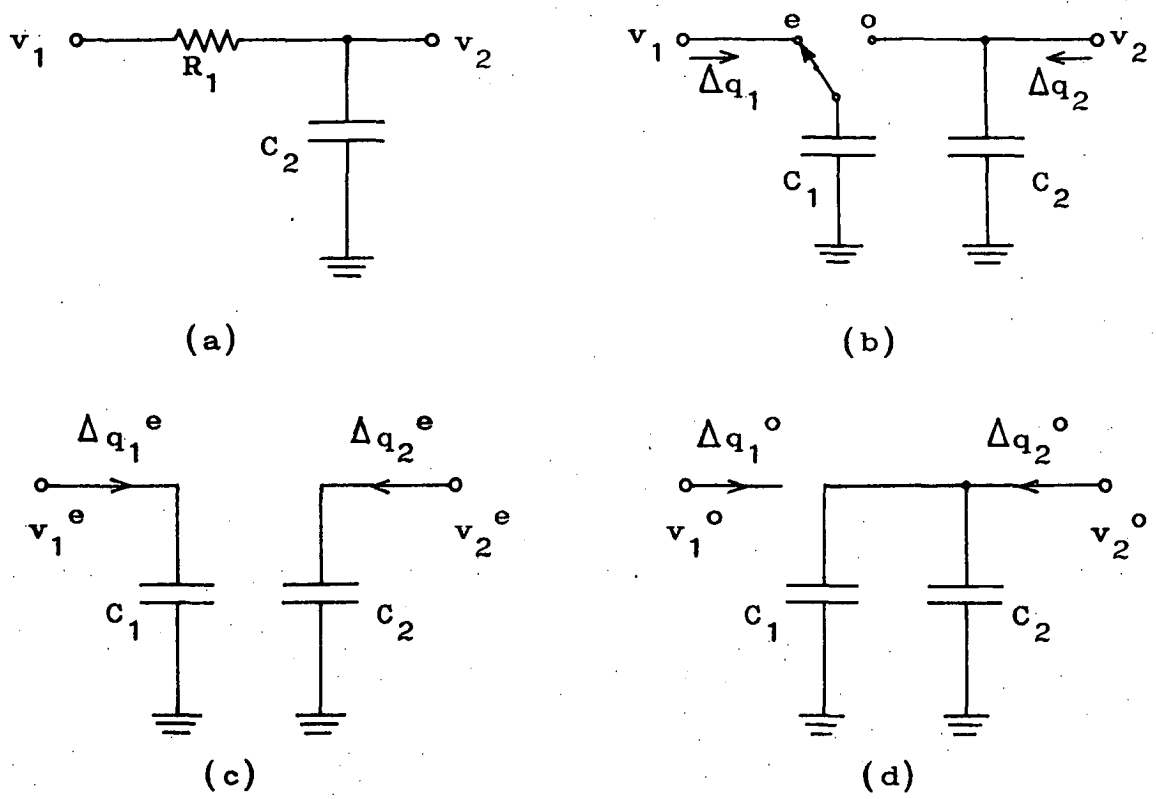


Fig. 2:1 (a) RC circuit. (b) A switched-capacitor network simulating the RC circuit. (c) network (b) during the even clock phase. (d) network (b) during the odd clock phase.

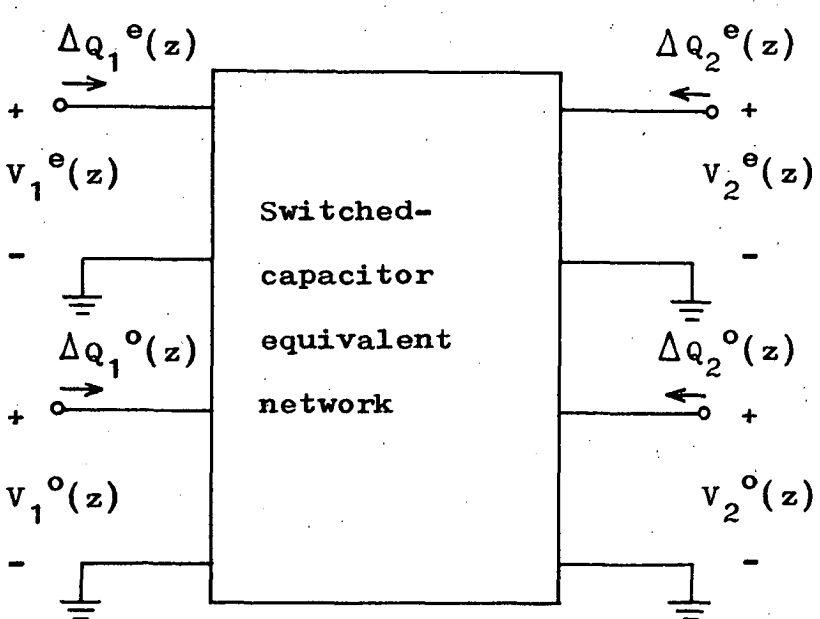


Fig.2:2 Four-port equivalent of a two-port switched capacitor network.

$$H^{ee} = \frac{V_2^e}{V_1^e} = \frac{|Y_{12}|}{|Y_{11}|} = \frac{C_1 z^{-1}}{C_1 + C_2 - C_2 z^{-1}} \qquad (2:4a)$$

$$H^{eo} = \frac{V_2^o}{V_1^e} = \frac{|Y_{14}|}{|Y_{11}|} = \frac{C_1 z^{-\frac{1}{2}}}{C_1 + C_2 - C_2 z^{-1}} \qquad (2:4b)$$

$$H^{oe} = \frac{V_2^e}{V_1^o} = \frac{|Y_{32}|}{|Y_{33}|} = 0 \qquad (2:4c)$$

$$H^{oo} = \frac{V_2^o}{V_1^o} = \frac{|Y_{34}|}{|Y_{33}|} = 0 \qquad (2:4d)$$

The SC network is thus fully characterised by the input-output relation,

$$\begin{bmatrix} V_2^e(z) \\ V_2^o(z) \end{bmatrix} = \begin{bmatrix} H^{ee} & H^{oe} \\ H^{eo} & H^{oo} \end{bmatrix} \begin{bmatrix} V_1^e(z) \\ V_1^o(z) \end{bmatrix} \qquad (2:5a)$$

where

$$V_1(z) = V_1^e(z) + V_1^o(z) \qquad (2:5b)$$

$$V_2(z) = V_2^e(z) + V_2^o(z) \qquad (2:5c)$$

The SC network can then also be represented by an equivalent four-port as shown in fig. 2:2 where the equivalent z-domain network is described by (2:5a) or (2:3).

Signal conditioning performed at the input and output determines the relevant transfer function relations of the SC network. As an example, if the output is sampled only at the even $k\tau$ time instants, then the relevant relation is

$$V_2^e(z) = H^{ee} V_1^e(z) + H^{oe} V_1^o(z) \qquad (2:6)$$

In the circuit of fig. 2:1(b), however, the input at the odd $k\tau$ time instants is not sampled, thus for this case only the transfer function H^{ee} is involved.

If a general SC network is now considered, the two z-transformed nodal charge equations at a particular node x are written as

$$\Delta Q^{e}_{x}(z) = \sum_{j=1}^{Nex} Q^{e}_{xj}(z) - z^{-\frac{1}{2}} \sum_{j=1}^{Nex} Q^{o}_{xj}(z) \qquad (2:7a)$$

$$\Delta Q^{o}_{x}(z) = \sum_{j=1}^{Nox} Q^{o}_{xj}(z) - z^{-\frac{1}{2}} \sum_{j=1}^{Nox} Q^{e}_{xj}(z) \qquad (2:7b)$$

where Nex, Nox denote the total number of capacitors connected to node x during the even and odd clock phases respectively. $Q^{e}_{xj}(z)$, $Q^{o}_{xj}(z)$ are z-transforms of the instantaneous charges stored on the j-th capacitor connected to node x at the even and odd $k\tau$ time instants respectively.

As the circuit increases in complexity, it becomes very difficult to write down (2:7). The transfer functions as in (2:5a) can no longer be easily obtained as for the case of the simple circuit of fig. 2:1(b). A number of analysis techniques have been proposed which simplify these steps. The following sections deal with two basic methods which are capable of handling any two-phase SC network containing ideal elements with S/H inputs. These are the nodal analysis technique [2] and the equivalent circuit method.[8] Based on these, more general methods have been developed but the following sections only elaborate them in their simplest forms.

2.2 Nodal Analysis Technique

Using (2:7), the total number of equations involved to describe a SC network is 2n, where n is the number of nodes in the network. In this nodal analysis technique, the network is broken down into switches and capacitors networks. Using matrices which describe these networks, equations such as in (2:7) can be assembled in a logical manner. This method is particularly attractive for computer analysis of SC networks.

In this analysis, it is first assumed that any branch between two nodes in the network consists only of a capacitor and a switch. Thus another node has to be introduced for the circuit of fig. 2:1(b) for its analysis using this method. The circuit is redrawn in fig. 2:3 broken down into its switches and capacitors networks with the nodes renumbered. In this way, the same capacitors are connected to each node at all time instants. Thus, from fig. 2:3(b), a fixed capacitance matrix can be written as follows,

$$[C] = \begin{bmatrix} 0 & 0 & 0 \\ 0 & C_1 & 0 \\ 0 & 0 & C_2 \end{bmatrix} \qquad (2:8)$$

The voltage at each node is determined by the switch connection. Thus when switch e closes, taking V_1^e as the reference in fig. 2:3(a),

$$V_1^e = V_1^e \ , \ V_2^e = V_1^e \ , \ V_3^e = V_3^e \qquad (2:9)$$

These can be written in matrix form as

$$\begin{bmatrix} V_1^e \\ V_2^e \\ V_3^e \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_1^e \\ V_2^e \\ V_3^e \end{bmatrix} = [S^e]V^e \qquad (2:10)$$

where $[S^e]$ is the even switching matrix and V^e is the corresponding vector of the voltages at the nodes of the circuit. Similarly, when switch o closes, the switching matrix $[S^o]$ can be obtained and the corresponding vector V^o defined as

$$[S^o] = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 1 \end{bmatrix}, \quad V^o = \begin{bmatrix} V_1^o \\ V_2^o \\ V_3^o \end{bmatrix} \qquad (2:11)$$

Equations such as in (2:7) can then be written in matrix form as follows

$$\begin{bmatrix} \Delta\hat{Q}^e \\ \Delta\hat{Q}^o \end{bmatrix} = \begin{bmatrix} [C] & [0] \\ [0] & [C] \end{bmatrix} \begin{bmatrix} [S^e] & -z^{-\frac{1}{2}}[S^o] \\ -z^{-\frac{1}{2}}[S^e] & [S^o] \end{bmatrix} \begin{bmatrix} V^e \\ V^o \end{bmatrix} \qquad (2:12)$$

where, due to the different node definition, $\Delta\hat{Q}(z)$ is now used to denote the z-transformed charge variation. $\Delta\hat{Q}^e$ and $\Delta\hat{Q}^o$ are vectors of the z-transformed charge variations at nodes of the network when switches e and o close, respectively.

The closing of the switches reduces the actual number of nodes in the circuit. This has to be taken into account by using the charge matrices $[I^e]$ and $[I^o]$ for the even and odd $k\tau$ time instants respectively. When switch e closes in fig. 2:3, the actual charge variation at the combined node is the combination of $\Delta\hat{Q}_1$ and $\Delta\hat{Q}_2$ which have been assumed to be present on nodes 1 and 2 separately. Thus taking node 1 as reference, the combined charge variations are

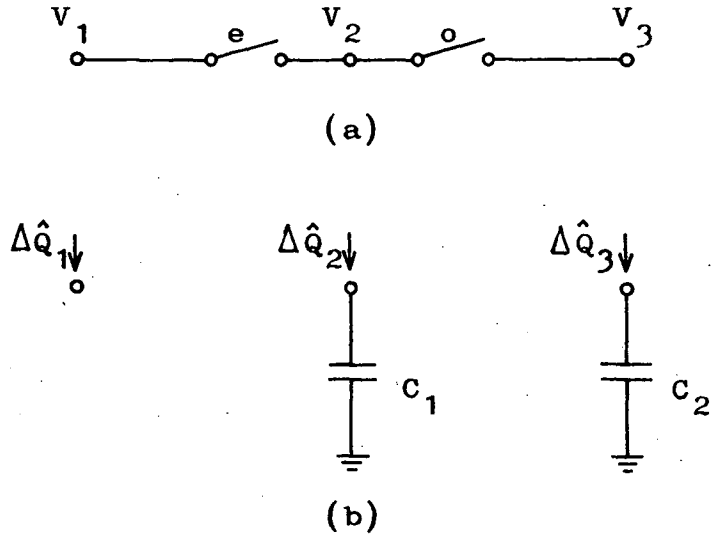
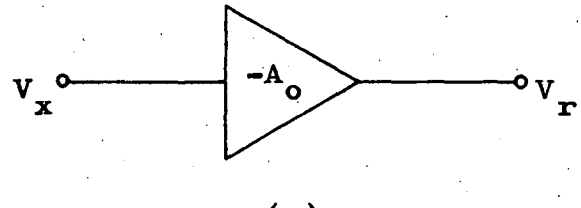


Fig. 2:3 (a) Switches network of the circuit in fig. 2:1(b). (b) Its capacitors network.



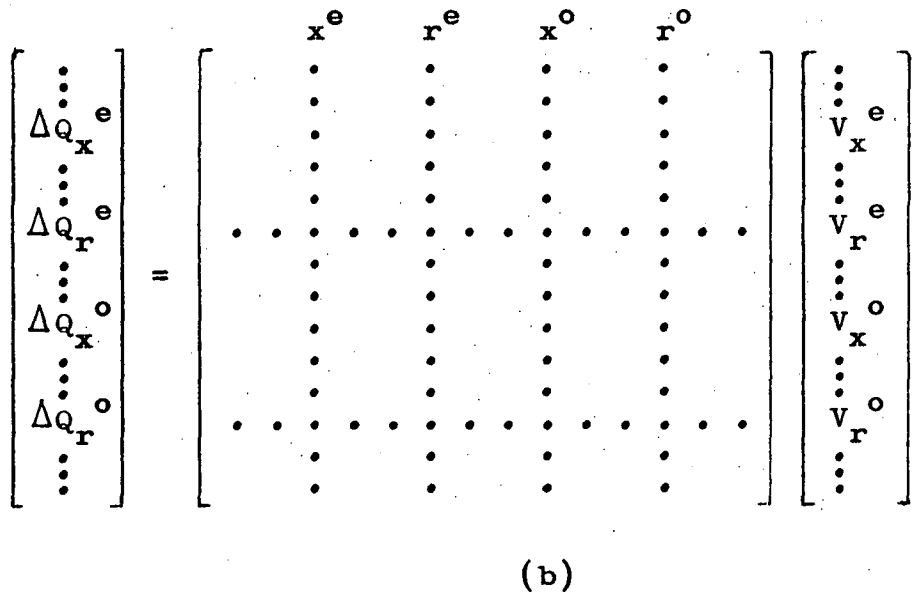


Fig. 2:4 (a) An ideal voltage amplifier between nodes x and r in a switched-capacitor network. (b) The matrix [Y] showing the affected rows and columns with the inclusion of the amplifier.

$$\Delta Q_1^{\,e} = \Delta\hat{Q}_1^{\,e} + \Delta\hat{Q}_2^{\,e}\ ,\ \Delta Q_2^{\,e} = 0 \qquad (2{:}13a)$$

and since switch o is open at this instant,

$$\Delta Q_3^{\,e} = \Delta\hat{Q}_3^{\,e} \qquad (2{:}13b)$$

These are written in matrix form as

$$\Delta Q^e = \begin{bmatrix} \Delta Q_1^{\,e} \\ \Delta Q_2^{\,e} \\ \Delta Q_3^{\,e} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \Delta\hat{Q}_1^{\,e} \\ \Delta\hat{Q}_2^{\,e} \\ \Delta\hat{Q}_3^{\,e} \end{bmatrix} = [I^e]\,\Delta\hat{Q}^e \qquad (2{:}14)$$

Similarly when switch o closes, the matrix equation is

$$\Delta Q^o = \begin{bmatrix} \Delta Q_1^{\,o} \\ \Delta Q_2^{\,o} \\ \Delta Q_3^{\,o} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} \Delta\hat{Q}_1^{\,o} \\ \Delta\hat{Q}_2^{\,o} \\ \Delta\hat{Q}_3^{\,o} \end{bmatrix} = [I^o]\,\Delta\hat{Q}^o \qquad (2{:}15)$$

Hence, in general, all the nodal charge equations can be assembled in matrix form as follows [2], using (2:12), (2:14) and (2:15);

$$\begin{bmatrix} \Delta Q^e \\ \Delta Q^o \end{bmatrix} = \begin{bmatrix} [I^e][C][S^e] & -z^{-\frac{1}{2}}[I^e][C][S^o] \\ -z^{-\frac{1}{2}}[I^o][C][S^e] & [I^o][C][S^o] \end{bmatrix} \begin{bmatrix} V^e \\ V^o \end{bmatrix} \qquad (2{:}16)$$

or

$$\Delta Q = [Y]V$$

For the circuit of fig. 2:1(b), the same matrix equation as in (2:3) is obtained after elimination of rows and columns of the matrix [Y] which are zero, and their corresponding variables.

The switches and capacitors have been assumed ideal. The presence of parasitic capacitance can, however, be easily incorporated in the analysis. The analysis can also accommodate the presence of an ideal voltage amplifier with gain, $-A_o$ as shown in fig. 2:4(a) connected between

nodes x and r. The voltages at the nodes are related by

$$V_x^e = -\frac{V_r^e}{A_o} \quad , \quad V_x^o = -\frac{V_r^o}{A_o} \qquad (2:17)$$

The matrix [Y] is shown in fig. 2:4(b) showing only variables, rows and columns of the relevant nodes. Using (2:17), column x^e of the matrix is divided by A_o and subtracted from column r^e and column x^e is discarded. Similar steps are done for columns x^o and r^o. The rows involving $\Delta Q^e{}_r$ and $\Delta Q^o{}_r$ are also discarded since they express the current outputs from a voltage source and thus are redundant. When $A_o \to \infty$ for an ideal OA, these steps merely involve discarding columns x^e, x^o and rows involving $\Delta Q^e{}_r$, $\Delta Q^o{}_r$. [3]

Thus normally the matrix [Y] can be reduced to at most a 4 x 4 matrix as in (2:3). If necessary, pivotal condensation can be applied to reduce the matrix. Then, after considering the signal conditioning to the SC network, cofactor techniques are used as before to derive the relevant transfer functions of the network.

This technique can be extended for the analysis of multiphase SC networks [4] and SC network using amplifier with finite gain and finite bandwidth. [5] Computer programs for the analysis of SC networks based on this technique have been implemented. However, most computer-aided-design (CAD) programs use the more efficient modified nodal analysis (MNA) techniques for the computation of SC network. [6][7]

2.3 Equivalent Circuit Method

This method involves deriving simple z-domain equivalent circuits or building blocks for several elements of the SC network using the

z-transformed nodal charge equations as in (2:7). Any SC network can then be transformed into a z-domain equivalent circuit by interconnecting the appropriate building blocks. It is then possible to apply familiar network analysis techniques on the SC network equivalent circuit to derive the transfer relations between any pair of nodes of the network. This method is appealing from the practical insight view.

The circuit shown in fig. 2:5 is the most general switched (single) capacitor element. Other SC elements are specific cases of its configuration. Thus only its equivalent circuit needs to be derived directly from the z-transformed nodal charge equations. By manipulating this equivalent circuit, the other useful SC building blocks can then be derived. These blocks, together with the equivalent circuits for independent and voltage-controlled voltage sources form a library of building blocks which can be used for both the analysis and synthesis of biphase SC networks.[8][9] This method of analysis has also been extended so that it can be applicable for multiphase SC network [10] and biphase SC network with continuous input signals, and duty cycle not equal to 50%.[11]

The z-transformed nodal charge equations for the toggle-switched floating four-port (TSFFP) in fig. 2:5 can be written as follows

$$\Delta Q_1^{e}(z) = CV_1^{e}(z) - CV_2^{e}(z) - Cz^{-\frac{1}{2}}V_3^{o} + Cz^{-\frac{1}{2}}V_4^{o} \quad (2:18a)$$

$$\Delta Q_1^{o}(z) = 0 \quad (2:18b)$$

$$\Delta Q_2^{e}(z) = CV_2^{e}(z) - CV_1^{e}(z) - Cz^{-\frac{1}{2}}V_4^{o} + Cz^{-\frac{1}{2}}V_3^{o} \quad (2:18c)$$

$$\Delta Q_2^{o}(z) = 0 \quad (2:18d)$$

$$\Delta Q_3^{e}(z) = 0 \quad (2:18e)$$

$$\Delta Q_3^{o}(z) = CV_3^{o}(z) - CV_4^{o}(z) - Cz^{-\frac{1}{2}}V_1^{e} + Cz^{-\frac{1}{2}}V_2^{e} \quad (2:18f)$$

$$\Delta Q_4^{e}(z) = 0 \quad (2:18g)$$

$$\Delta Q_4^{o}(z) = CV_4^{o}(z) - CV_3^{o}(z) - Cz^{-\frac{1}{2}}V_2^{e} + Cz^{-\frac{1}{2}}V_1^{e} \quad (2:18h)$$

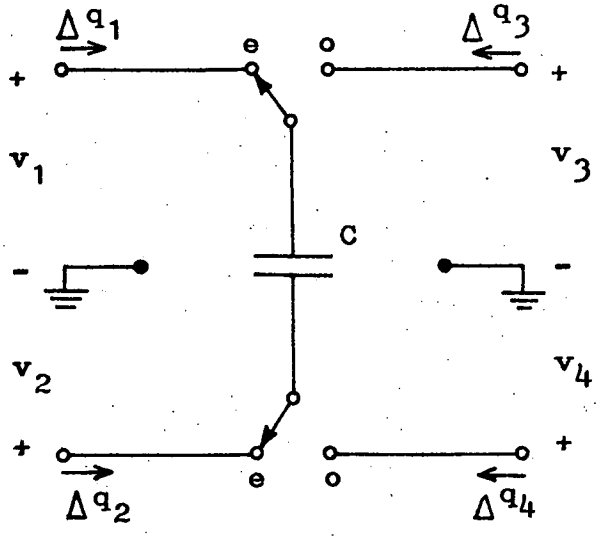


Fig. 2:5 Toggle-switched floating four-port. [8]

Equation (2:18) describes an eight-port equivalent circuit with four open ports. These open ports can be deleted and the remaining equations in (2:18) are used to derive the four-port equivalent circuit shown in fig. 2:6(a) for the TSFFP. Note that the even (e) and odd (o) phases are interchangeable on the SC circuit, i.e. if the capacitor in fig. 2:5 is connected to V_1 and V_2 during the o phase and to V_3 and V_4 during the e phase, then the equivalent circuit is obtained by interchanging the superscripts of the variables of the equivalent circuit in fig. 2:6(a).

The TSFFP is equivalent to the floating capacitor in fig. 2:6(b) if $V_3 = V_1$ and $V_4 = V_2$. Thus the equivalent circuit for the floating capacitor can be derived from that of the TSFFP by making similar replacement of the subscripts for its variables. The toggle-switched capacitor of fig. 2:6(c) can be obtained by grounding $V_2$and V_4 of the TSFFP. Thus the corresponding equivalent circuit is similarly obtained. The series-switched capacitor of fig. 2:6(d) is obtained by shorting V_3 and V_4 of the TSFFP and its equivalent circuit is as shown. Other SC z-domain equivalent circuits can similarly be derived.

The independent voltage source and its corresponding equivalent circuit is shown in fig. 2:7(a), where the voltage source is split into two for the even and odd phases. The equivalent circuit for the full cycle sampled-and-held independent voltage source, the voltage controlled voltage source and the ideal OA are shown in fig. 2:7(b), (c) and (d) respectively. Thus fig. 2:6 and fig. 2:7 give a sample of equivalent circuits which are often used, from the library of z-domain equivalent circuits for switched-capacitor building blocks.[8] From these equivalent circuits, the SC network of fig. 2:1(b), for example, can be analysed

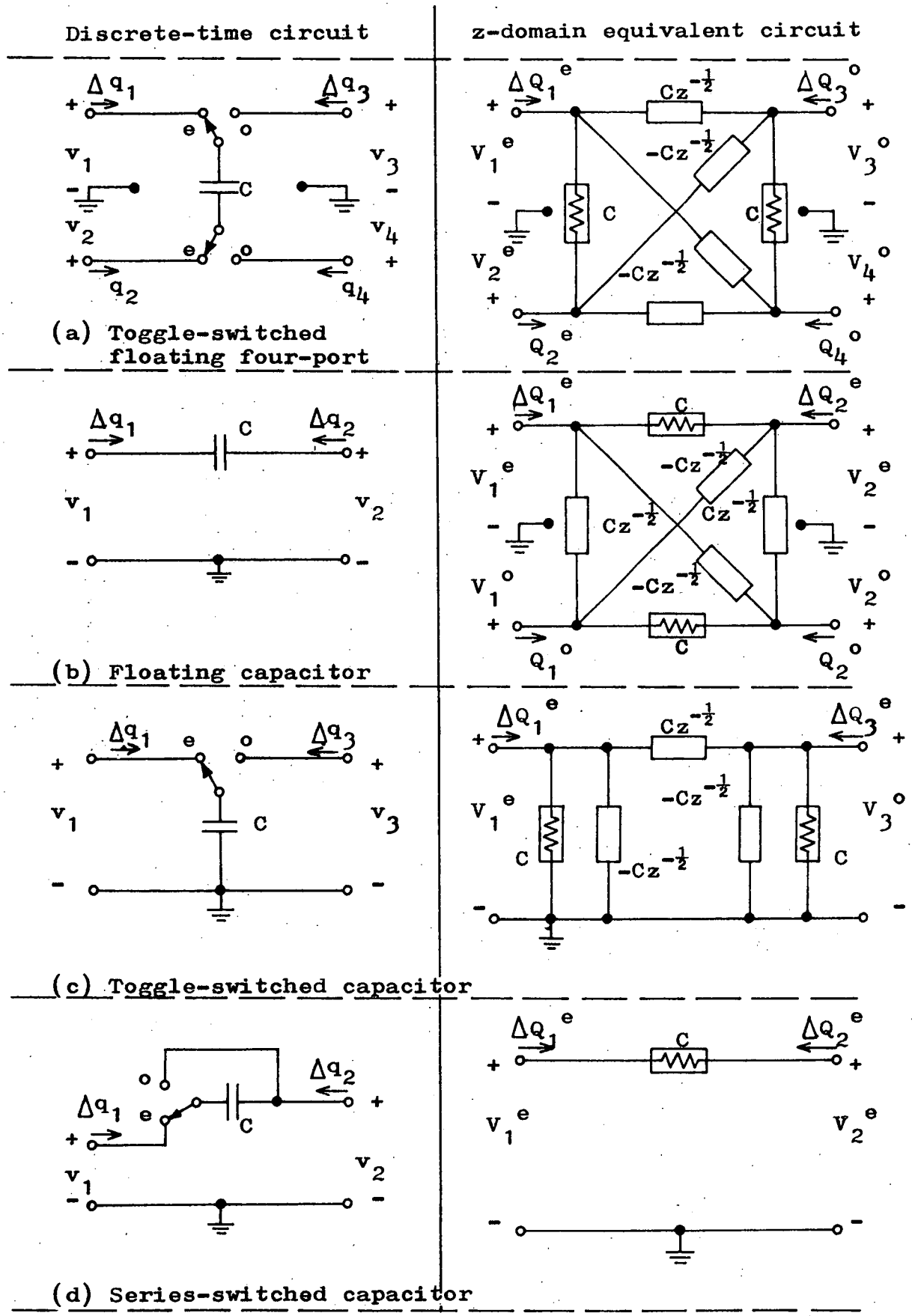


Fig. 2:6 z-domain equivalent circuits for switched-capacitor elements

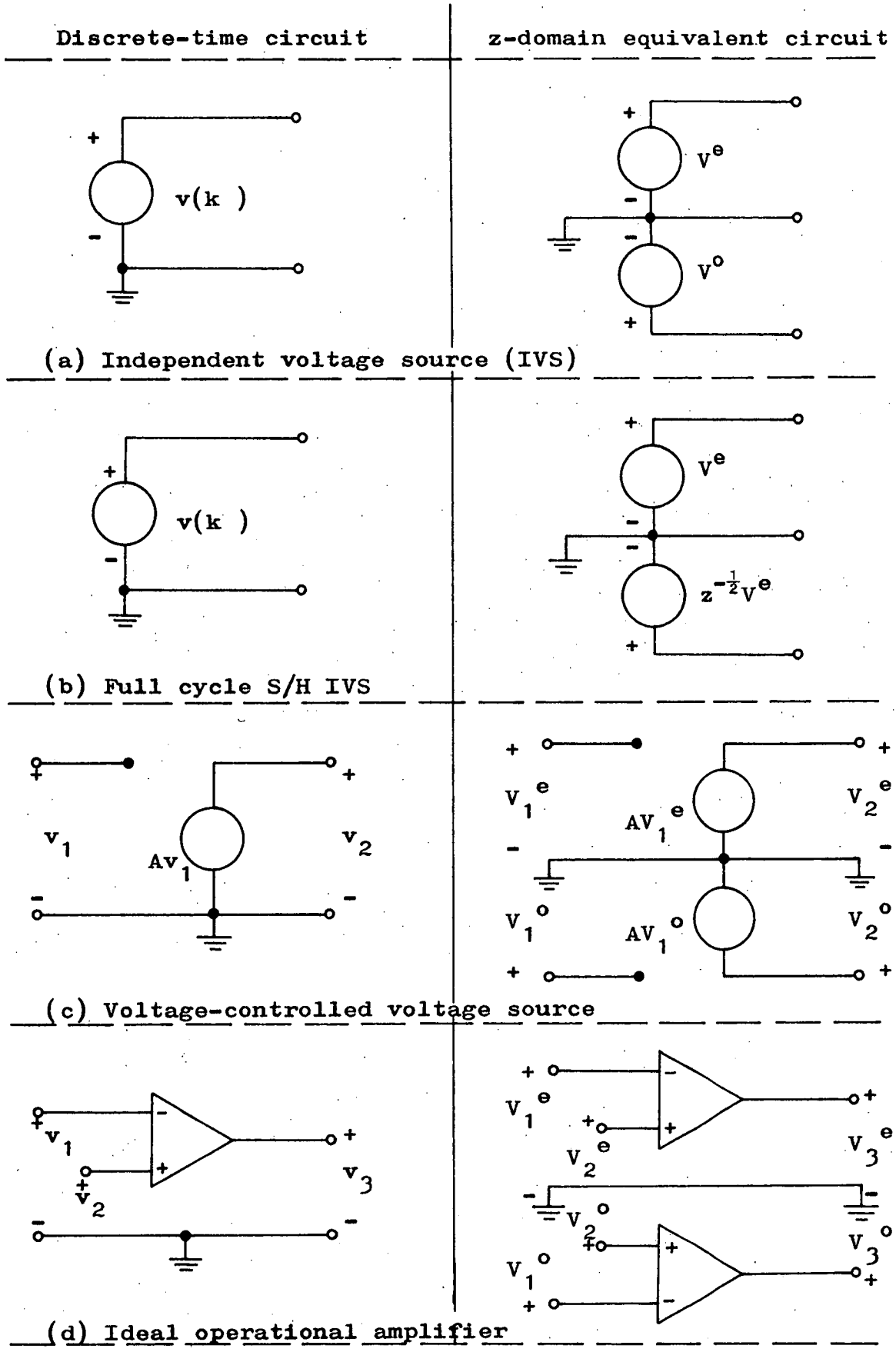


Fig. 2:7 z-domain equivalent circuits for voltage sources.

by appropriately interconnecting the blocks in fig. 2:6(b) and (c), and the source in fig. 2:7(a).

2.4 Examples

The SC network shown in fig. 2:8 will be used to further demonstrate the two methods of analyses described. The network is actually a circuit for the switched-capacitor integrator (SCI) as will be shown in chapter 3. The relevant transfer functions as defined in (2:5) for this circuit are derived.

1. Deriving transfer functions using nodal analysis technique.

The circuit in fig. 2:8 has its nodes numbered as shown. The switches and capacitors networks of the circuit can then be drawn separately as in fig. 2:9. From fig. 2:9(a), the following matrices can be written

$$[S^e] = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \qquad [S^o] = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

(2:19)

$$[I^e] = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \qquad [I^o] = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

From fig. 2:9(b), the capacitor matrix is

$$[C] = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & C_1 & 0 & 0 \\ 0 & 0 & C_2 & -C_2 \\ 0 & 0 & -C_2 & C_2 \end{bmatrix} \qquad (2:20)$$

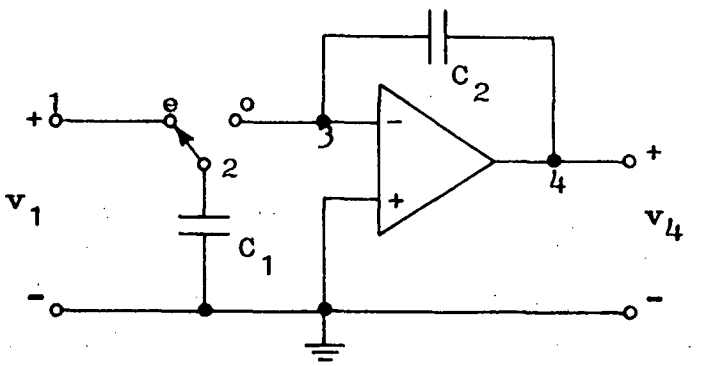


Fig. 2:8 A switched-capacitor integrator.

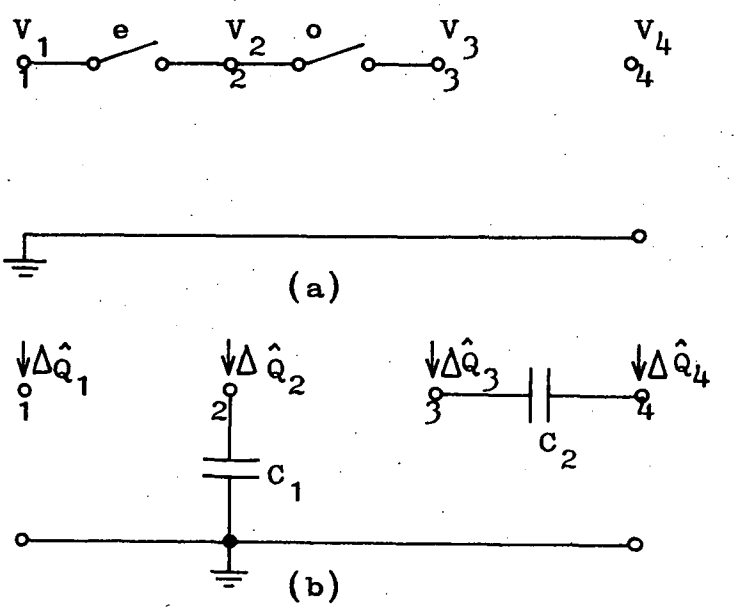


Fig. 2:9 (a) Switches network of the switched-capacitor integrator. (b) Capacitors network of the switched-capacitor integrator.

Putting (2:19) and (2:20) in (2:16), the following matrix equation is obtained,

$$\begin{bmatrix} \Delta Q_1^e \\ \Delta Q_2^e \\ \Delta Q_3^e \\ \Delta Q_4^e \\ \Delta Q_1^o \\ \Delta Q_2^o \\ \Delta Q_3^o \\ \Delta Q_4^o \end{bmatrix} = \begin{bmatrix} C_1 & 0 & 0 & 0 & 0 & 0 & -z^{-\frac{1}{2}}C_1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & C_2 & -C_2 & 0 & 0 & -z^{-\frac{1}{2}}C_2 & z^{-\frac{1}{2}}C_2 \\ 0 & 0 & -C_2 & C_2 & 0 & 0 & z^{-\frac{1}{2}}C_2 & -z^{-\frac{1}{2}}C_2 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -z^{-\frac{1}{2}}C_1 & 0 & -z^{-\frac{1}{2}}C_2 & z^{-\frac{1}{2}}C_2 & 0 & 0 & C_1+C_2 & -C_2 \\ 0 & 0 & z^{-\frac{1}{2}}C_2 & -z^{-\frac{1}{2}}C_2 & 0 & 0 & -C_2 & C_2 \end{bmatrix} \begin{bmatrix} V_1^e \\ V_2^e \\ V_3^e \\ V_4^e \\ V_1^o \\ V_2^o \\ V_3^o \\ V_4^o \end{bmatrix} \qquad (2:21)$$

The zero columns and rows of the matrix in (2:21) can be eliminated. Also, the presence of the ideal OA between nodes 3 and 4 makes it possible to discard columns 3 (even), 3 (odd) and rows 4 (even), 4 (odd). Thus the reduced matrix equation is

$$\begin{bmatrix} \Delta Q_1^e \\ \Delta Q_3^e \\ \Delta Q_3^o \end{bmatrix} = \begin{bmatrix} C_1 & 0 & 0 \\ 0 & -C_2 & z^{-\frac{1}{2}}C_2 \\ -z^{-\frac{1}{2}}C_1 & z^{-\frac{1}{2}}C_2 & -C_2 \end{bmatrix} \begin{bmatrix} V_1^e \\ V_4^e \\ V_4^o \end{bmatrix} \qquad (2:22)$$

Note that V_1^o is absent in (2:22) since the input is only sampled during the even clock phase. The relevant transfer functions of the SCI are

$$H^{ee} = \frac{V_4^e}{V_1^e} = \frac{|Y_{12}|}{|Y_{11}|} = \frac{-C_1 z^{-1}}{C_2(1 - z^{-1})} \qquad (2:23a)$$

$$H^{eo} = \frac{V_4^o}{V_1^e} = \frac{|Y_{13}|}{|Y_{11}|} = \frac{-C_1 z^{-\frac{1}{2}}}{C_2(1 - z^{-1})} \qquad (2:23b)$$

2. Deriving transfer functions using equivalent circuit method.

By properly interconnecting the SC building blocks of fig. 2:6(b), (c) and fig. 2:7(a),(d), the SCI in fig. 2:8 is transformed into its z-domain equivalent circuit shown in fig. 2:10(a). This can be simplified by removing elements shunting virtual ground points and voltage sources. The simplified circuit is shown in fig. 2:10(b) which can be reconfigured into the circuit in fig. 2:10(c).[8] The relevant transfer functions can then be easily obtained to be

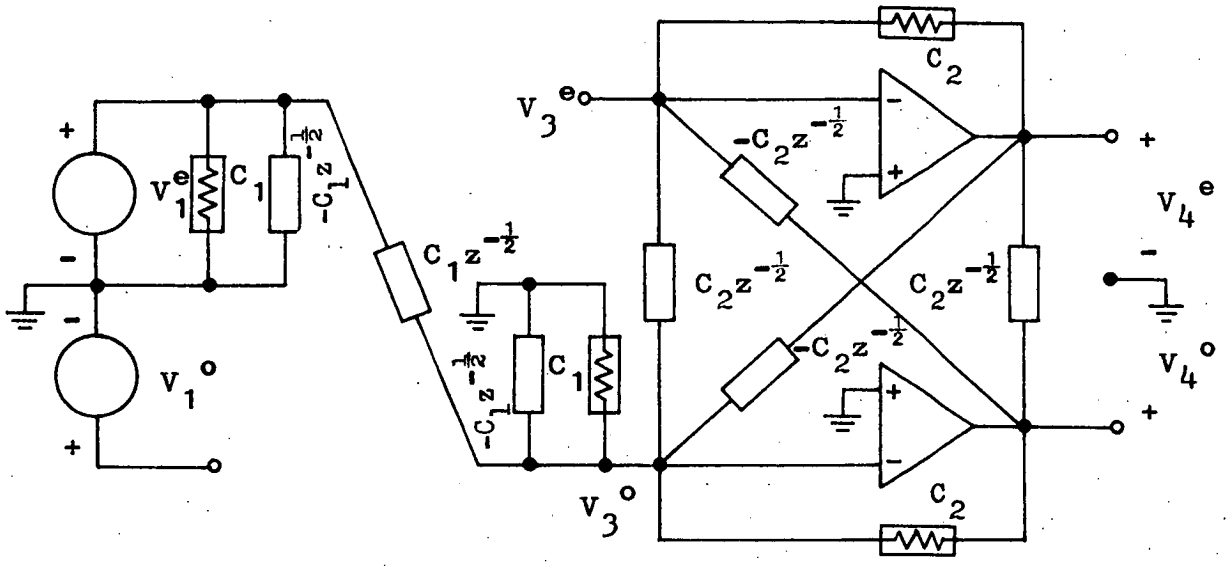
$$H^{ee} = \frac{V_4^e}{V_1^e} = -\frac{C_1 z^{-1}}{C_2(1 - z^{-1})} \qquad (2:24a)$$

$$H^{eo} = \frac{V_4^o}{V_1^e} = -\frac{C_1 z^{-\frac{1}{2}}}{C_2(1 - z^{-1})} \qquad (2:24b)$$

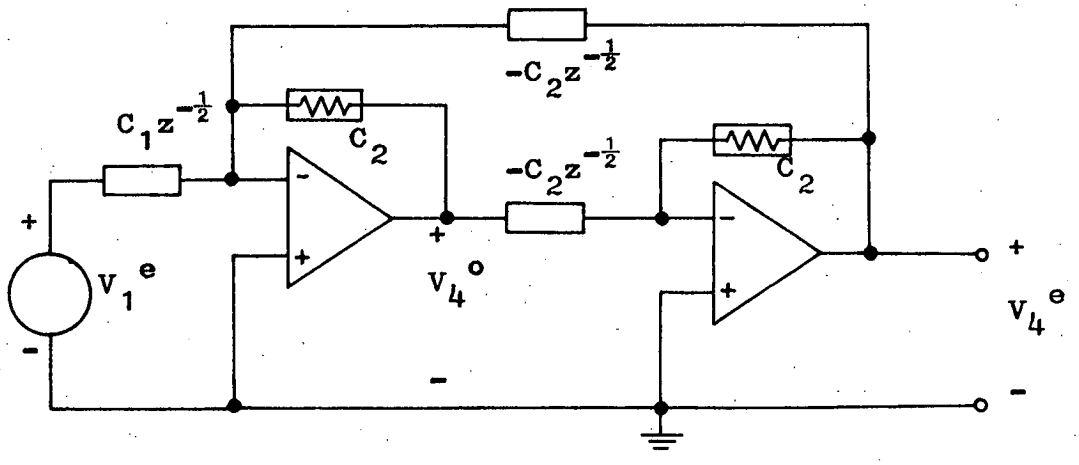
which are the same as in (2:23). Note that $H^{ee} = z^{-\frac{1}{2}}H^{eo}$, i.e. the output of the SCI is held over the full clock cycle.

3. Frequency responses

The above z-transform techniques accurately predict the input-output relationship of the SCI on a sample-by-sample basis. The frequency response on this basis is obtained by setting $z = \exp(j\omega T)$. However, in between these samples, the output of the SCI has the held, staircase-like wave shape. This analogue character of the circuit can be taken into account by multiplying the z-transform-computed frequency response with $(\sin\omega T/2)/(\omega T/2)$. For high sampling rates, where $\omega T \ll 1$, the passband of the frequency response is virtually unaffected.



(a)



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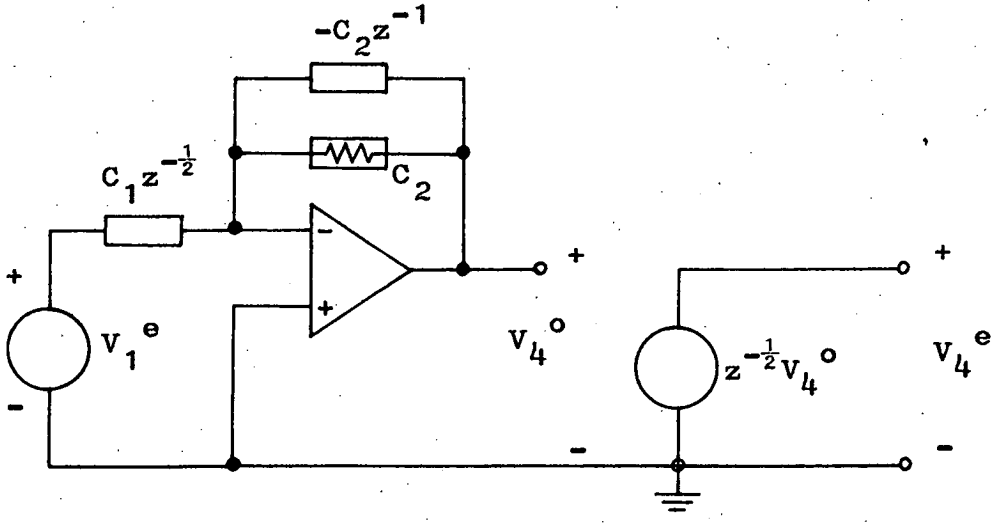

(c)

Fig. 2:10 Equivalent circuits of the switched-capacitor integrator in fig. 2:8.

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CHAPTER THREE

SWITCHED-CAPACITOR INTEGRATORS

An attractive technique for the design of switched-capacitor filters is based on active-RC filters which use integrators as building blocks. These include state-variable biquadratic circuits which are used in cascade design and leap-frog filters which simulate the operation of low-sensitivity, doubly-terminated LC ladder networks. The integrators in active-RC filters can simply be replaced by active switched-capacitor integrators (SCIs) such as given in fig. 2:8. The presence of the operational amplifier in each integrator makes it possible to eliminate effects of parasitics, thus ensuring accurate and reproducible filters. These features make the technique a popular approach for SCF design. Thus the SCIs form an important part of many realisable SCFs.

Hence, its development is discussed in detail in the following sections.

3.1 Transfer Functions

Fig. 3:1(a) shows the conventional analogue integrator with transfer function

$$H(s) = -\frac{1}{R_1 C_2 s} \qquad (3:1)$$

Originally, the SCI is developed from the analogue integrator by replacing the resistor with its switched-capacitor equivalent discussed in chapter 1.[1][2] Using the switched-capacitor "resistor" of fig. 1:1, results in the SCI in fig. 3:1(b) as in fig. 2:8, which has been referred to as the toggle-switched integrator. With $R_1 = 1/(f_c C_1)$, assuming frequencies much less than the clock rate, f_c, the frequency response of the SCI is given by, (setting $s = j\omega$)

$$H(\omega) = - f_c \left| \frac{C_1}{C_2} \right| \frac{1}{j\omega} \qquad (3:2)$$

Using the series switched capacitor in fig. 1:3, the integrator in fig. 3:1(c) is obtained.

Eqn. (3:2) shows that the integrator gain is dependent on a capacitor ratio and the clock frequency. The ability to obtain precise capacitor ratios and a very stable clock means that precision integrator gain can be produced.

However, the actual frequency response of the SCI deviates from that of the analogue integrator, especially for frequencies approaching the clock frequency. Due to its sampled-data nature, a more exact analysis using z-transform techniques as discussed in chapter 2 has to be used. The transfer function of the SCI when the output is sampled during the even interval is (see eqn. (2:24a))

$$H^{ee} = - \frac{C_1}{C_2} \cdot \frac{z^{-1}}{1 - z^{-1}} \qquad (3:3)$$

By setting $z = \exp(j\omega T)$ where $T = 1/f_c$, the frequency response is then given by

$$H(\omega) = - f_c \frac{C_1}{C_2} \cdot \frac{1}{j\omega} \left[\frac{\omega T}{2\sin(\frac{\omega T}{2})} \right] \exp\left(- \frac{j\omega T}{2}\right) \qquad (3:4)$$

Comparing (3:2) and (3:4), both magnitude and phase deviations are present in the frequency response of the SCI, especially when $\omega T << 1$ is not satisfied. The magnitude deviation is not significant. However, the excess phase shift is important in that it will cause distortion in the form of Q-enhancement in which the response of the complete filter shows some undesired peaking. [3]

If eqns (3:1) and 3:3) are compared, then it can be seen that

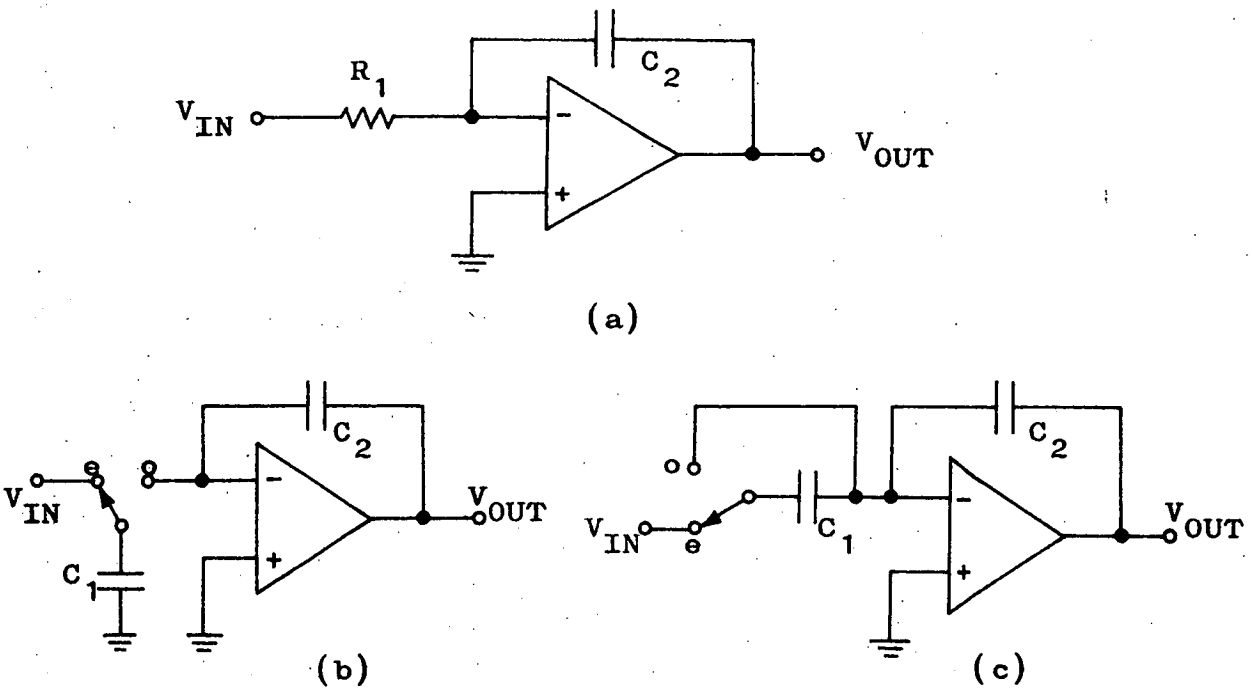

Fig. 3:1 (a) Analogue integrator. (b) Toggle-switched integrator. (c) Series-switched integrator.

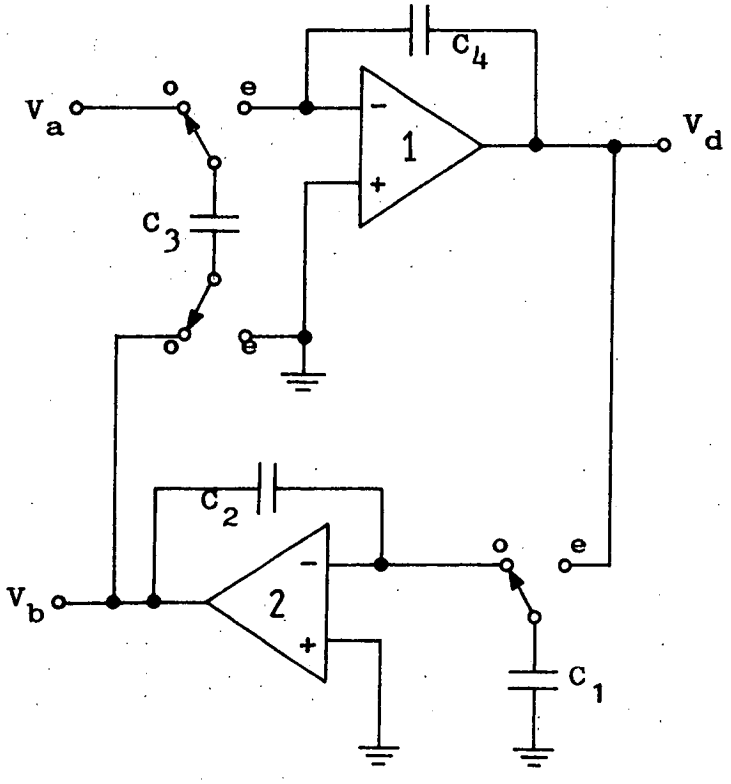

Fig. 3:2 A two-integrator loop with proper switch phasing.

implementing the integrator as in fig. 3:1(b) realise the mapping

$$s \rightarrow \frac{1}{T} \frac{1 - z^{-1}}{z^{-1}} \qquad (3:5)$$

which is the forward difference transformation. This transforms the imaginary axis in the s-plane to the vertical line going through z = 1 in the z-plane instead of onto the unit circle. Thus it maps high-Q s-plane poles and zeros into z-plane poles and zeros which are very close to the unit circle or even outside it.

For the integrator in fig. 3:1(c), its transfer functions can be obtained from its equivalent circuit in which blocks of fig. 2:6(b), (d) and fig. 2:7(a), (d) are interconnected. When its output is sampled during the even interval, the transfer function is,

$$H^{ee} = -\frac{C_1}{C_2} \frac{1}{1 - z^{-1}} \qquad (3:6)$$

Comparing (3:1) and (3:6), this implements the backward difference transformation.

$$s \rightarrow \frac{1}{T} (1 - z^{-1}) \qquad (3:7)$$

This maps the imaginary axis of the s-plane inside the unit circle of the z-plane.

The excess phase shift in (3:4) can be eliminated if the output is sampled during the odd interval.[4] Hence, as in eqn. (2:24b), the transfer function of the SCI is

$$H^{eo} = -\frac{C_1}{C_2} \frac{z^{-\frac{1}{2}}}{1 - z^{-1}} \qquad (3:8)$$

which gives the frequency response,

$$H(\omega) = -\frac{f_c C_1}{C_2} \cdot \frac{1}{j\omega} \left[\frac{\omega T}{2\sin(\omega T/2)} \right] \qquad (3:9)$$

Thus, if the switch phasing in the overall circuit of the filter ensures that the output of the integrator is sampled correctly, then the undesirable effects due to the excess phase shift can be avoided. This implementation is equivalent to realising the lossless discrete integrator (LDI) transformation

$$s \rightarrow \frac{1}{T} \quad \frac{1 - z^{-1}}{z^{-\frac{1}{2}}} \qquad (3:10)$$

The LDI transformation, maps the imaginary axis of the s-plane onto the unit circle of the z-plane and ensure stable s-domain transfer functions map into stable z-domain transfer functions. The magnitude deviation as in (3:9) is due to the fact that only the portion $-\frac{2}{T} < \Omega < \frac{2}{T}$ of the imaginary axis of the s-plane is mapped onto the unit circle. The deviation can thus be adjusted, if necessary, by prewarping the continuous-time filter frequency, Ω using

$$\Omega = \frac{2}{T} \sin\left(\frac{\omega T}{2}\right) \qquad (3:11)$$

i.e. by replacing ω in (3:2) by Ω, (3:2) becomes equivalent to (3:9).

As an example, the two-integrator loop shown in fig. 3:2 has proper switch phasing and thus is free from phase errors. This loop forms an important section in building switched-capacitor ladder filters as discussed in chapter 6. Note that integrator 1 in fig. 3:2 realises the switched-capacitor differential integrator, since capacitor C_3 is charged to the difference between two input voltages, V_a and V_b. Using the equivalent circuit method in chapter 2, the input-output relation is determined to be

$$V_d^e = -\frac{C_3}{C_4} \frac{z^{-\frac{1}{2}}}{1 - z^{-1}} (V_a^o - V_b^o) \qquad (3:12)$$

From (3:12), it can also be noted that integrator 1 in fig. 3:2 becomes a non-inverting integrator if V_a is grounded.

3.2 Effects of Parasitic Capacitances

Another deviation of the SCI from ideal behaviour could be contributed by parasitic capacitances as shown in fig. 3:3 with the SCI of fig. 3:1(b) drawn in its MOS implementation. The gate-to-diffusion overlap capacitance, such as C_{gd} feeds a portion of the clock signal, ϕ_o onto the output. The effect of this feedthrough is to produce a dc offset voltage at the output of the integrator. Self-aligned MOS technologies with small overlap capacitances can be used to greatly reduce this effect.[5] Also, if CMOS switches are used, the positive rising and negative falling edges causing feedthrough are nearly matched and almost exactly cancelled.[6]

Another technique to overcome clock feedthrough is by adding a network to the positive input of the OA to cancel the signal injected by clock feedthrough at the negative terminal. [7] The cancellation, however, is dependent upon matching of the switches involved and assumes infinite common mode rejection ratio (CMRR) of the OA besides requiring double the total amount of capacitances.

Parasitic capacitances C_{t2} and C_{b2} from the top and bottom plates, respectively, of the integrating capacitor C_2, have no effect on circuit operation. This is due to their being always connected to virtual ground and a voltage source respectively. The top plate of the capacitor, which has lower parasitics, needs to be connected to the negative input of the OA in order not to impose stringent requirement on the OA low frequency gain.

The parasitic capacitance, C_{t1}, from the top plate of capacitor C_1, includes parasitic capacitances from the source or drain of the switches connected to C_1. It is charged to V_{IN} and discharged onto the integrating

capacitor. Thus error is introduced into the integrator gain. To attain a required accuracy, large C_1 is needed which increases the required circuit area. Furthermore, the parasitic capacitance is non-linear, hence, unacceptable harmonic distortion may be generated.

The non-inverting integrator 1, with V_a grounded in fig. 3:2, however, is free from effects of parasitic capacitances. The top plate parasitic of C_3 is switched between ground and virtual ground while the bottom plate parasitic capacitance is switched between a voltage source and ground. The same arrangement is used to obtain parasitic-insensitive inverting SCI as shown in fig. 3:4.[8] This circuit realises the same transfer function (3:6) as the series-switched integrator of fig. 3:1(c) except that the latter is sensitive to parasitics.

Eqn. (3:6) shows that this inverting integrator is delay free, and thus, in order to realise the same function as provided by the loop in fig. 3:2, it is necessary to connect it with a non-inverting integrator having one cycle delay as shown in fig. 3:5.[9] On the average through the loop there will still be half-cycle delay per integrator as required to realise the LDI transformation. Integrator 1 in fig. 3:5 also implements a switched-capacitor differential integrator. It remains parasitic insensitive since the bottom plate parasitic capacitance of capacitor C_3 is now switched between voltage sources. The input-output relation of the integrator is

$$V_d e = - \frac{C_3}{C_4} \frac{1}{1-z^{-1}} (z^{-\frac{1}{2}} V_a o - z^{-1} V_b e) \qquad (3:13)$$

Although the parasitic-insensitive integrators above provide efficient and practical solutions to many SCF problems, there are certain advantages in keeping the toggle-switched topology as in fig. 3:1(b). As an example,

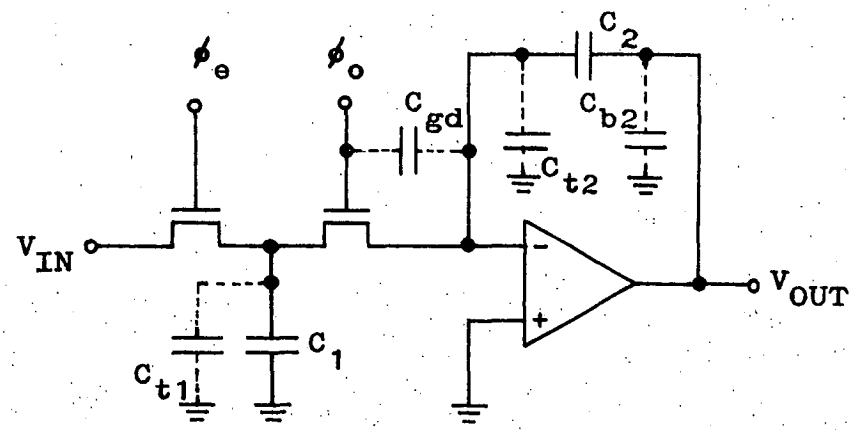

Fig. 3:3 MOS implementation of the toggle-switched integrator with parasitic capacitances.

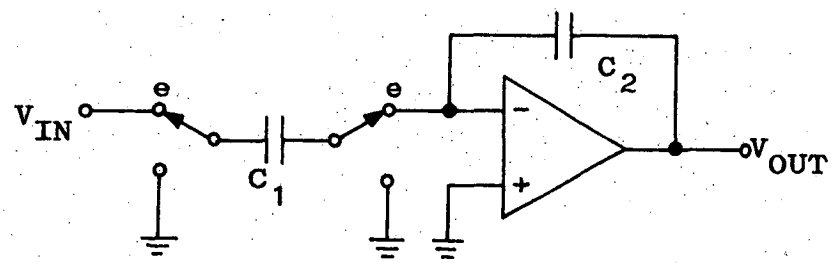

Fig. 3:4 Parasitic-insensitive inverting integrator.

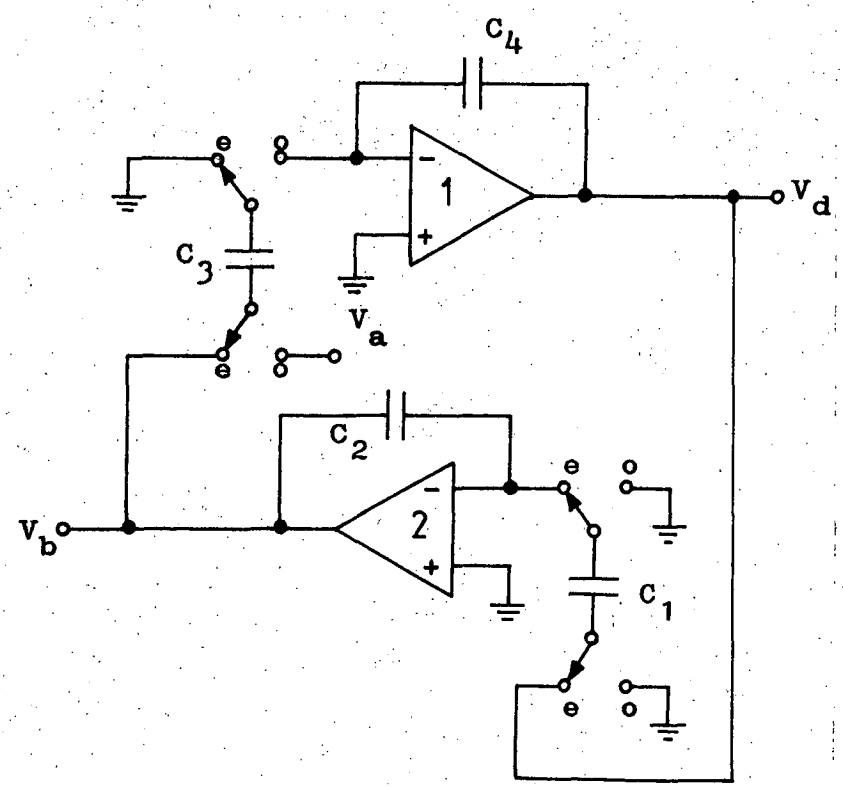

Fig. 3:5 Parasitic-insensitive two-integrator loop.

the toggle-switched integrator does not have a continuous path between input and output at any time. Thus other ways of overcoming the top-plate parasitics in the toggle-switched integrator have been suggested.

One such method is through the use of the parasitic compensated integrator shown in fig. 3:6(a) together with the relevant parasitic capacitances, C_{t1} and C_{t2}. The equivalent circuit of the integrator is shown in fig. 3:6(b). Assuming linear parasitic capacitances, the transfer function is given by

$$H^{eo} = -\frac{2C_1(2C_1 + C_{t2})z^{-\frac{1}{2}}}{C_2(4C_1 + C_{t1} + C_{t2})(1 - z^{-1})} \qquad (3:14)$$

The same transfer functions as in (2:24) are obtained if $C_{t1} = C_{t2}$. This is possible if the routings associated with nodes 1 and 2 are made equal and equal-sized switches are used.[10] The same is true when non-linear parasitic capacitances are considered as shown in [11].

The matching condition may be difficult to ensure in practice. Nevertheless this method is better than predistorting the capacitor C_1 in fig. 3:1(b) to compensate for the top plate parasitic capacitance. The compensated integrator of fig. 3:6(a), however, requires two capacitors for C_1, each having double the value of C_1 in fig. 3:1(b). The parasitic compensated non-inverting integrator is obtained by changing the phasing of the switches connected to nodes 1 and 2 of the integrator in fig. 3:6(a). It differs from the non-inverting integrator in fig. 3:2 in that it produces an extra half-cycle delay.

3.3 Frequency Limitations

Non-ideal switches and OA used in the SCI are further causes of deviation in its behaviour. Their effects, however, are mainly frequency

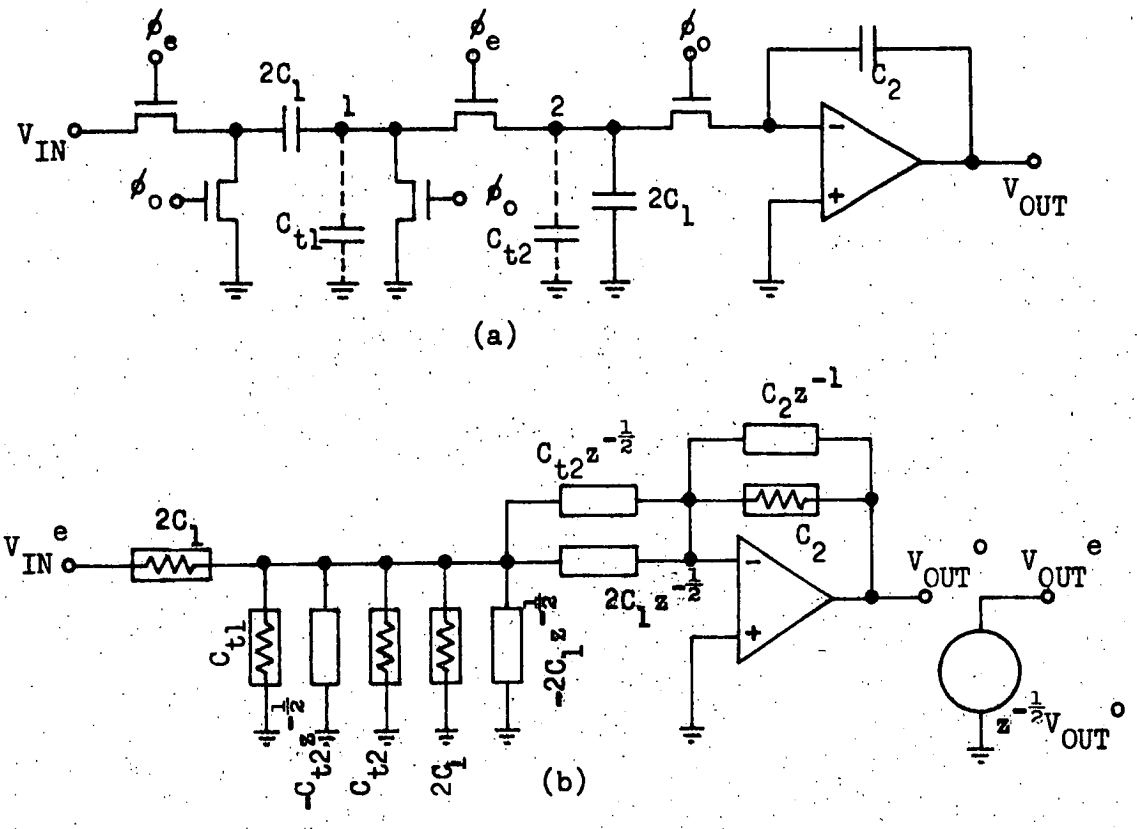

Fig. 3:6(a) Parasitic-compensated inverting integrator.
(b) Its equivalent circuit.

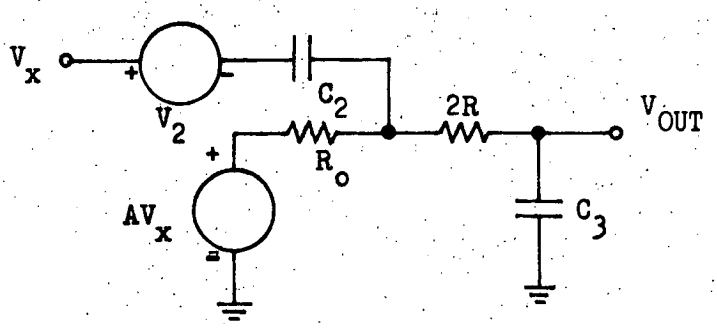

Fig. 3:7 Equivalent circuit for a charging half-period.

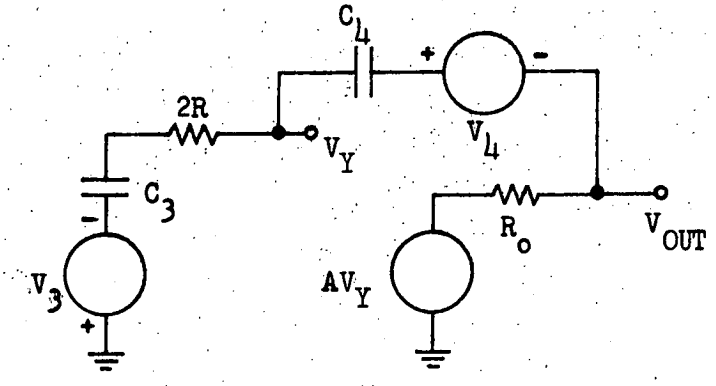

Fig. 3:8 Equivalent circuit for a discharging half-period.

dependent. A range of frequencies can thus be found where the effects of these non-idealities are negligible.

Low frequency use of the SCI is limited by leakage currents from the switch source and drain to the substrate during its off-state. These cause a dc voltage drift which shows up as a component of the output voltage offset. This offset can be reduced by limiting the usable clock frequency to a few hundred Hertz. Other major offset contributions due to clock feedthrough and offset of the OA have also to be reduced for low frequency applications. The dc input offset of the OA can be reduced by employing auto-zero techniques.[12]

The switch on-resistance, R, on the other hand, has an effect on the maximum allowable clock frequency. Its effects have to be analysed together with that of the OA non-idealities due to their interaction.[13] The OA is assumed to have a finite low frequency gain, A_o and a single pole, with output resistance, R_o. This represents a practical model for the OA with its gain function given by

$$A(s) = - \frac{A_o p_o}{s + p_o} \qquad (3:15)$$

where $A_o p_o = \omega_t = 2 \pi f_t$ is the unity-gain bandwidth of the OA.

The analysis involves considering the charging and discharging transients of the integrator stages. In fig. 3:5, during the even half period, amplifier 2 is charging capacitor C_3. If the integrating capacitor C_2 is assumed to have been fully charged to attain a voltage V_2 across it, then the equivalent circuit in fig. 3:7 can be used. The output is given by

$$V_{out} = - \frac{A_o p_o V_2}{(R_o + 2R)C_3 s^2 + [1 + (R_o + 2R)p_o C_3 + 2RA_o p_o C_3]s + p_o + A_o p_o} \qquad (3:16)$$

The final value of V_{out} is

$$V_{out}\Big|_{t\to\infty} = -\frac{A_o}{1+A_o}V_2 \qquad (3:17)$$

Large A_o is thus required to ensure complete charge transfer. If A_o is large, then P_o and the second term of the coefficient of s in (3:16) can be neglected.

The time V_{out} takes to reach an acceptable percentage of its final value can be estimated from the poles of (3:16). For complex poles, their real part can be taken as the controlling time constant. In case of real poles, the one with the lowest absolute value can usually be taken as the controlling term. These estimates give an indication the minimum length of time required for the even half period and thus the maximum clock frequency for the integrator.

During the odd half period in fig. 3:5, capacitor C_3 is now discharged through the following amplifier 1. If V_a is grounded, the equivalent circuit for the discharging transient is given in fig. 3:8, where V_3 is nearly equal to the final value in (3:17). The output, in this case, is given by, (neglecting p_o in (3:15)),

$$V_{out} = -\frac{(C_3/C_4)(R_oC_4s^2 - A_oP_o)V_3 + [R_oC_3s^2 + 2RC_3A_oP_os + A_oP_o]V_4}{(R_o+2R)C_3s^2 + (1 + C_3/C_4 + 2RA_oP_oC_3)s + A_oP_o} \qquad (3:18)$$

Thus an indication for the minimum length of time required for the odd half period can similarly be obtained.

It should be noted that in fig. 3:5, the charging and discharging of C_1 occurs in the same even half period as the charging of C_3. Hence, in actual fact, for this case, the time for the even half period need to be longer than that estimated using (3:16). The switch on-resistance can be

reduced to 1kΩ or less by increasing the width-to-length ratio of the switching transistors but leakage will increase. A choice can thus be made between the two extremes depending on whether high or low frequency application is desired.

In practice, the capacitance level is usually low enough for the effects of switch on-resistance to be neglected, if the frequencies of interest are not too high. As an example, using capacitor values C_3 = 10pF, C_4 = 30pF and pessimistic values for R = R_o = 5kΩ, A_o = 500 and p_o = 2Π(1kHz) in fig. 3:8, eqn (3:18) gives an estimate that the maximum allowable clock frequency is about 230kHz for V_{out} to reach 99.5 percent of its final value. If R is made zero, the maximum allowable clock frequency is estimated to be about 245kHz, showing little variation over the whole range of R. Thus keeping the clock frequency below 230kHz, the effects of the switch on-resistance can be neglected.

In this case, the effects of the OA finite bandwidth, ω_t may become dominant. The transfer function of the SCI, incorporating these effects, can be derived through time domain analysis assuming input signals which are step functions as shown in Appendix A. In the loop of fig. 3:5 with V_a grounded, OA 1 receives a step input at the beginning of the o clock phase and thus V_b is assumed to be sampled at this instant. V_d is sampled at the beginning of the e clock phase and it is assumed to be constant during this phase while being received by OA 2. Under these conditions transfer functions H_1^{oe} and H_2^{eo} of integrators 1 and 2, respectively, are given by (let $C_1 = C_3$, $C_2 = C_4$ for convenience),

$$H_1^{oe} = -H_2^{eo} = \frac{C_1}{C_2}\,\frac{z^{-\frac{1}{2}}}{1-z^{-1}}\,\frac{1-[1-Kz^{-1}(1-\exp(-k_2))]\exp(-k_1)}{1-Kz^{-1}\exp(-k_1-k_2)} \qquad (3:19)$$

where

$$k_1 = Kk_2,\ k_2 = \omega_t T/2,\ K = \frac{C_2}{C_1 + C_2} \qquad (3:20)$$

If an integrator has more than one input capacitor, then the sum of all the input capacitors replaces C_1 in (3:19). However, the signals into these capacitors must be step functions, as assumed in the analysis. If the sum of the input capacitors is smaller in value than the integrating capacitor, and $f_t/f_c > 5$, (3:19) shows that the effects of the OA bandwidth are negligible.[14]

The transfer function of the SCI, incorporating the effects of only the finite gain, A_o can be obtained using the equivalent circuit analysis as in fig. 2:10, with the OA replaced by voltage controlled voltage sources. For the inverting integrator in fig. 3:5, the transfer function is

$$H^{ee} = -\frac{C_1}{C_2}\,\frac{1}{1 - z^{-1}}\,\frac{1}{1 + \frac{1}{A_o}\left(1 + \frac{C_1}{C_2}\,\frac{1}{1 - z^{-1}}\right)} \qquad (3:21)$$

The same error expression as in the bracket in (3:21) is obtained for the non-inverting integrator in fig. 3:5. The error consists of the magnitude error, $M(\omega)$ and the phase error, $\Theta(\omega)$, where [14]

$$M(\omega) = -\frac{1}{A_o}\left(1 + \frac{C_1}{2C_2}\right)$$

$$\Theta(\omega) = \frac{C_1}{C_2}\,\frac{1}{2A_o \tan\,(\omega T/2)} \qquad (3:22)$$

The phase error requires the clock frequency to be low compared to the signal frequencies. Otherwise A_o has to be made large to keep the error below an acceptable level.

The OA slew rate and settling time are other factors which limit the highest possible clock frequency. The amplifier needs to respond to change

in signal which occurs each clock cycle. The amount of change is dependent on the ratio of the clock to passband frequencies. Knowing the maximum instantaneous change in the signal, and given the OA slew rate and settling time, the maximum clock frequency can be determined.

3.4 Noise Considerations

Noise is another limiting factor in the use of the SCI. The important sources of noise in SCI are the thermal noise in the MOS transistor switches, the wideband thermal noise and the 1/f noise of the OA.[15] The thermal noise in the switches is due to their on-resistances. The total input-referred rms noise within the bandwidth of the integrator is approximately kT/C where C is the integrating capacitance and kT is the thermal voltage.[16] This is assuming the clock frequency is much larger than the frequencies of interest. Thus C needs to be large to reduce this noise. Power supply noise coupled into the integrating node by parasitic capacitance also require that C be large for good power supply rejection ratio (PSRR).[17] However, circuit area consideration poses a limit to the size of C.

The wideband noise of the OA has bandwidth greater than the clock rate of the SCI. Hence a portion of the high frequency components of this noise is aliased into the passband when the integrators are cascaded.[18] A low level of noise output at frequencies beyond the f_t of the OA can be achieved by using one or two stages OA without an output stage. f_t of the OA in excess of the settling requirements, as dictated by clock frequencies, has also to be avoided in order to reduce the effect of this noise.

$1/f$ noise is concentrated at low frequencies and arises because of the surface behaviour in the channel of MOS transistors. Its magnitude is dependent on the process used, the design of the OA, and the size of input

transistors used in the OA. This noise is often the dominant source in low frequency applications. Approaches which involved modifying the channel of the transistors have been used in the past to reduce the $1/f$ noise. Two other approaches, using circuit techniques, have also been suggested.

One method is through using the correlated double sampling (CDS) technique. This involves replacing the SCI such as integrator 1 in fig. 3:5 by the integrator shown in fig. 3:9. The OA is replaced by a very high gain inverter, ensuring virtual ground at the amplifier input. Thus the same stray insensitive function as for integrator 1 in fig. 3:5 is obtainable with the advantage that it is also insensitive to offset of the amplifier and to slow variation with respect to the clock frequency. [19] The effect of $1/f$ noise component generated in the amplifier will now be reduced.

An inverter with a lower noise factor than the OA can also be used to reduce the wideband thermal noise component as well. Thus, in this case, the thermal noise of the switches becomes the dominant noise source. The signal output of the integrator, however, is now only available during the odd half period. Hence an extra clock phase is necessary for its use in the loop as in fig. 3:5.

Another method of $1/f$ noise reduction is by using chopper stabilisation technique. This involves modulating the noise using a chopping square wave causing the $1/f$ noise component to be shifted to the odd harmonic frequencies of the chopper. If the chopper frequency is much higher than the signal bandwidth, then $1/f$ noise in the signal band will be greatly reduced. The maximum reduction occurs when the chopper frequency equals $f_{c/2}$.

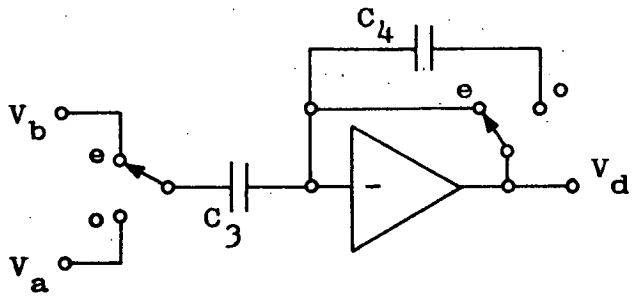

Fig. 3:9 Correlated double sampling differential integrator.

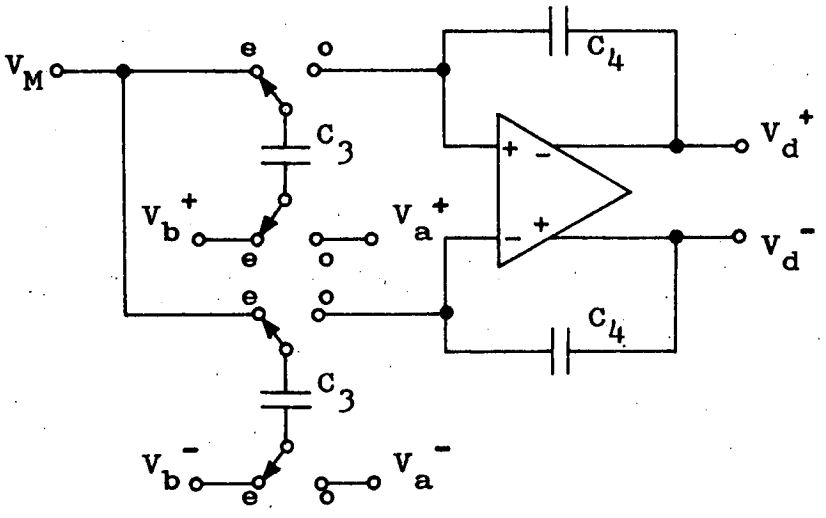

Fig. 3:10 Fully differential switched-capacitor integrator.

The chopper circuitry is amenable for incorporation in an OA with differential output configuration such as for the fully differential SCI shown in fig. 3:10.[20] V_M sets the common mode voltage at the OA input. This configuration doubles the effective signal swing, thus increasing the dynamic range further. It also reduces clock feedthrough and has good PSRR. However, the circuitry is more complex and a differential to single-ended conversion may be necessary in some applications.

These techniques enable the dynamic range of SCF to be extended beyond 100dB.[20] However, without these modifications, dynamic range of up to 90dB is still possible. This is usually sufficient in many applications.

3.5 Damped Switched-capacitor Integrators

It has been shown in sections 3.1 and 3.2 that integrator structures implementing the LDI transformation can provide accurate switched-capacitor realisation of the analogue integrator. However, a problem arises when damping resistance has to be realised in damped SCI. The damped analogue integrator in fig. 3:11 has transfer function,

$$H(s) = - \frac{\frac{1}{R_1C_2}}{s + \frac{1}{R_5C_2}} \qquad (3:23)$$

Applying the LDI transformation in (3:10), the transfer function becomes

$$H(z) = - \frac{\frac{T}{R_1C_2} z^{-\frac{1}{2}}}{1 + \frac{Tz^{-\frac{1}{2}}}{R_5C_2} - z^{-1}} \qquad (3:24)$$

The $z^{-\frac{1}{2}}$ term in the denominator associated with the damping resistor, R_5 is not realisable by switched-capacitor circuits. Theoretically, a new z-domain variable $\hat{z}^{-1} = z^{-\frac{1}{2}}$ can be introduced in (3:24) to eliminate the $z^{-\frac{1}{2}}$ term, but the circuit so obtained is unstable. Thus damping in biquadratic circuits and termination in ladder networks cannot be realised exactly through the LDI transformation.

The $z^{-\frac{1}{2}}$ term can, however be approximated by (a) 1, (b) z^{-1} or (c) $(1 + z^{-1})/2$.[21] Using approximation (a) is equivalent to realising the resistor through the backward difference transformation in (3:7). A damped SCI which implements this approximation is shown in fig. 3:12 and has the transfer function.

$$H^{eo} = - \frac{\frac{C_1}{C_2} z^{-\frac{1}{2}}}{1 + \frac{C_5}{C_2} - z^{-1}} \qquad (3:25)$$

The forward difference transformation in (3:5) is used to realise the resistor when adopting approximation (b). One circuit implementing this approximation is given in fig. 3:13(a) with transfer function,

$$H^{eo} = - \frac{\frac{C_1}{C_2} z^{-\frac{1}{2}}}{1 + \frac{C_5}{C_2} z^{-1} - z^{-1}} \qquad (3:26)$$

This circuit is sensitive to the top-plate parasitic capacitance of C_5. Fortunately when C_5 is less than C_2, which is true in most practical cases, the parasitic insensitive circuit in fig. 3:13(b) can be used to obtain the same transfer function (3:26). The above approximations can also be implemented for non-inverting damped SCI circuits.[9]

Errors associated with approximations (a) and (b) have both real and imaginary terms resulting in significant frequency response distortion.[22]

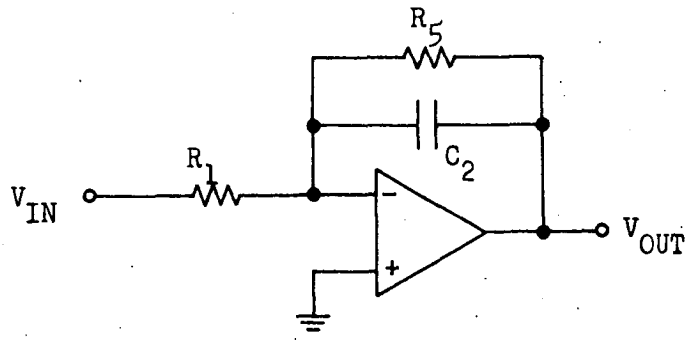

Fig. 3:11 Analogue integrator with damping.

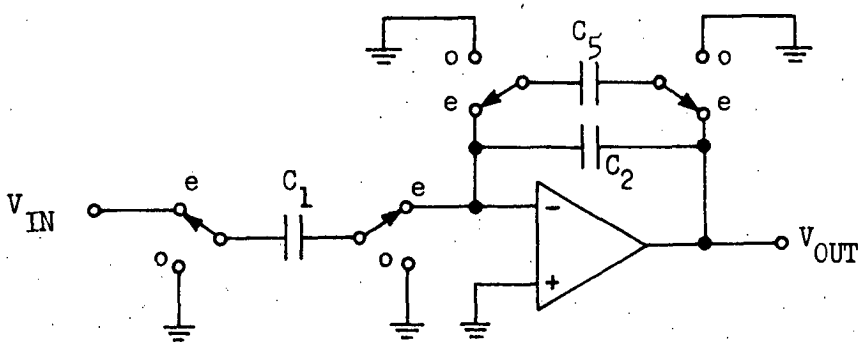

Fig. 3:12 LDI integrator with backward difference damping.

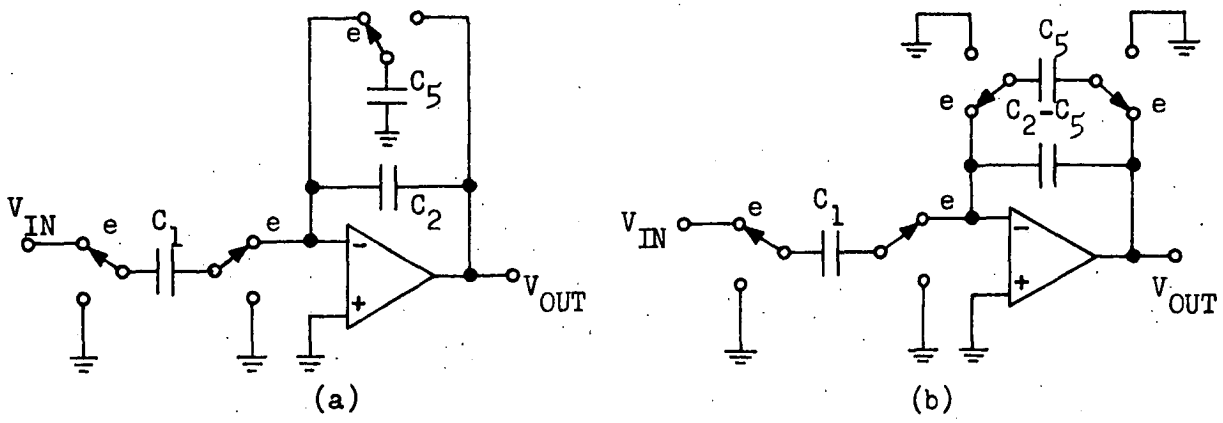

Fig. 3:13 (a) LDI integrator with forward difference damping.
(b) Parasitic insensitive equivalent of (a).

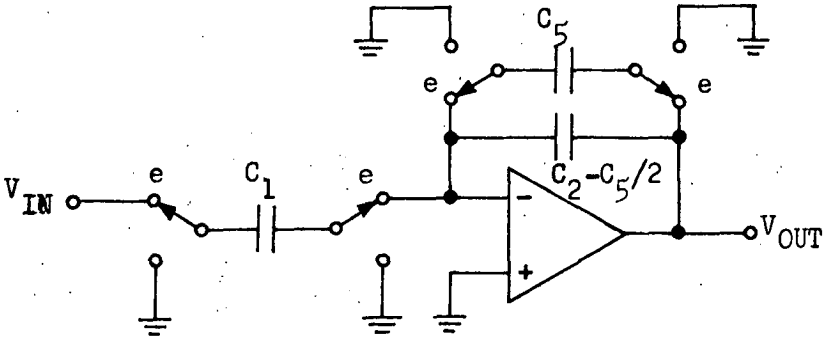

Fig. 3:14 LDI integrator with bilinear damping.

Error associated with approximation (c), on the other hand, is purely real. Thus approximation (c) only affects the element values with no dissipative effect and hence causes less distortion. However, for all three approximations, the distortion can be made small by having $\omega T << 1$.

A stray insensitive damped LDI integrator implementing approximation (c) can be derived from integrators in fig. 3:12 and fig. 3:13(b). It is shown in fig. 3:14 and has transfer function,

$$H^{eo} = -\frac{\frac{C_1}{C_2} z^{-\frac{1}{2}}}{1 + \frac{C_5}{2C_2} - (1 - \frac{C_5}{2C_2})z^{-1}} \qquad (3:27)$$

In this case, the resistor is implemented through the bilinear transformation

$$s \rightarrow \frac{2}{T} \frac{1 - z^{-1}}{1 + z^{-1}} \qquad (3:28)$$

The bilinear transformation, as the LDI, also maps the imaginary axis of the s-plane onto the unit circle in the z-plane and ensure a stable continuous-time filter is transformed into a stable discrete-time filter. In this case, however, the entire imaginary axis of the s-plane is mapped onto the unit circle and prewarping is done using

$$\Omega = \frac{2}{T} \tan (\frac{\omega T}{2}) \qquad (3:29)$$

This shows that the bilinear transformation compresses the frequency scale thus it enhances the high frequency attenuation for lowpass and bandpass filters. This is especially advantageous when the clock to signal frequency ratio is low. The LDI transformation, on the other hand, expands the frequency scale.[22]

The possibility of implementing the bilinearly transformed resistor implies that accurate switched-capacitor realisation of the analogue integrator

is also possible through the bilinear transformation. Also, damped bilinear SCI can be realised exactly without the restriction $\omega T \ll 1$. Thus the Nyquist frequency is the lowest frequency the clock can take though anti-aliasing requirement may set a higher limit.

The circuit in fig. 3:15(a) has the transfer function, [22]

$$H^{ee} = -\frac{C_1}{2C_2}\,\frac{1 + z^{-1}}{1 - z^{-1}} \qquad (3:30)$$

This is equivalent to putting (3:28) in (3:1) and replacing R_1 by $1/(f_c C_1)$, i.e. the bilinear integration is performed. The circuit in fig. 3:15(b) also realises the transfer function (3:30) if the input is full cycle sampled-and-held. [23] The circuit in fig. 3:15(a) does not have this limitation but requires two operational amplifiers. A number of other circuits have been suggested to implement bilinear integration but they are sensitive to stray capacitances. [22][24][25] Non-inverting bilinear integration is possible with the circuit in fig. 3:15(a) if the switch phasing of the switches at the OA input is interchanged as shown in brackets. For the circuit in fig. 3:15(b), a unity-gain inverting amplifier is required at its output to realise the non-inverting bilinear integrator.

Fig. 3:16(a) shows a damped bilinear SCI with transfer function,

$$H^{ee} = -\frac{\frac{C_1}{2C_2}\,(1 + z^{-1})}{1 + \frac{C_5}{2C_2} - (1 - \frac{C_5}{2C_2})\,z^{-1}} \qquad (3:31)$$

Putting (3:28) in (3:23), the transfer function becomes,

$$H(z) = -\frac{\frac{T}{2R_1C_2}\,(1 + z^{-1})}{1 + \frac{T}{2R_5C_2} - (1 - \frac{T}{2R_5C_2})\,z^{-1}} \qquad (3:32)$$

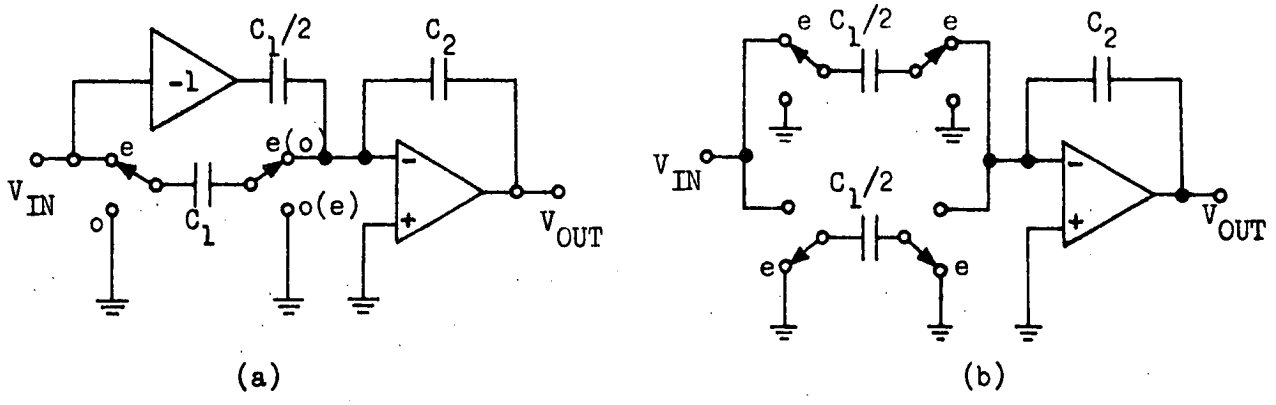

Fig. 3:15 Stray insensitive bilinear integrators.

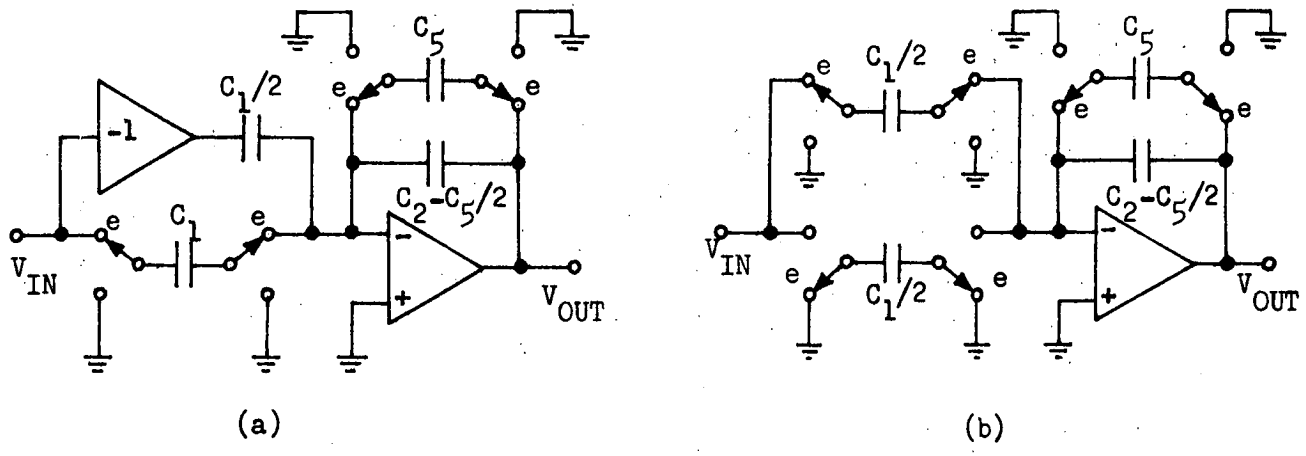

Fig. 3:16 Bilinear integrators with damping.

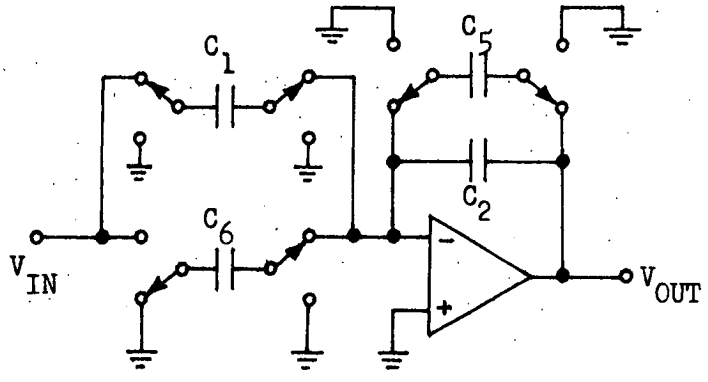

Fig. 3:17 A circuit realising first order filter with finite zero.

If H(s) in (3:23) is the prewarped desired function, then the capacitor ratios, for the switched-capacitor circuit in fig. 3:16(a) realising the desired function, can be obtained directly from the constants of H(s) and the clock frequency. Fig. 3:16(b) also realises a damped bilinear SCI with the same transfer function (3:31) if its input is full cycle sampled-and-held. [26]

The damped integrators can be used to realise first order lowpass transfer functions, as illustrated by (3:23) and (3:31). Finite zeros can also be realised by such circuits by including switched-capacitor, C_6 as shown in fig. 3:17. If the input is full cycle sampled-and-held, its transfer functions are

$$H^{ee} = -\frac{C_1 - C_6 z^{-1}}{C_5 + C_2 - C_2 z^{-1}} \qquad (3:33)$$

$$H^{eo} = z^{-\frac{1}{2}} H^{ee}$$

The output is thus also fully held over the clock period. [26] Similar transfer function as in (3:33) is also obtained if the backward, forward or bilinear transformation is applied to the s-domain transfer function,

$$H(s) = -\frac{a_1 s + a_o}{s + b_o} \qquad (3:34)$$

For example, using the bilinear transformation by applying (3:28) to (3:34) the following transfer function is obtained

$$H(z) = -\frac{(a_1 + a_o T/2) - (a_1 - a_o T/2) z^{-1}}{1 + b_o T/2 - (1 - b_o T/2) z^{-1}} \qquad (3:35)$$

The capacitor values in (3:33) can thus be designed, in this case, by equating the coefficients of z in (3:33) with those of (3:35). A first order highpass transfer function can be obtained by setting $a_o = 0$ in (3:35) and $C_1 = C_6$ in (3:33).

3.6 Summary

In this chapter, the derivations of SCIs through the various transformations are shown. The parasitic insensitive inverting and non-inverting integrators derivable through the backward and forward difference transformations respectively, can be combined in a loop to realise the LDI transformation. The LDI transformation is a suitable s-z transformation but LDI transformed resistor is not realisable by SC circuits. The bilinear transformation is a more suitable transformation but its use results in SCIs which require more OAs in order to be insensitive to parasitic capacitances.

Besides the effects of parasitic capacitances, other factors limiting the use of the SCIs are noise contributions from the MOS components and non-idealities in the switches and OAs. Modifications of the SCIs to reduce noise are possible if very large dynamic range is required. Non-ideal MOS switches and OAs restrict the useful frequency range of the SCFs. Its extension is possible with further improvement to MOS components especially the OAs.

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CHAPTER FOUR

DESIGN OF SWITCHED-CAPACITOR BANDPASS FILTERS

The design of switched-capacitor bandpass filters are used as examples for the application of the various techniques possible in switched-capacitor filter design. In particular, the bandpass (BP) filter required for acoustical measurement, i.e. the one-third octave bandpass (OTOB) filter is designed. This chapter gives the preliminary designs necessary before the application of the SC techniques such as the prewarping of the specifications. Also, procedures for obtaining the transfer function and the ladder network which meet the specification are given. The SC BP filters are then designed according to the various techniques in the following chapters as the techniques are described.

4.1 Specification of the Bandpass Filter

The specification of the OTOB filter can be obtained from the British Standard 2475:1964 and is given in fig. 4:1 and Table 4:1.[1] A set of these filters is required for acoustic noise measurement. The preferred midband frequencies, f_m are given by

$$f_m = 1000 \times 10^{n/10} \qquad (4:1)$$

where n is a positive or negative integer or zero.[1] The list of midband frequencies intended to be achieved by the SC BP filters are given in Table 4:2.

Table 4:1 Specification for one-third octave Bandpass Filter.

Frequency Range	Attenuation *A*dB
From $\frac{fm}{12\sqrt{2}} = 0.944f_m$ to $f_m \sqrt[12]{2} = 1.060f_m$	$-0.5 \leq A \leq 1$
From $\frac{fm}{6\sqrt{2}} = 0.891f_m$ to $f_m \sqrt[6]{2} = 1.122f_m$	$-0.5 \leq A \leq 6$
At $\frac{fm}{8\sqrt{2}} = 0.794f_m$ to $f_m \sqrt[8]{2} = 1.260f_m$	≥ 13
Below $\frac{fm}{4}$ and above 4 f_m	≥ 50
Below $\frac{fm}{8}$ and above 8 f_m	≥ 60

Table 4:2 Preferred Midband Frequencies for one-third octave Bandpass Filter.

Midband frequencies f_m (nominal values)			
Hz	HZ	kHz	kHz
10	100	1.0	10
12.5	125	1.25	12.5
16	160	1.6	16
20	200	2.0	20
25	250	2.5	
31.5	315	3.15	
40	400	4.0	
50	500	5.0	
63	630	6.3	
80	800	8.0	

4.2 Transfer Function Satisfying the Specification

From the specification in Table 4:1, the frequency values are normalised to f_m and rewritten in Table 4:3. These frequencies are geometrically symmetric, i.e.

$$f_m^2 = f_{+1} \cdot f_{-1} = f_{+2} \cdot f_{-2} = f_{+3} \cdot f_{-3} = f_{+4} \cdot f_{-4} = f_{+5} \cdot f_{-5} \qquad (4:2)$$

Thus the specification for the reference lowpass filter can be obtained by using the lowpass to bandpass transformation

$$s = a \left(\frac{s}{\Omega_R} + \frac{\Omega_R}{s}\right) \qquad (4:3)$$

In this case

$$a = \frac{fm}{f_{+1} - f_{-1}} = 8.651359 \qquad (4:4)$$

and $\Omega_R = 2\pi$. Thus using (4:3), the frequencies for the specification of the lowpass (LP) filter in fig. 4:2 are given by

$$g = a(f_+ - f_-) \qquad (4:5)$$

The calculated frequency values are given in Table 4:3.

Table 4:3 Specified Frequencies of the OTOB Filter and its corresponding reference Lowpass Butterworth filter gain response.

	Frequency values		$g = a(f_+ - f_-)$ $a = 8.651359$	magnitude (dB) $d = 0.337106$
f_m	1.000000			
f_{+1}	1.059463	g_1	1.000000	-0.467
f_{-1}	0.943874			
f_{+2}	1.122462	g_2	2.003337	-4.52
f_{-2}	0.890899			
f_{+3}	1.259921	g_3	4.033441	-14.9
f_{-3}	0.793701			
f_{+4}	4.000000	g_4	32.44259	-51.0
f_{-4}	0.250000			
f_{+5}	8.000000	g_5	68.12945	-63.9
f_{-5}	0.125000			

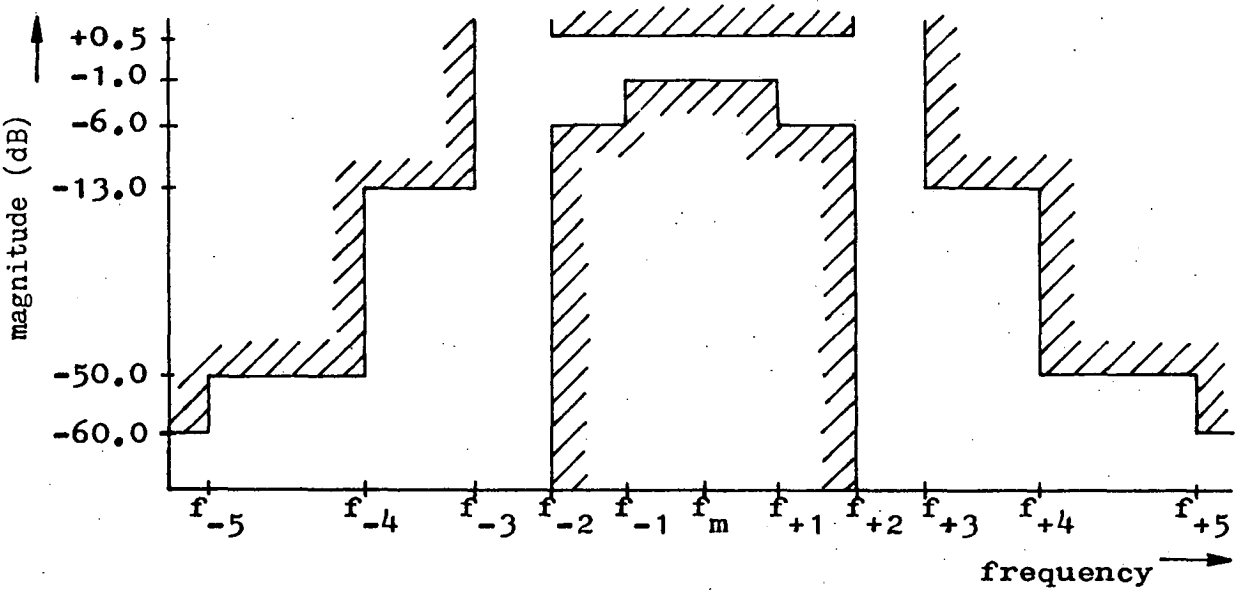


Fig. 4:1 Specification for the OTOB filter.

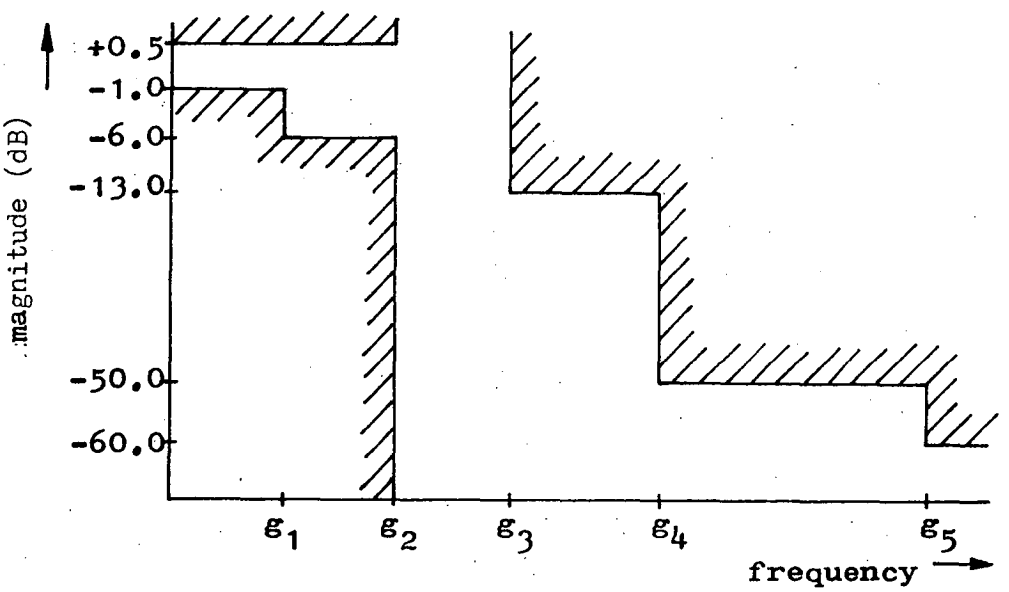


Fig. 4:2 Specification of the reference lowpass filter corresponding to that of the OTOB filter.

The specification in fig. 4:2 can be satisfied by a second-order Butterworth LP filter with magnitude function

$$H(g) = \frac{1}{\sqrt{1 + d^2 g^4}} \qquad (4:6)$$

Using d = 0.337106, the magnitudes as given in the last column of Table 4:3 are obtained at the specified frequencies. These values satisfy the given specification with allowances for droops which may be caused by the antialiasing and smoothing filters and the sample-and-hold function, and also for some tolerance in the element values. With the above d, the Butterworth LP filter transfer function is given by

$$H_{LP}(s) = \frac{1/d}{s^2 + \sqrt{2/d}\ s + 1/d} \qquad (4:7)$$

Applying the transformation in (4:3), the BP transfer function is

$$H_{BP}(s) = \frac{\frac{\Omega_R^2}{a^2 d}\, s^2}{s^4 + \frac{\Omega_R}{a}\sqrt{\frac{2}{d}}\, s^3 + \Omega_R^2\left(2 + \frac{1}{a^2 d}\right)s^2 + \frac{\Omega_R^3}{a}\sqrt{\frac{2}{d}}\, s + \Omega_R^4} \qquad (4:8)$$

For the design of filters using cascaded biquadratic sections, the BP transfer function can be factored as

$$H_T(s) = \frac{K_T s^2}{\left(s^2 + \frac{\omega_A}{Q}\, s + \omega_A^2\right)\left(s^2 + \frac{\omega_B}{Q}\, s + \omega_B^2\right)} \qquad (4:9)$$

where both biquads are set the same Q. Equating (4:8) and (4:9), we have

$$Q^2 = a^2 d + \tfrac{1}{4} + \sqrt{(a^2 d)^2 + 1/16} \qquad (4:10a)$$

$$\omega^2_{A,B} = \Omega^2_R \left[\left(\frac{Q^2}{a^2 d} - 1\right) \mp \sqrt{\left(\frac{Q^2}{a^2 d} - 1\right)^2 - 1} \right] \qquad (4:10b)$$

$$K_T = \frac{\Omega^2_R}{a^2 d} \qquad (4:10c)$$

Thus for values in Table 4:3, using BP functions for both factors, the two biquadratic transfer functions are

$$h_A(s) = \frac{K_A s}{s^2 + 0.822243s + 34.2865} \qquad (4:11a)$$

$$h_B(s) = \frac{K_B s}{s^2 + 0.946754s + 45.4566} \qquad (4:11b)$$

where $K_T = K_A . K_B = 1.56468$.

4.3 Transfer function satisfying the Bilinearly-prewarped Specification

If the SCF is to be designed using the bilinear transformation then it is necessary to prewarp the specification according to (3:29) especially when low f_c/f_m is used. The clock frequency, f_c is chosen to be 16 times the midband frequency of the BP filter. This is the lowest possible, so as to account for the magnitude specification at $8f_m$. The other consideration is that of the requirement for the antialiasing and smoothing filters as may be desired. With this low f_c at least a third-order LP function is required for the antialiasing filter. High f_c, however, results in large capacitor spread and large total capacitance required by the SCF which means more silicon area. Thus the emphasis, in this choice, is to achieve the lowest total capacitance possible for the SCF.

Using (3:29) which, in this case, is

$$\Omega = 32 \tan\left(\frac{\pi f}{16}\right) \qquad (4:12)$$

the prewarped frequencies are shown in Table 4:4. The prewarped frequencies are no longer symmetrical. The symmetry factor can be calculated as

$$A_s = \frac{\Omega_{+4} \cdot \Omega_{-4}}{\Omega_{+1} \cdot \Omega_{-1}} \qquad (4:13)$$

which is greater than unity. The prewarped specifications are made geometrically symmetric by using the reference frequency

$$\Omega_R = \sqrt{\Omega_{+1} \cdot \Omega_{-1}} \qquad (4:14)$$

and decreasing the upper stopband frequency, Ω_{+4}. [2] Thus

$$\tilde{g}_{+1} = \frac{\Omega_{+1}}{\Omega_R} \quad , \quad \tilde{g}_{-1} = \frac{1}{\tilde{g}_{+1}} \qquad (4:15a)$$

$$\tilde{g}_{-4} = \frac{\Omega_{-4}}{\Omega_R} \quad , \quad \tilde{g}_{+4} = \frac{1}{\tilde{g}_{-4}} \qquad (4:15b)$$

Similarly the other frequencies are calculated and are shown in Table 4:4. From this the specification of the corresponding reference LP filter is obtained using

$$g = a(\tilde{g}_+ - \tilde{g}_-) \qquad (4:16)$$

where

$$a = \frac{1}{\tilde{g}_{+1} - \tilde{g}_{-1}} = 8.429955 \qquad (4:17)$$

Using a second-order Butterworth LP function, the specification is satisfied, with allowances as before, at values given under g in Table 4:4 with d = 0.343383. Following similar steps as in section 4.2, the two biquadratic transfer functions are

$$H_A(s) = \frac{K_A s}{s^2 + 0.845999s + 35.1098} \qquad (4:18a)$$

$$H_B(s) = \frac{K_B s}{s^2 + 0.976431s + 46.7706} \qquad (4:18b)$$

where $K_T = K_A \cdot K_B = 1.66063$.

Table 4:4 Bilinearly prewarped frequencies of the OTOB filter and its corresponding reference Butterworth LP filter gain response.

Sub-script	f	$\frac{\Omega}{2\pi}$	$\tilde{g}$ Ω_R=6.365762	g a=8.429955	magnitude (dB) d=0.343383
m	1.000000				
+1	1.059463	1.075015	1.061070	1.000000	-0.484
-1	0.943874	0.954831	0.942445		
+2	1.122462		1.125591	1.999321	-4.60
-2	0.890899	0.900098	0.888422		
+3	1.259921		1.266129	4.015356	-15.0
-3	0.793701	0.800189	0.789809		
+4	4.000000	5.092958	4.049315	32.05372	-51.0
-4	0.250000	0.250201	0.246955		
+5	8.000000		8.103513	67.27196	-63.8
-5	0.125000	0.125025	0.123403		

4.4 Transfer function satisfying the LDI-prewarped specification

When the SCF is designed using the LDI transformation, prewarping is done according to (3:11) if low f_c/f_m is used. As mentioned in chapter 3 this transformation reduces the high frequency attenuation of the BP filter. If very low f_c is used, the high frequency attenuation may not meet the specified values. In fact $f_c = 16f_m$ cannot be used if a fourth-order Butterworth BP filter is required to meet the specification. Instead, $f_c = 24f_m$ is chosen. In this case (3:11) becomes

$$\Omega = 48\sin(\frac{\pi f}{24}) \qquad (4:19)$$

The prewarped frequency values are shown in Table 4:5. These are also not symmetrical but the symmetry factor is less than unity. They

are made geometrically symmetric by using Ω_R as in (4:14) with $\tilde{g}_{+1}$, $\tilde{g}_{-1}$ as in (4:15a) and increasing the lower stopband frequency as follows,

$$\tilde{g}_{+4} = \frac{\Omega_{+4}}{\Omega_R} \quad , \quad \tilde{g}_{-4} = \frac{1}{\tilde{g}_{+4}} \qquad (4:20)$$

The other frequencies are similarly calculated and are shown in Table 4:5. The specified frequencies of the reference LP filter are given under g with a = 8.701280. The specification is satisfied by a second-order Butterworth LP function with d = 0.342392.

Table 4:5 shows that less allowances for tolerance in the element values are available for the stopband attenuation. However, it is not detrimental in this case since the higher frequency attenuation will be enhanced by the antialiasing filter response while for the lower frequencies of the BP response, a margin has been created when the prewarped values are made geometrically symmetric.

Table 4:5 LDI-prewarped frequencies of the OTOB filter and its corresponding reference Butterworth LP filter gain response.

Sub-script	$\frac{\Omega}{2\pi}$	$\tilde{g}$ Ω_R=6.265137	g a = 8.701280	magnitude (dB) d=0.342392
m	0.997147			
+1	1.056070	1.059112	1.000000	-0.481
-1	0.941475	0.944187		
+2	1.118428	1.121650	2.002212	-4.60
-2		0.891544		
+3	1.254217	1.257830	4.027043	-15.0
-3		0.795020		
+4	3.819719	3.830722	31.06074	-50.4
-4	0.249955	0.261047		
+5	6.615947	6.635005	56.42162	-60.7
-5		0.150716		

4.5 Ladder network satisfying the specification

The normalised LP ladder network satisfying the second-order Butterworth function with a given d is shown in fig. 4:3.[2] The ladder network for the OTOB filter is then obtained by applying the transformation in (4:3). This is shown in fig. 4:4.

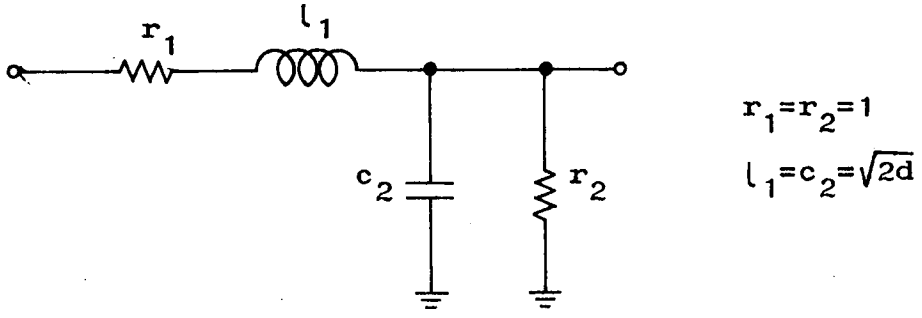


Fig. 4:3 Ladder realisation of second-order Butterworth lowpass filter.

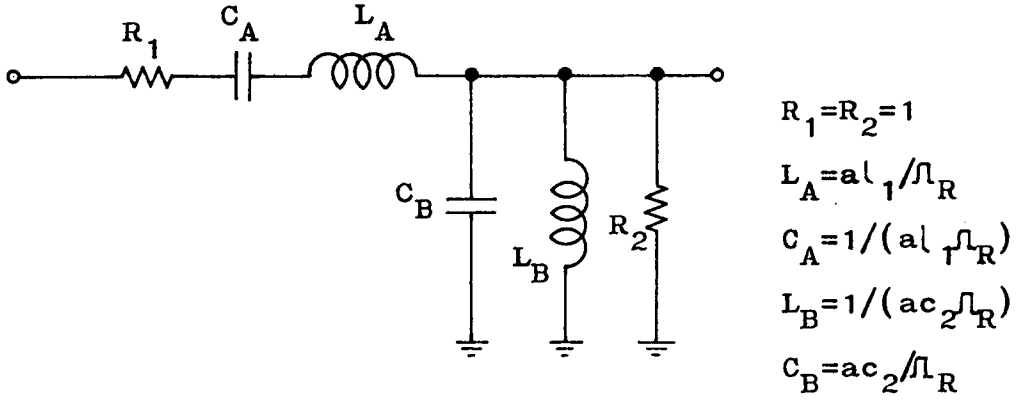


Fig. 4:4 Ladder realisation of fourth-order bandpass filter.

REFERENCES

[1] British Standard 2475:1964, "British Standard Specification for Octave and one-third Octave band-pass filters".

[2] R. Saal, *Handbook of Filter Design*, Berlin, W. Germany: AEG Telefunken, 1979.

CHAPTER FIVE

SWITCHED-CAPACITOR BIQUADS

One common method in the design of high order active-RC filters is through cascading biquadratic circuits. Similar procedure is possible for SCF realisations. As mentioned earlier, the biquadratic networks which are of special importance to SCF design are those which use integrators as building blocks. These integrators can be realised in SC forms through the LDI and bilinear transformations. Thus by directly replacing the integrators of the active-RC biquadratic circuit with SCIs as described in chapter 3, the resulting SC biquad can simply be designed.

However, in this case, the SC biquad obtained using LDI integrators requires that $\omega T \ll 1$. The SC biquad obtained using bilinear integrators does not have this limitation but requires more OAs so as to be insensitive to the effects of parasitic capacitances. Nevertheless it is desirable that the bilinear transformation be used in order to achieve a wider range of usable frequencies.

A better design possibility involves finding a SC biquad which has transfer function equals to the bilinear transformed transfer function of any biquadratic continuous-time filter.[1] This is illustrated for the first order transfer function by eqns (3:33) and (3:35) in chapter 3. A general SC biquad can be obtained based on the two-integrator loop topology as in fig. 3:5. The biquad requires only two OAs and is free from the effects of parasitic capacitances. The capacitor ratios are designed by equating coefficients of the SC biquad z-domain transfer function with those of the bilinear transformed s-domain transfer function.

When using the bilinear transformation, the s-domain transfer function must be prewarped by adjusting the cut-off and stopband edge frequencies according to eqn (3:29). The prewarping of the specification presents no difficulties but it does require a new filter table look-up or a new run through an approximation program. This can be avoided by using another method of designing SCF which works quite well for biquadratic sections. It involves setting up design equations based on matching the z-domain transfer function directly with the s-domain transfer function.[2] These two design methods for the SC biquad are described further in the following sections.

5.1 General Biquadratic Structure

A general switched-capacitor biquadratic structure based on the two-integrator loop topology is shown in fig. 5:1. It has z-domain transfer functions from both V_1 and V_2 of the form,

$$H(z) = \frac{\gamma + \varepsilon z^{-1} + \delta z^{-2}}{\Theta + \alpha z^{-1} + \beta z^{-2}} \qquad (5:1)$$

In the general structure, all possible parasitic insensitive switching arrangements for each required switched-capacitor of the integrators are included, such as, PC_2, QC_2, RC_2 and SC_2 for the SC between the two OAs.

Only one of the two integrators need to be damped. In this case, it does not matter on which OA the damping SC is placed since the output can be taken from either V_1 or V_2. In fig. 5:1, the damping is provided by either of TC_2, UC_2, WC_2 or YC_2 on OA 2. Alternatively, damping can be provided by connecting an unswitched capacitor between the OAs. An unswitched capacitor in the analysis is equivalent to the set of all possible switched-capacitors. If an unswitched capacitor $E'C_2$ is required between

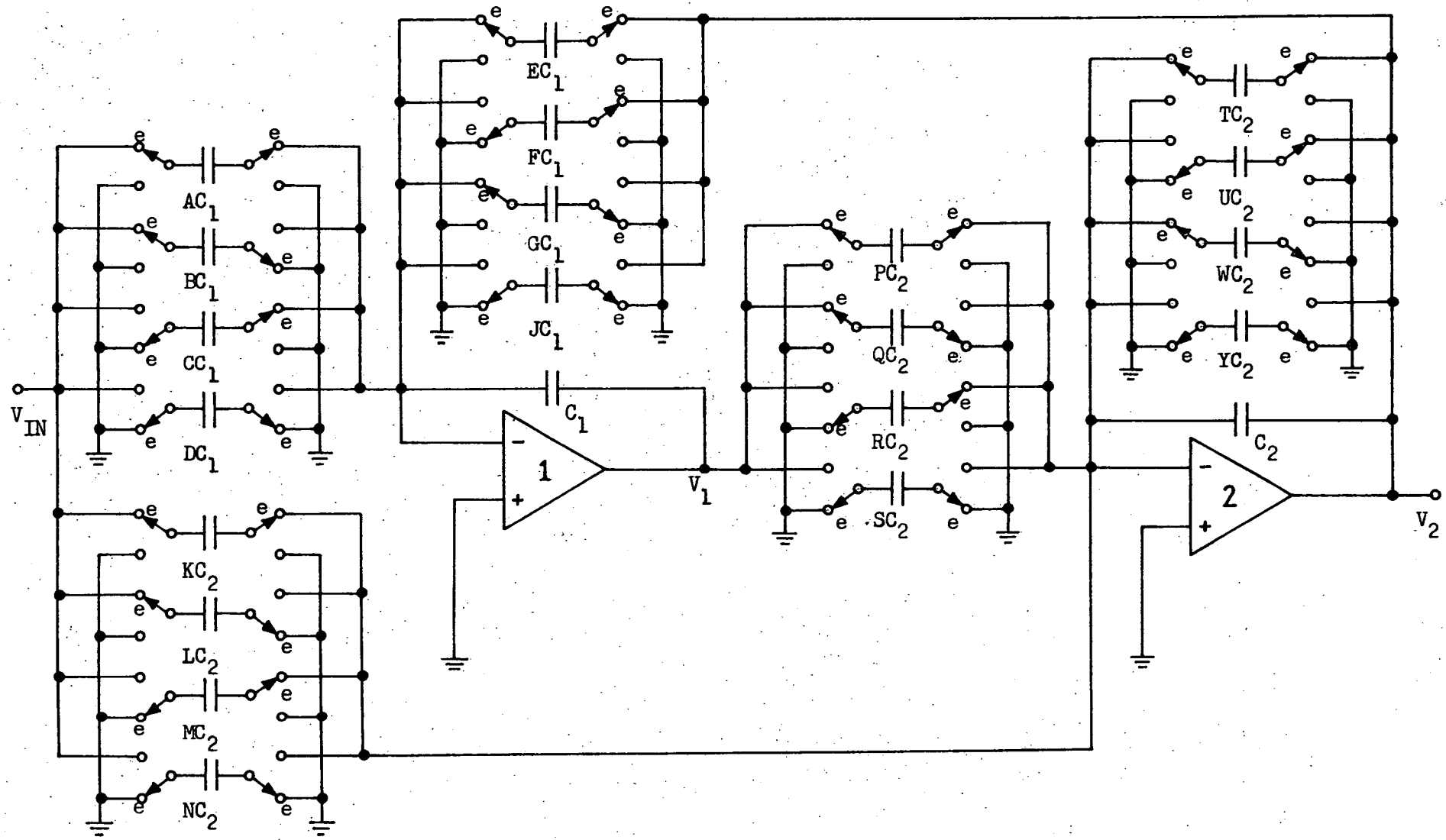


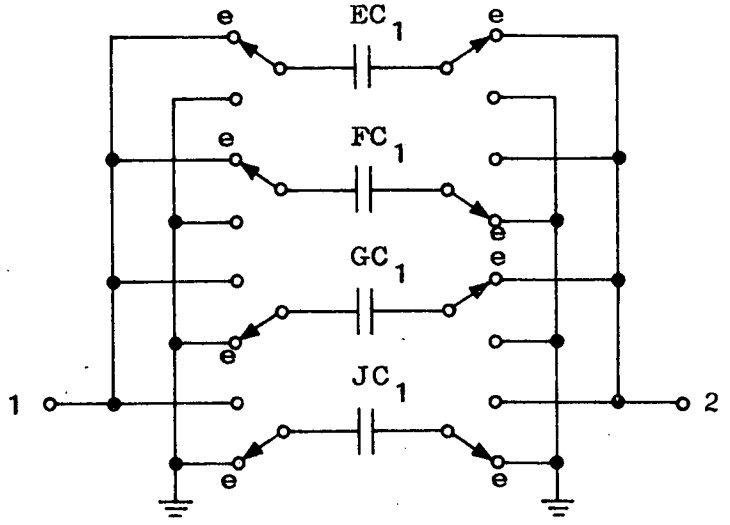
Fig. 5:1 A general switched-capacitor biquadratic structure.

V_2 and the negative input of OA 1, then this is equivalent to making E=F=G=J=E'.

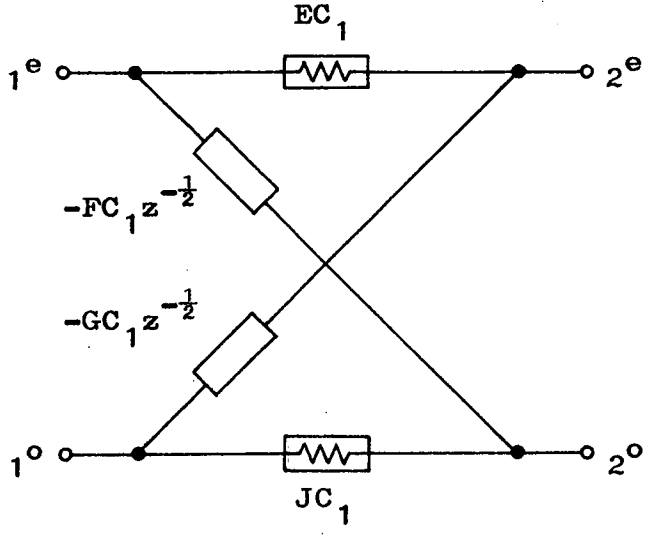
This equivalence is illustrated in fig. 5:2. The z-domain equivalent circuit of the set of all possible switched-capacitors shown in fig. 5:2(a) can be derived from the block in fig. 2:6(a). When both ends of the circuit are either voltage driven or at virtual ground then the equivalent circuit is given in fig. 5:2(b). When E=F=G=J, this is equivalent to the equivalent circuit of the floating capacitor in fig. 2:6(b) under the same terminal conditions.

The transmission zeros for the biquadratic transfer function are realised by the multiple feed-forward paths provided by the SCs from V_{IN} in fig. 5:1. Many of these SCs can be removed depending on the application desired of the biquad. Also, for reasons of stability, neither capacitors EC_1 and PC_2 nor capacitors JC_1 and SC_2 can both exist in a practical circuit.[3] Further reduction in the capacitor and switch count can be effected using SC element transformations which are specific cases of that shown in fig. 5:2.

Some examples of the SC element transformations are shown in fig. 5:3.[3] Unless specified, terminals 1 and 2 are either voltage driven or at virtual ground. In fig. 5:3(c), 1(a) and 1(b) must both be driven by different voltage sources or both at different virtual grounds. If EC_1 and GC_1 are unequal reduction is still possible by the transformations shown in fig. 5:3(d).[4] The switches marked (*) can be removed and the capacitors GC_1 and EC_1 are connected directly to terminal 2, if terminal 1 is connected to a full cycle S/H source and 2 is at virtual ground.



(a)



(b)

Fig. 5:2 (a) A set of parasitic-insensitive switched-capacitors with all possible switching arrangement. (1,2 are either voltage driven or at virtual ground). (b) z-domain equivalent circuit of (a) equivalent to that of an unswitched capacitor when E=F=G=J.

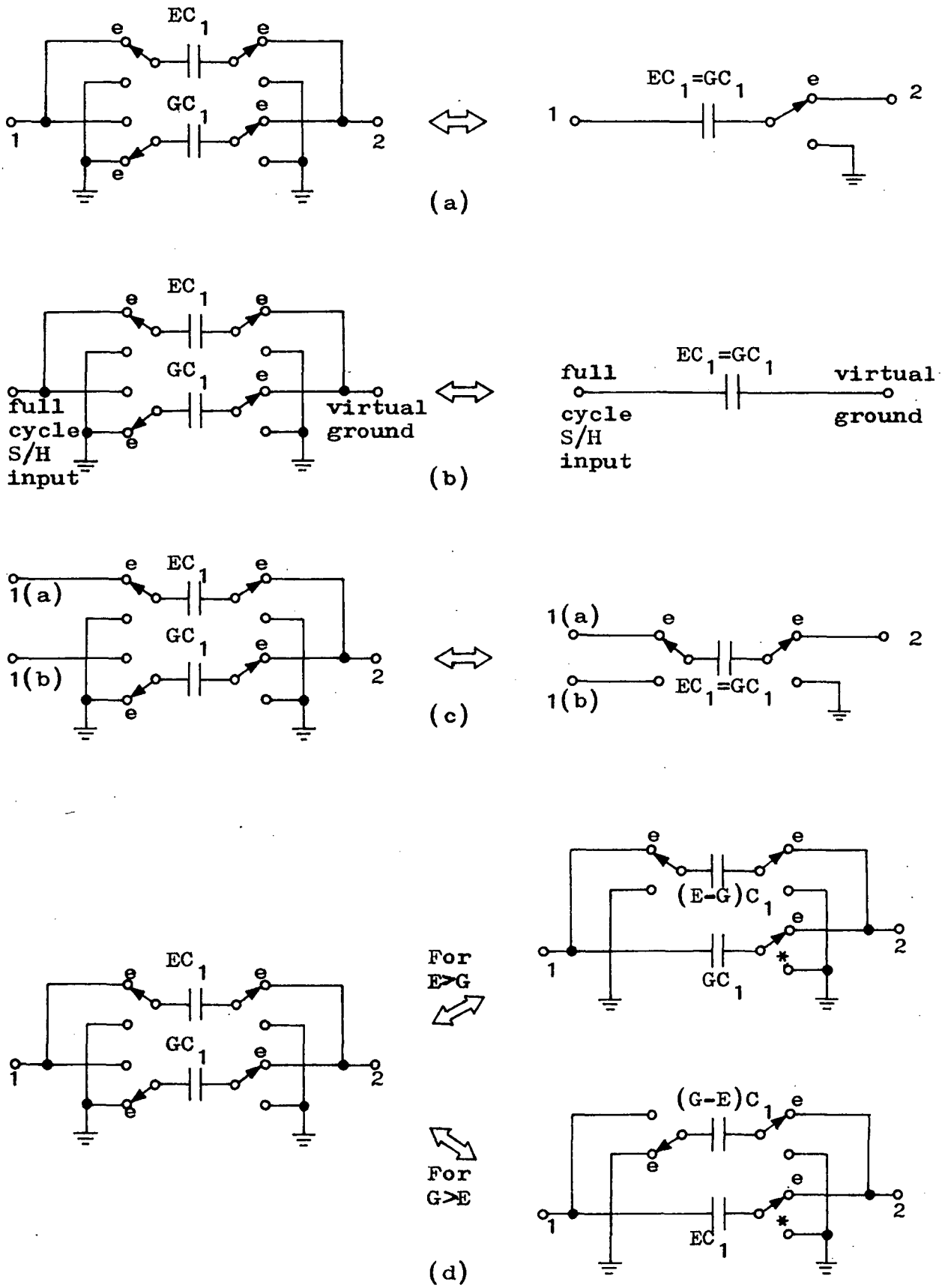


Fig. 5:3 Switched-capacitor element transformations. 1,2 are either voltage driven or at virtual ground. In (d) the switches marked (*) can be removed as in (b) if the same terminal conditions exist.

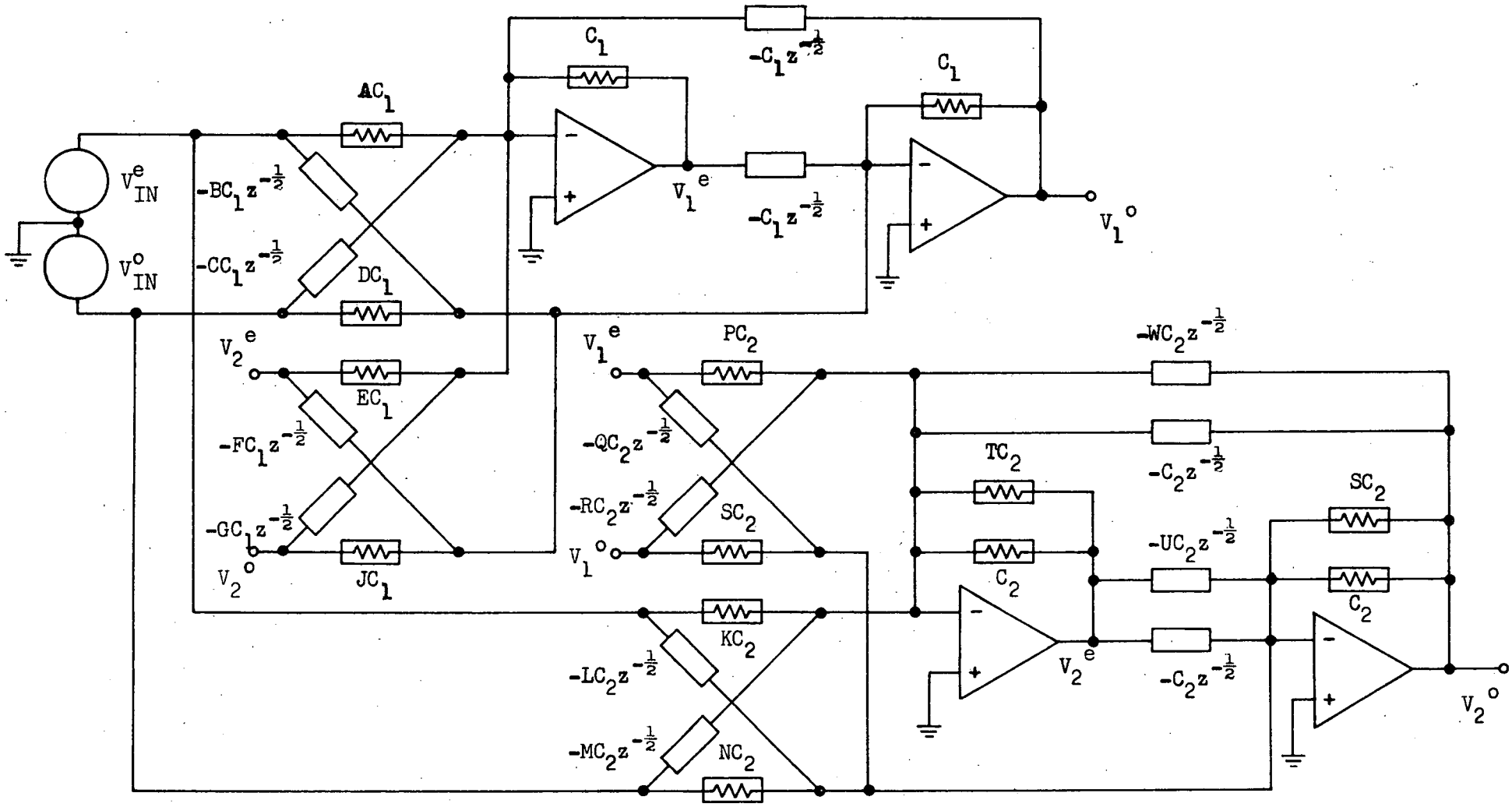


Fig. 5:4 z-domain equivalent circuit of the biquadratic structure in fig 4:1

5.2 Transfer Functions of the general biquad

The SC biquadratic circuit of fig. 5:1 can be replaced by its z-domain equivalent circuit using the equivalence in fig. 5:2 and the blocks in fig. 2:7. The equivalent circuit is given in fig. 5:4, from which the transfer functions from the input to V_1 and V_2 respectively are determined to be

$$H_1^{ee} = \frac{V_1^e}{V_{IN}^e} = (\gamma_1 + \varepsilon_1 z^{-1} + \delta_1 z^{-2})/\Delta \qquad (5:2a)$$

$$H_1^{oe} = \frac{V_1^e}{V_{IN}^o} = z^{-\frac{1}{2}}(\phi_1 + \sigma_1 z^{-1})/\Delta \qquad (5:2b)$$

and

$$H_2^{ee} = \frac{V_2^e}{V_{IN}^e} = (\gamma_2 + \varepsilon_2 z^{-1} + \delta_2 z^{-2})/\Delta \qquad (5:3a)$$

$$H_2^{oe} = \frac{V_2^e}{V_{IN}^o} = z^{-\frac{1}{2}}(\phi_2 + \sigma_2 z^{-1})/\Delta \qquad (5:3b)$$

where

$$\Delta = \Theta + \alpha z^{-1} + \beta z^{-2} \qquad (5:4a)$$

$$\Theta = (1 + T - EP)(1 + Y - JS) \qquad (5:4b)$$

$$\alpha = (1 + T - ER)[JQ - (1+Y)] + (1 + W - GP)[FS - (1 + U)] + (P - R)[F(1 + Y) - J(1 + U)] + (Q - S)[E(1 + W) - G(1 + T)] \qquad (5:4c)$$

$$\beta = (1 + W - GR)(1 + U - FQ) \qquad (5:4d)$$

and

$$\gamma_1 = (1 + Y - JS)[EK - A(1 + T)] \qquad (5:5a)$$

$$\varepsilon_1 = (1 + T - ER)[B(1 + Y) - JL] + (1 + U - FS)[A(1 + W) - GK] + (AR - K)[F(1 + Y) - J(1 + U)] + (BS - L)[E(1 + W) - G(1 + T)] \qquad (5:5b)$$

$$\delta_1 = (1 + W - GR)[FL - B(1 + U)] \qquad (5:5c)$$

$$\phi_1 = (1 + T - ER)[JN - D(1 + Y)] + (1 + Y - JS)[C(1 + T) - EM] + (N - DS)[E(1 + W) - G(1 + T)] \qquad (5:5d)$$

$$\sigma_1 = (1 + W - GR)[D(1 + U) - FN] + (1 + U - FS)[GM - C(1 + W)] + (M - CR)[F(1 + Y) - J(1 + U)] \qquad (5:5e)$$

and

$$\gamma_2 = (AP - K)(1 + Y - JS) \qquad (5:6a)$$

$$\varepsilon_2 = (K - AR)(1 + Y - JQ) + (L - BS)(1 + W - GP) + (R - P)[B(1 + Y) - JL] + (S - Q)[A(1 + W) - GK] \qquad (5:6b)$$

$$\delta_2 = (BQ - L)(1 + W - GR) \qquad (5:6c)$$

$$\phi_2 = (DS - N)(1 + W - GP) + (M - CP)(1 + Y - JS) + (R - P)[JN - D(1 + Y)] \qquad (5:6d)$$

$$\sigma_2 = (N - DQ)(1 + W - GR) + (CR - M)(1 + Y - JQ) + (S - Q)[GM - C(1 + W)] \qquad (5:6e)$$

The other transfer functions H_1^{oo}, H_1^{eo}, H_2^{oo}, H_2^{eo} are derivable from H_1^{ee}, H_1^{oe}, H_2^{ee}, H_2^{oe} respectively by recognising and interchanging the SC elements which are relevant to the transfer functions. A, B, E, F, K, L, P, Q, T, U are replaced by D, C, J, G, N, M, S, R, Y, W respectively and vice versa. Also, H_1^{oe}, H_2^{oe} can actually be derived from H_1^{ee}, H_2^{ee} respectively by replacing A, B, K, L in H_1^{ee}, H_2^{ee} with $-CZ^{-\frac{1}{2}}$, $-DZ^{+\frac{1}{2}}$ $-MZ^{-\frac{1}{2}}$, $-NZ^{+\frac{1}{2}}$ respectively.

In the above analysis for the transfer functions, the input signal is assumed to be sampled and held twice per clock period. Eqns (5:2) and (5:3) show that the biquadratic transfer functions are achieved when the input and output are sampled synchronously, i.e. both during the even clock phase or both during the odd clock phase. Thus for a particular biquadratic

transfer function, the structure in fig. 5:1 needs to sample the input voltage only once per clock period.

As an example, for the transfer function H_2^{ee}, the switched capacitors which are connected to the input during the odd clock phase can be removed. The modified structure can then take input which is held for any time interval less than or equal to the clock period. The clock phases, however, have to be adjusted so that the even clock phase is not longer than the time the input is held. In the limit, the S/H function is not necessary and an analogue signal can be applied directly to the input of the modified biquadratic structure.

Note, however, that in general $H_2^{eo} \neq Z^{-\frac{1}{2}}H_2^{ee}$ thus the output during the odd clock phase is different from that during the even clock phase. If a fully held output signal is desired, the biquad has to be followed by a suitable S/H circuit. A fully held output signal can be obtained directly from the biquad if charge transfers onto the integrating capacitor of the OA, from which the output is to be taken, are allowed only during one of the clock phases.

If the input signal to the biquadratic structure in fig. 5:1 is sampled, say at the start of the even clock phase and held over the full clock period, i.e. $V_{IN}^{o} = Z^{-\frac{1}{2}}V_{IN}^{e}$, then from (5:2) and (5:3),

$$V_1^e = (H_1^{ee} + Z^{-\frac{1}{2}}H_1^{oe})V_{IN}^e \qquad (5:7a)$$

$$V_2^e = (H_2^{ee} + Z^{-\frac{1}{2}}H_2^{oe})V_{IN}^e \qquad (5:7b)$$

Thus biquadratic transfer functions are still achieved during the even clock phase.

5.3 Derivation from the general biquad

All the second-order switched-capacitor circuits in the literature based on the two-integrator two-clock phase structure can be generated from the general biquadratic structure in fig. 5:1. The transfer functions of these circuits can also be easily derived from eqns (5:2) or (5:3). Many different biquad realisations are possible from the general structure for any desired transfer function. For examples, there are choices between using V_1 or V_2, and between damping with a switched-capacitor or using the unswitched capacitor.

There is no single biquad realisation which can be suitable for all applications. Also, so far, there is no general method to determine the biquad realisation which is most suitable for any particular application.[4] Thus it is necessary to compare all possible realisations in any particular design if the most efficient realisation is required. Some of the considerations for making this choice are as given in section 1.4.

Fig. 5:5 shows an example of a second order circuit generated from the general structure which is capable of realising bandpass transfer functions. The SC element transformations in fig. 5:2 and fig. 5:3 are used to reduce the number of capacitors and switches. Further switch reduction is obtained by making similarly switched capacitors share a common switch as shown at the negative inputs of the OAs. The damping for the circuit is provided by the unswitched capacitor $E'C_1$.

Using eqns (5:2) and (5:3), setting to zero all unused capacitors, the following transfer functions are obtained,

$$H_1^{ee} = [(EK + E'K - A) + (A - GK)Z^{-1}]/\Delta \qquad (5:8a)$$

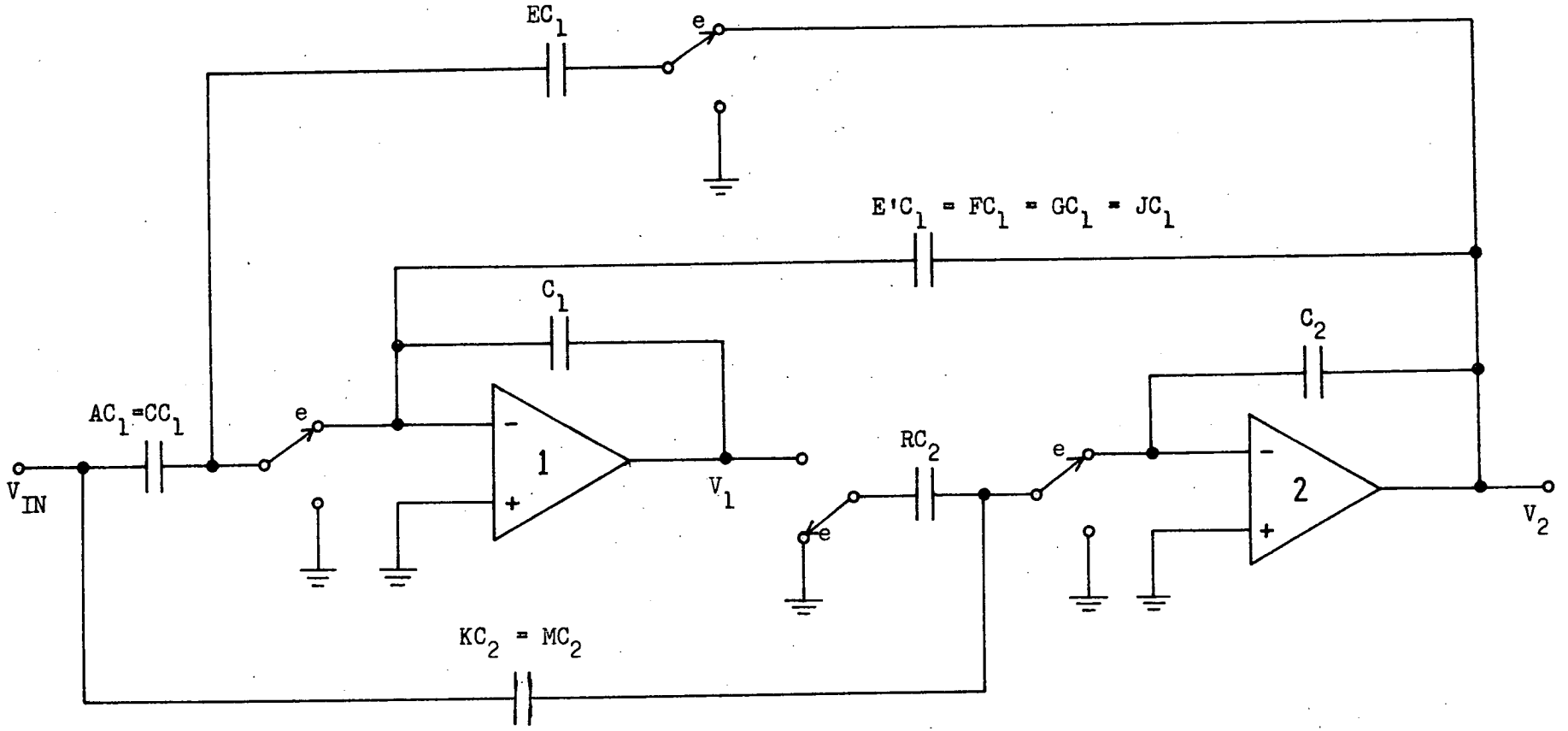


Fig. 5:5 A circuit for realising second-order bandpass transfer functions.

$$H_1^{oe} = Z^{-\frac{1}{2}}[(C - EM - E'M) + (GM - C)Z^{-1}]/\Delta \quad (5:8b)$$

$$H_1^{oo} = Z^{-\frac{1}{2}} H_1^{oe} \quad (5:8c)$$

$$H_1^{eo} = Z^{-\frac{1}{2}} H_1^{ee} \quad (5:8d)$$

and

$$H_2^{ee} = [-K + (K - AR)Z^{-1}]/\Delta \quad (5:9a)$$

$$H_2^{oe} = Z^{-\frac{1}{2}}[M + (CR - M)Z^{-1}]/\Delta \quad (5:9b)$$

$$H_2^{oo} = Z^{-\frac{1}{2}} H_2^{oe} \quad (5:9c)$$

$$H_2^{eo} = Z^{-\frac{1}{2}} H_2^{ee} \quad (5:9d)$$

where

$$\Delta = 1 + (ER + E'R - 2)Z^{-1} + (1 - GR)Z^{-2} \quad (5:10)$$

If the input signal to the circuit in fig. 5:5 is full cycle sampled-and-held, then using eqns (5:7) to (5:10), noting the equality of some of the capacitors, the transfer functions of the circuit becomes

$$H_1(z) = \frac{V_1^e}{V_{IN}^e} = \frac{(EK + E'K - A) + (2A - EK - 2E'K)Z^{-1} + (E'K - A)Z^{-2}}{1 + (ER + E'R - 2)Z^{-1} + (1 - E'R)Z^{-2}} \quad (5:11)$$

$$V_1^o = Z^{-\frac{1}{2}} V_1^e$$

$$H_2(z) = \frac{V_2^e}{V_{IN}^e} = - \frac{K + (AR - 2K)Z^{-1} + (K - AR)Z^{-2}}{1 + (ER + E'R - 2)Z^{-1} + (1 - E'R)Z^{-2}} \quad (5:12)$$

$$V_2^o = Z^{-\frac{1}{2}} V_2^e$$

The outputs from both V_1 and V_2 are also held over the full clock period. This circuit and the transfer functions can also be derived from the general biquad given in [4]. The denominator such as in (5:11) and (5:12) ensure

that all stable poles can be realised by the circuit. The numerators, on the other hand, allow the different usable forms of the bandpass function to be realised as shown in table 5:1.

The generic forms are referred to as BPij, where i, j denote the number of $(1 + Z^{-1})$, Z^{-1} factors respectively. The BP10 function arises when the bilinear transformation is applied to an s-domain BP transfer function. The BP01 and BP00 are achieved from the s-domain BP transfer function through the forward difference and backward difference transformations respectively. Table 5:1 also shows that $H_1(z)$ realises positive BP functions whereas $H_2(z)$ realises negative functions.

The circuit in fig. 5:5 can be modified for an input signal which is not held for the full clock period by switching the input capacitors to the signal during the even clock phase. This means only switched capacitors AC_1 and KC_2 are used at the input. From (5:8) and (5:9), H_1^{oe}, H_1^{oo}, H_2^{oe} and H_2^{oo} become zero. The outputs are still fully held but only the

Table 5:1 Design Equations for realising the different generic forms of the bandpass functions using the circuit of fig. 5:5.

Generic form	Numerator	Design Equations $H_1(z)$	Design Equations $H_2(z)$
BP10	$K^z(1 - z^{-1})(1 + z^{-1})$	$A = \frac{EK}{2} + E'K$ $K^z = \frac{EK}{2}$	$2K = AR$ $K^z = -K$
BP01	$K^z z^{-1}(1 - z^{-1})$	$A = EK + E'K$ $K^z = EK$	$K = 0$ $K^z = -AR$
BP00	$K^z(1 - z^{-1})$	$A = E'K$ $K^z = EK$	$K = AR$ $K^z = -K$

BP00 function can be realised. If the BP10 function is required with this input signal, then $AC_1 = BC_1$ and $KC_2 = LC_2$ have to be used as the input switched-capacitors, and switched-capacitor RC_2 in fig. 5:5 has to be replaced by the switched capacitor QC_2. The same transfer functions as (5:11) and (5:12) are obtained with R replaced by Q. The output, however, is no longer fully held. [4]

In the following design examples, the input signal is assumed to be held over the full clock period. The circuit in fig. 5:5 is used for the design of BP filters which fit the specification given in chapter 4. Circuits for realising other second-order transfer functions, such as the lowpass, highpass (HP), notch and allpass (AP) can also be generated from the general biquadratic structure in fig. 5:1 but are not discussed in detail here.

5.4 Design using the Bilinear Transformation

Higher order SCFs can be designed using the circuits realising bilinear transformed biquadratic transfer function which can be derived from the general structure in fig. 5:1. The following steps can be used.

1. The frequencies, at which the filter magnitudes are specified, are prewarped according to eqn (3:29).
2. Filter tables or computer programs are then used to find a transfer function $H_T(s)$ whose magnitude function $H_T(j\Omega)$ meets the specification. The procedures shown in chapter 4 are used in our case.
3. If $H_T(s)$ is even, then it is factored into the product of biquadratic transfer functions of the general form,

$$H(s) = \frac{a_2 s^2 + a_1 s + a_o}{s^2 + b_1 s + b_o} \qquad (5:13)$$

These second order transfer functions are chosen taking into consideration conditions for optimum pole-zero pairing, cascading sequence and gain distribution.[5]

4. The bilinear transformation as in (3:28) is then applied to (5:13). The bilinear transformed biquadratic transfer function is then

$$H(z) = \frac{(a_2 + a_1T/2 + a_oT^2/4) + 2(a_oT^2/4 - a_2)Z^{-1} + (a_2 - a_1T/2 + a_oT^2/4)Z^{-2}}{(1 + b_1T/2 + b_oT^2/4) + 2(b_oT^2/4 - 1)Z^{-1} + (1 - b_1T/2 + b_oT^2/4)Z^{-2}} \qquad (5:14)$$

5. Biquadratic circuits with transfer function equivalent to H(z) in (5:14) can be derived from fig. 5:1 and the capacitor ratios are designed by equating their coefficients.
6. The resulting biquadratic circuits are then cascaded to realise the overall filter transfer function.[1]
7. If $H_T(s)$ is odd, the remaining first order factor can be realised as described by eqns (3:33) to (3:35) and the circuit such as in fig. 3:17 is appropriately cascaded to the other biquadratic circuits. Third order SCF sections can also be used in cascade with the biquadratic circuits for odd transfer functions.[6]

If the filter requirements are already given by its s-domain transfer function, the easier approach is to first factor the transfer function into second order sections. The prewarped s-domain functions are then obtained by prewarping critical frequencies of these second order sections. Then steps (4) onwards can be used. This approach allows different clock frequencies to be used for different sections.

5.5 Design by matching transfer functions

The prewarping step above can be avoided by matching the factored second order s-domain transfer function directly with the z-domain transfer function of the biquads. The s-domain first and second order transfer functions can be expressed, in general, by

$$h_a(s) = \frac{K^s_a(s + \sigma_z)}{s + \sigma_p} \qquad (5:15a)$$

$$h_b(s) = \frac{K^s_b(s^2 + \frac{\omega_z}{Q_z} s + \omega_z{}^2)}{s^2 + \frac{\omega_p}{Q_p} s + \omega_p{}^2} \qquad (5:15b)$$

The corresponding z-domain transfer functions are expressed as

$$H_a(z) = \frac{K^z_a(1 + \gamma' Z^{-1})}{1 + \theta' Z^{-1}} \qquad (5:16a)$$

$$H_b(z) = \frac{K^z_b(1 + \varepsilon' Z^{-1} + \delta' Z^{-2})}{1 + \alpha' Z^{-1} + \beta' Z^{-2}} \qquad (5:16b)$$

The coefficients θ',α' and β' of the denominators in (5:16) can be expressed in terms of the pole frequencies σ_p, ω_p and pole quality factor Q_p of (5:15), which are

$$\theta' = \exp(-\sigma_p/f_c) \qquad (5:17a)$$

$$\alpha' = -2 \exp(-\frac{\Omega_p}{2Q_p}) \cos(\Omega_p \sqrt{1 - \frac{1}{4Q_p{}^2}}) \qquad (5:17b)$$

$$\beta' = \exp(-\frac{\Omega_p}{Q_p}) \qquad (5:17c)$$

where $\Omega = \omega T$ is the normalised frequency, i.e. $\Omega_p = {}^{\omega_p}/_{f_c}$.[7] γ', ε' and δ' are given by similar expressions as for θ', α' and β' respectively, with the subscript p replaced by z.

The matching of the gain of the functions at any desired frequency, ω can be done by noting that

$$\left|1 + uz^{-1} + vz^{-2}\right|_{z=e^{j\Omega}} = \sqrt{1 + u^2 + v^2 + 2v\cos(2\Omega) + 2u(1 + v)\cos\Omega} \qquad (5:18)$$

Thus for gain matching at low (L) frequencies ($s = 0$, $z = 1$), K^z_b can be obtained from (5:15b), (5:16b) and (5:18),

$$K^z_{bL} = \frac{1 + \alpha' + \beta'}{1 + \varepsilon' + \delta'} \left(\frac{\omega_z}{\omega_p}\right)^2 K^s_b \qquad (5:19)$$

For matching at high (H) frequencies ($s = 00$, $z = -1$),

$$K^z_{bH} = \frac{1 - \alpha' + \beta'}{1 - \varepsilon' + \delta'} K^s_b \qquad (5:20)$$

K^z_a can similarly be obtained using (5:18) when $v = 0$.[2] The transfer function of any first or second order switched-capacitor circuit can then be equated to the z-domain transfer function in (5:16) and design equations for the capacitor ratios can be derived.

5.6 Design Example using the Bilinear Transformation

The transfer functions of two biquad sections which when cascaded satisfy the bilinearly-prewarped specification of the OTOB filter are derived in chapter 4. These are

$$H_A(s) = K_A T_A = \frac{K_A s}{s^2 + 0.845999\, s + 35.1098} \qquad (5:21a)$$

$$H_B(s) = K_B T_B = \frac{K_B s}{s^2 + 0.976431\, s + 46.7706} \qquad (5:21b)$$

where $K_T = K_A . K_B = 1.66063$ and $H_T = H_A . H_B$.

The pole-zero pairing in (5:21) is chosen so that both sections can be realised by the BP circuit of fig. 5:5. Both the denominators have the same Q and the zeros are both at s = 0. Thus the sensitivity of the filter to component variations is quite independent of the pole-zero pairings.[5] With respect to the section dynamic ranges equalisation, the pairing in (5:21) is not far below the optimum. Sections with the optimum pairing are discussed in section 5.7.

The overall dynamic range of the filter is also controlled by the ordering of the sections and the gain distribution among the sections, such as K_A and K_B in (5:21). The ordering is determined using the method of minimising the maximum-to-minimum ratios at each biquad output in the cascade.[5] For the sections in (5:21), the ordering has very slight effect on the dynamic range. The section with the lower centre frequency, $H_A(s)$ is chosen to be first in the cascade on the basis it provides more attenuation at high frequencies. In this case, however, it only gives a very slight advantage in terms of antialiasing requirement.

After the pole-zero pairing and ordering of the sections are determined, the gain distribution is done by making all the biquad outputs in the cascade have the same peak voltage. This is achieved for the sections in (5:21) by using

$$K_A = \frac{\max\limits_{0\le\omega<\infty} |H_T|}{\max\limits_{0\le\omega<\infty} |T_A|} \qquad (5:22a)$$

$$K_B = \frac{\max\limits_{0\le\omega<\infty} |H_T|}{\max\limits_{0\le\omega<\infty} |T_A T_B|} = \frac{K_T}{K_A} \qquad (5:22b)$$

Thus $K_A = 0.845999$ and $K_B = 1.96292$.

The transfer functions in (5:21) are now fully determined. Firstly, the biquad corresponding to the transfer function in (5:21a) is designed. With the circuit in fig. 5:5, two designs are possible, using either $H_1(z)$ or $H_2(z)$ in (5:11) and (5:12) respectively. The design equations are obtained by comparing these to (5:14) with $a_2 = a_o = 0$. The denominators are the same in both cases.

As examples, the coefficients of z^{-1}, z^{-2} in the denominator of (5:11) are equated to those of (5:14) to give respectively

$$ER + E'R - 2 = 2m\,(b_oT^2/4 - 1) \qquad (5:23a)$$

$$1 - E'R = m(1 - b_1T/2 + b_oT^2/4) \qquad (5:23b)$$

where

$$m = 1/(1 + b_1T/2 + b_oT^2/4) \qquad (5:23c)$$

If R is first chosen to be unity, then

$$E = mb_oT^2\ ,\ E' = mb_1T \qquad (5:24)$$

The expressions for the other capacitor ratios can similarly be obtained and are given in Table 5:2.

Table 5:2 Expressions for capacitor ratios of the circuit in fig. 5:5 with its transfer functions equated to (5:14). $a_2 = a_o = 0$.

Capacitor ratio	$H_1(z)$	$H_2(z)$
R	1	
E'	mb_1T	
E	mb_oT^2	
K	$a_1/(b_oT)$	$ma_1T/2$
A	$ma_1(T/2 + b_1/b_o)$	ma_1T
$m = 1/(1 + b_1T/2 + b_oT^2/4),\quad T = 1/f_c$		

From Table 5:2, the unscaled capacitor values can be calculated for the transfer function in (5:21a). These are shown in Tables 5:3 and 5:4 for the designs using $H_1(z)$ and $H_2(z)$ respectively. The extra degree of freedom in R can be used to maximise the dynamic range within the biquad. This is achieved by making the outputs V_1 and V_2 of the OAs in the biquad of fig. 5:5 have the same peak voltage.

For the design using $H_1(z)$, the voltage level of V_2 needs to be adjusted without affecting the gain level of $H_1(z)$. This can be done by scaling all the capacitors connected to V_2, i.e. C_2, EC_1 and $E'C_1$. Thus if the gain level of $H_2(z)$ is to be scaled by μ, then these capacitors must be scaled by $1/\mu$. When using the $H_2(z)$ design, the capacitors C_1 and RC_2 connected to V_1 have to be similarly scaled according to the gain adjustment made to $H_1(z)$. These scaled capacitor values are also shown in Tables 5:3 and 5:4.

Note that after the adjustment, E becomes approximately equal to R. E and R actually represent the gains for the two integrators of the biquad circuit. Thus for a quick design, a near optimum solution for maximum dynamic range can be obtained by making these gains equal when deriving the capacitor ratio expressions as in Table 5:2.[1]

Finally, the admittances associated with each stage are adjusted so that the minimum capacitance value in the circuit becomes unity. This allows easy comparison of the capacitor spread and the total capacitance required by the biquad in each design. Two groups of capacitors may be scaled together. One group consists of C_1, AC_1, EC_1 and $E'C_1$ which are all connected to the negative input of OA 1 in fig. 5:5. The others are C_2, KC_2 and RC_2 connected to the negative input of OA 2. Thus the final capacitor values in Tables 5:3 and 5:4 are obtained.

Table 5:3 Capacitor values for the circuit in fig. 5:5 realising $H_A(s)$ with $H_1(z)$ design (using bilinear transformation).

Capacitor	Unscaled	Dynamic-Range-Adjusted $\mu = 0.35116$	Final
C_1	1.0000		22.654
$E'C_1$	0.049848	0.14195	3.2158
EC_1	0.12930	0.36819	8.3411
AC_1	0.044142		1.0000
C_2	1.0000	2.8477	7.3864
RC_2	1.0000		2.5938
KC_2	0.38553		1.0000
		Total capacitance (pF)	46.2

Table 5:4 Capacitor values for the circuit of fig. 5:5 realising $H_A(s)$ with $H_2(z)$ design (using bilinear transformation).

Capacitor	Unscaled	Dynamic-Range-Adjusted $\mu = 2.8096$	Final
C_1	1.0000	0.35592	7.1401
$E'C_1$	0.049848		1.0000
EC_1	0.12930		2.5938
AC_1	0.049848		1.0000
C_2	1.0000		40.122
RC_2	1.0000	0.35592	14.280
KC_2	0.024924		1.0000
		Total capacitance (pF)	67.1

It is observed that the design using $H_1(z)$ provides a lower total capacitance and smaller capacitor spread. However, the $H_2(z)$ may afford the less sensitive realisation.[4] Comparing (5:11) and (5:12), the numerator coefficients of $H_1(z)$ are more dependent on the cancellation of terms than those of $H_2(z)$. On the other hand, $H_1(z)$ has pole-zero dependence property which can have a beneficial effect on sensitivity. Thus the advantage in capacitance saving has to be compared with the sacrifice in sensitivity, if any, before a choice between the two designs can be made.

Hence both designs are also used for the biquad to realise the transfer function in (5:21b). The final capacitor values are shown in Table 5:5. The complete circuit for the OTOB filter is obtained by appropriately cascading the biquads realising the two transfer functions in (5:21). The total capacitance with the $H_2(z)$ design is 106.0 pF and the capacitor spread is 1:40.1. The $H_1(z)$ design requires a total capacitance of 69.8 pF and has capacitor spread of 1:22.7.

If the design were to be done using the other cascade sequence, i.e. having $H_B(s)$ first in the cascade, the total capacitance for the filter with the $H_1(z)$ design is 69.5 pF and the capacitor spread is 1:21.1. Thus the differences in this context are very slight. Also, there are other SC BP circuits, derivable from the general biquad in fig. 5:1, which can realise $H_A(s)$ and $H_B(s)$ through the bilinear transformation. These circuits, such as those using switched-capacitor damping, however, have larger capacitor spread and larger total capacitance for this particular filter realisation.

Table 5:5 Capacitor values for the circuit in fig. 5:5 realising $H_B(s)$ with $H_1(z)$ and $H_2(z)$ designs (using bilinear transformation)

Capacitor (pF)	$H_1(z)$	$H_2(z)$
C_1	10.518	7.1790
$E'C_1$	1.4844	1.0000
EC_1	4.4438	2.9937
AC_1	1.0000	2.0104
C_2	3.7063	17.544
RC_2	1.4892	7.1422
KC_2	1.0000	1.0000
Total	23.6	38.9

5.7 Realising sections with the optimum pole-zero pairing

The optimum pole-zero pairing for section dynamic range equalisation is obtained when both zeros of the fourth order BP function are paired with the closest poles. Thus the filter is made up of a highpass and a lowpass section. Their transfer functions are

$$H_H(S) = \frac{K_H S^2}{s^2 + 0.845999\ s + 35.1098} \qquad (5:25a)$$

$$H_L(S) = \frac{K_L}{s^2 + 0.976431\ s + 46.7706} \qquad (5:25b)$$

where $K_T = K_L . K_H = 1.66063$ as before. The ordering of these sections has no significant effect on the dynamic range.

The bilinear transform of the transfer functions in (5:25) can be realised by circuits of similar structure to that of fig. 5:5. The HP

circuit can be realised with A = C = 0 for the $H_2(z)$ design or with K = M = 0 for the $H_1(z)$ design. The LP circuit is realised for the $H_2(z)$ design when C = 0 and for the $H_1(z)$ design when C = 0 and $K \neq M$. Considering both possible ordering of the sections, the OTOB filter is designed using both the $H_1(z)$ and $H_2(z)$ designs. The capacitance requirement and the capacitor spread for each case are shown in Table 5:6.

Table 5:6 Total capacitance (pF) for the OTOB filter using sections with optimum pole-zero pairing. Capacitor spreads are given in brackets.

Ordering \ Design	$H_1(z)$	$H_2(z)$
$H_L.H_H$ K_L=6.6607, K_H=0.24932	85.8 (1:24.8)	280.8 (1:165.5)
$H_H.H_L$ K_H=0.14241, K_L=11.661	56.7 (1:14.2)	173.2 (1:94.5)

Table 5:6 shows that the least total capacitance is obtained using the $H_1(z)$ design when the HP section is placed first in the cascade. The complete circuit for this realisation is shown in fig. 5:6. Note that the SC element transformation of fig. 5:3(d) is used for K and M to reduce the total capacitance and the number of switches. The capacitor values are also shown in the same figure. Though this realisation affords the least total capacitance and the optimum with respect to maximising the possible signal level, it is often not desirable to have the HP section at the beginning of the cascade. This ordering is only suitable if the input is expected to have a sizeable dc or low frequency, out-of-band components.[5]

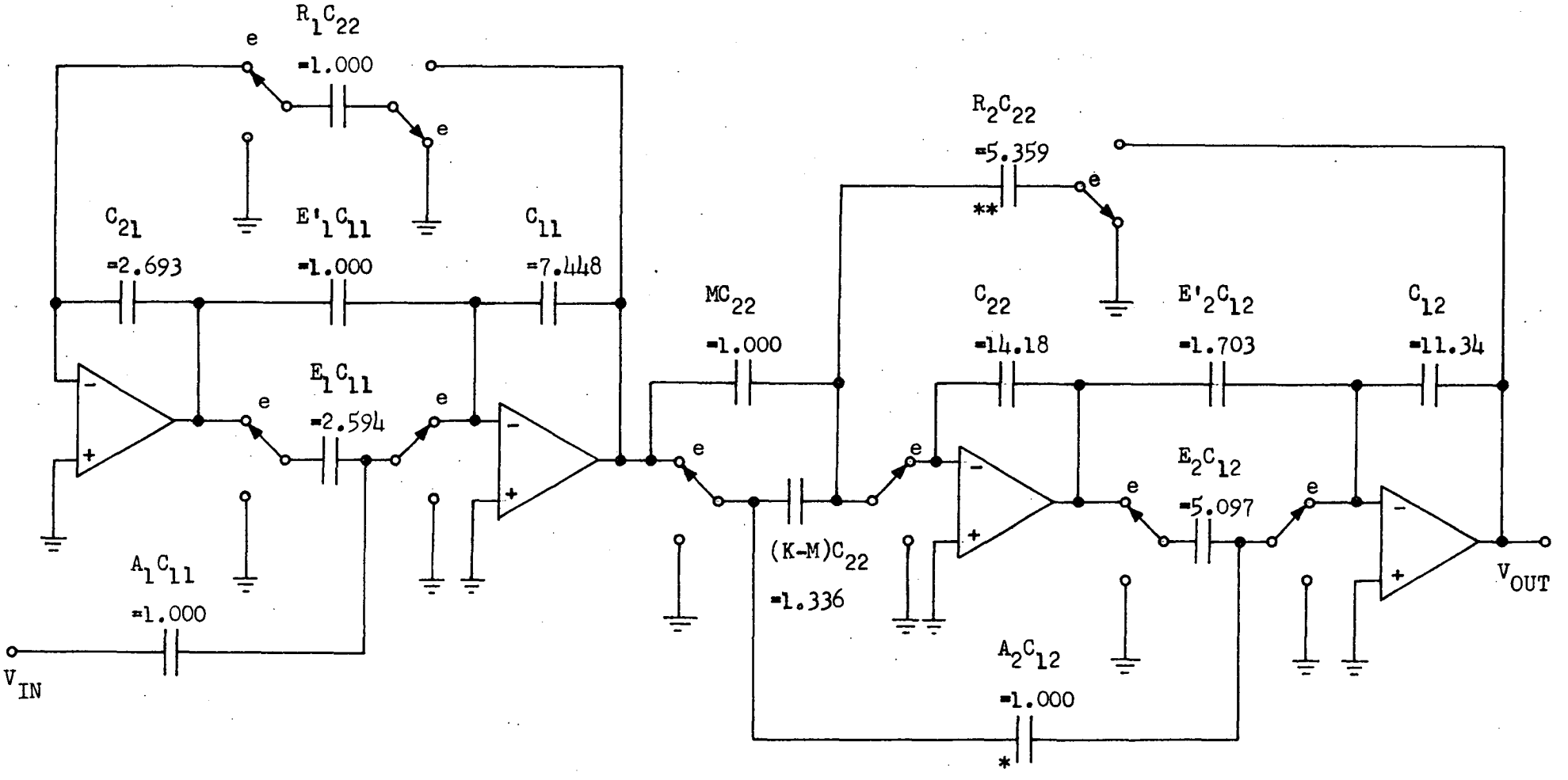


Fig. 5:6 Switched-capacitor one third octave bandpass filter using cascaded high-pass and low-pass sections. (Capacitor values in pF, $f_c = 16 f_m$).

Otherwise it is desirable to have either a LP or a BP section at the beginning of the cascade for simpler antialiasing requirement as well as preventing strong high frequency noise from entering the succeeding stages of the cascade. Also, it is desirable to have either a HP or a BP at the end of the cascade to eliminate dc offsets of the preceeding stages and to reduce intenrally generated low-frequency noise. Under these considerations, usage of two BP sections for the filter provides a better solution.

5.8 Design Examples by matching transfer functions

The two cascaded biquadratic functions which satisfy the specification for the OTOB are given by

$$h_A(s) = \frac{0.822243\ s}{s^2 + 0.822243\ s + 34.2865} \qquad (5:26a)$$

$$h_B(s) = \frac{1.90294\ s}{s^2 + 0.946754\ s + 45.4566} \qquad (5:26b)$$

These are derived from chapter 4 following the same considerations as in section 5.6. Also, the same BP10 realisation from the circuit in fig. 5:5 is used for this design. Thus the z-domain transfer function, obtained from (5:16b) with $\varepsilon' = 0$, $\delta' = -1$, is

$$H(z) = \frac{K^z(1 - z^{-2})}{1 + \alpha' z^{-1} + \beta' z^{-2}} \qquad (5:27)$$

The transfer functions in (5:26) can be written in the form of (5:15b), i.e.

$$h(s) = \frac{K^s \frac{\omega_p}{Q_p} s}{s^2 + \frac{\omega_p}{Q_p} s + \omega_p^2} \qquad (5:28)$$

Hence, the values for α' and β' can be obtained using (5:17). The value of K^z is obtained by matching the peak gain of the bandpass functions in (5:27) and (5:28) at ω_p. Using (5:18),

$$K^z = K^s \frac{\sqrt{1 + (\alpha')^2 + (\beta')^2 + 2\beta'\cos(2\Omega_p) + 2\alpha'(1 + \beta')\cos\Omega_p}}{2\sin\Omega_p} \qquad (5:29)$$

The capacitor ratio expressions for the $H_1(z)$ and $H_2(z)$ designs can now be derived in terms of α', β' and K^z by comparing (5:11) and (5:12) with (5:27). These are shown in Table 5:7. The $H_1(z)$ design is used to design the SC biquads for the transfer functions in (5:25). Using Table 5:7 and following similar steps as in section 5.6, the final capacitor values for realising $h_A(s)$ and $h_B(s)$ are shown in Table 5:8. Comparison of these values with those achieved in Tables 5:3 and 5:5, shows that the matching technique provides a very close approximation to the desired transfer function as provided by using the bilinear transformation.

Thus this technique is further used to design the OTOB filter with a higher clock frequency. A clock frequency of fc = 48fm is chosen. In this case, the antialiasing requirement can be met by just a second-order continuous time filter such as the Sallen & Key section. It has been noted earlier that the use of high clock frequency will cause the required total capacitance for the circuit to increase. The higher clock to midband frequency ratio, however, may allow the BP01 and BP00 realisations to be used. These circuits usually require a lower total capacitance.

Table 5:7 Expressions for capacitor ratios of the circuit in fig. 5:5 with its transfer functions equated to (5:27).

Capacitor Ratio	$H_1(z)$	$H_2(z)$
R	1	
E'	$1 - \beta'$	
E	$1 + \alpha' + \beta'$	
K	$2K^z/E$	K^z
A	$K^z(3 + \alpha' - \beta')/E$	$2K^z$

Table 5:8 Capacitor values for the circuit in fig. 5:5 realising $h_A(s)$ and $h_B(s)$ with $H_1(z)$ design (using matching technique).

Capacitor (pF)	$h_A(s)$	$h_B(s)$
C_1	22.481	10.331
$E'C_1$	3.2098	1.4774
EC_1	8.2725	4.3682
AC_1	1.0000	1.0000
C_2	7.3461	3.6615
RC_2	2.5772	1.4710
KC_2	1.0000	1.0000

Using the matching technique and the quick design method suggested in section 5.6, designs are carried out on all possible realisations given in Table 5:1 with $f_c = 16\ f_m$ and $fc = 48\ f_m$. These simple designs

can be used to compare the total capacitance required by each realisation of the OTOB filter and the effect of the clock frequency on the capacitance requirement. The results are shown in Table 5:9 together with the capacitor spread of each realisation.

It is observed from Table 5:9 that the BP01 realisation using the $H_2(z)$ design gives the least total capacitance and capacitor spread. It also requires one less capacitor than the other realisations, since K = 0. The increase in clock frequency only results in a slight increase in the capacitance requirement. The high frequency attenuation of this realisation, however, will no longer be enhanced as the case for the BP10 realisation. With fc = 16 fm, at 4 fm and 8 fm the attenuations are 49.3 dB and 56.0 dB respectively which do not satisfy the specification. This effect is less significant when using the higher clock frequency. With fc = 48 fm, the attenuations at 4 fm and 8 fm are 50.8 dB and 63.1 dB respectively which satisfy the required attenuation given in chapter 4.

Table 5:9 Total capacitance (pF) required for the OTOB filter using the realisations given in Table 5:1. The capacitor spreads are given in brackets.

Design	$H_1(z)$		$H_2(z)$	
Clock frequency	16 fm	48 fm	16 fm	48 fm
BP10	69 (1:23)	89 (1:36)	106 (1:40)	215 (1:118)
BP01	52 (1:15)	73 (1:27)	32 (1:7)	40 (1:8)
BP00	138 (1:52)	120 (1:51)	67 (1:20)	120 (1:59)

The z^{-1} factor in the BP01 function constitutes a delay which is usually immaterial. However, if additional feedback is required around

the biquad, this delay term becomes critical.[4] Thus, for cascade realisations where very high clock frequency is necessary, the BP01 circuit will be the best choice with a greatly reduced capacitance requirement. However, if the advantages of the bilinear transformation are desired then the $H_1(z)$ design with the BP10 realisation requires a reasonable amount of capacitance. Also, the increase in capacitance with clock frequency is not very drastic for this case. The complete circuits for these minimum capacitance BP01 and BP10 realisations of the OTOB filter are given in figs 5:7 and 5:8 respectively. The capacitor values for the BP10 circuits with $f_c = 16f_m$ are given in Table 5:8. Using similar procedures the capacitor values are obtained for the BP01 and BP10 circuits with $f_c = 48f_m$ and are given on the figures.

5.9 Summary

This chapter describes a variety of design possibilities using SC biquads. A general SC biquadratic structure is first given from which all second-order filter transfer functions can be generated. In particular, a circuit is derived which can realise the bandpass transfer functions, BP10, BP01 and BP00 where both inverting and non-inverting functions are available. The capacitor values of the SC biquad circuit are designed by using either the bilinear transformation or the matching technique.

SCFs meeting the OTOB specification are obtained by either cascading two BP sections or cascading an LP and an HP section. Among the satisfactory cascaded BP circuits, the cascaded non-inverting BP10 realisation affords the least total capacitance when the clock to midband frequencies ratio is low. If the ratio is high, then the cascaded inverting BP01 realisation requires the least total capacitance.

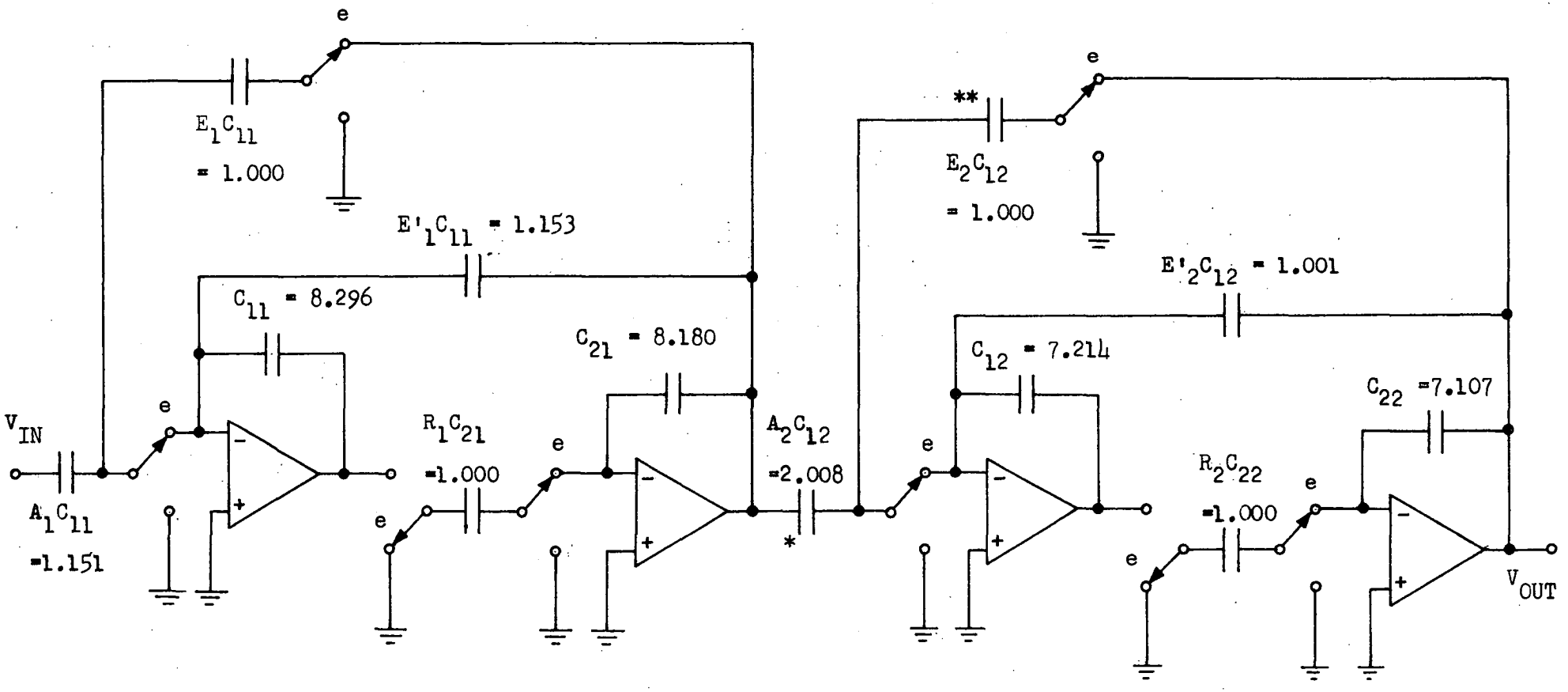


Fig. 5:7 Switched-capacitor OTOB filter using cascaded BP01 sections.
(Capacitor values in pF, $f_c = 48f_m$)

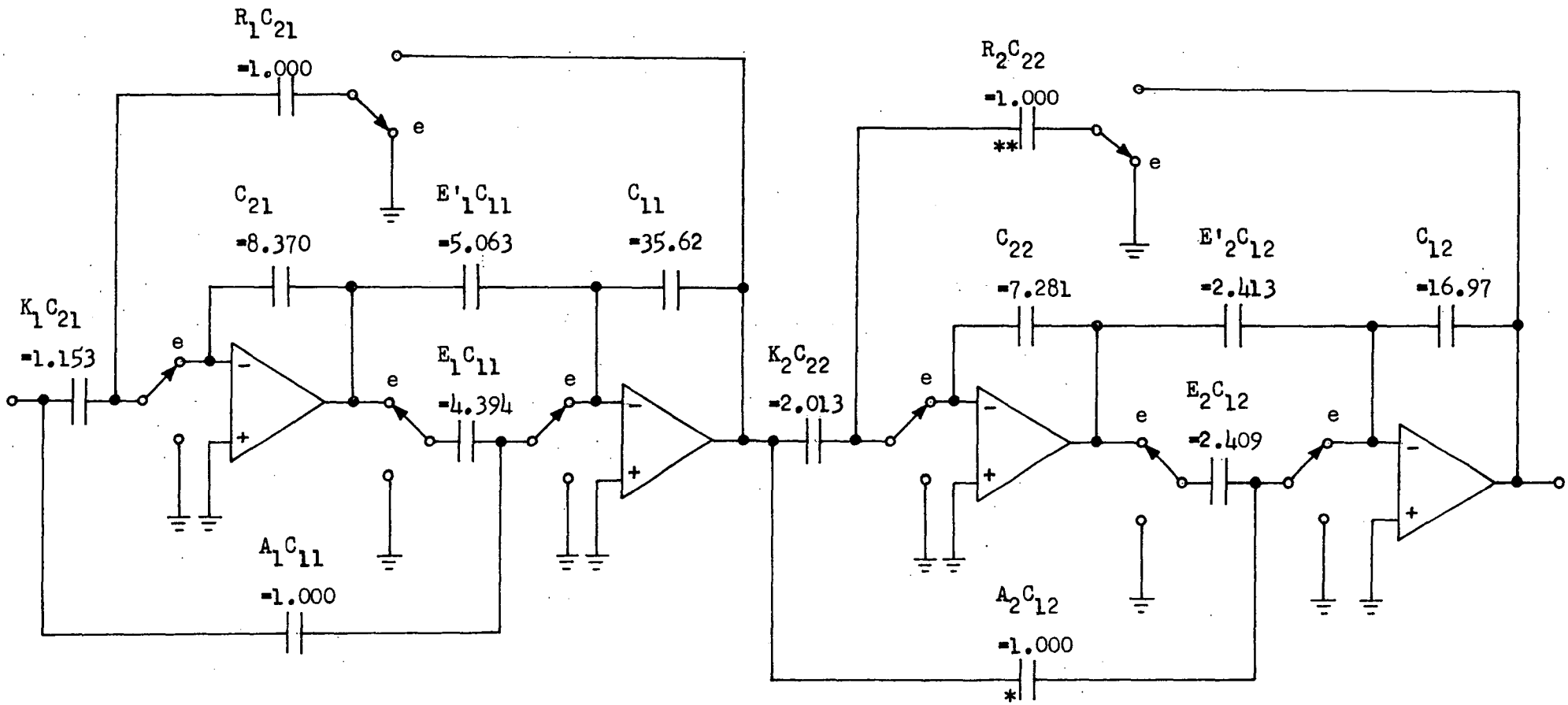


Fig. 5:8 Switched-capacitor OTOB filter using cascaded BP10 sections.
(Capacitor values in pF, $f_c = 48f_m$)

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CHAPTER SIX

SWITCHED-CAPACITOR LADDER FILTERS

It has been shown in chapter 5 that high order switched-capacitor filters can be realised by cascading switched-capacitor biquads. Another method of designing high order SCF is by simulating the doubly terminated LC ladder network which is the subject of this chapter. The SC biquad has sensitivity to component variation which is at least comparable to any active-RC biquad. However, cascading the non-interacting biquad sections result in sensitivity which is the sum of the sensitivity for each of the sections. Thus, as the order of the filter increases, the cascade can be too sensitive to meet high precision filtering requirement.

On the other hand, the ladder filters can be made to have the minimum sensitivity possible when designed for maximum power transfer. The passive ladder networks have been simulated exactly in active filters through the leapfrog or active ladder systhesis using integrators. Thus SCF can also similarly simulate the passive ladder network by using switched-capacitor integrators. Through this approach, the low sensitivity property is retained and large dynamic range is possible in the SCF. This chapter describes the development in the design methods for the SC ladder filters and designs for the SC OTOB filter are given as examples.

6.1 Design using LDI transformation

This design method starts by transforming the differential equations describing the passive ladder network into a signal flow graph. This graph is manipulated in order to obtain a representation which can be realised using integrators. Then the graph can easily be transformed into a SC circuit.[1] The parasitic insensitive LDI integrators such as given in

the two-integrator loop in fig. 3:5 are very suitable in this realisation. The detailed design procedures are illustrated by designing the SC OTOB filter using this method.

The RLC ladder network which can meet the specification for the OTOB filter is given in fig. 6:1. A complete set of loop and node equations for the ladder network which involves only integrations is given below,

$$V_3 = V_{IN} - V_1 - V_2 - V_4 \qquad (6:1a)$$

$$V_1 = I_1 R_1 \qquad (6:1b)$$

$$V_2 = I_1 \frac{1}{sC_A} \qquad (6:1c)$$

$$V_4 = I_2 \frac{1}{sC_B} \qquad (6:1d)$$

$$I_1 = V_3 \frac{1}{sL_A} \qquad (6:1e)$$

$$I_3 = V_4 \frac{1}{sL_B} \qquad (6:1f)$$

$$I_4 = \frac{V_4}{R_2} \qquad (6:1g)$$

$$I_2 = I_1 - I_3 - I_4 \qquad (6:1h)$$

A signal flow graph (SFG) representing these equations is given in fig. 6:2. It shows that four integrators are required with two of them damped to incorporate the terminations of the ladder network. The implementation of this graph by the SC circuit is shown in fig. 6:3.

The summations at the relevant nodes and the switch phasing are appropriately arranged using the two-integrator loop of fig. 3:5 to achieve the SC circuit realising the LDI transformation. This necessitates the inversion of the path with $1/sC_A$ in the SFG and the corresponding inversion of the path out of V_2. The capacitor ratios can be obtained by

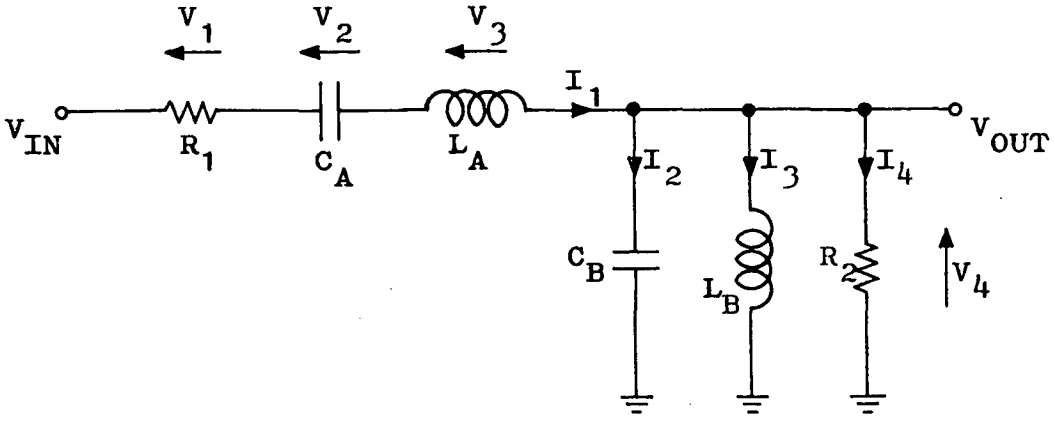


Fig. 6:1 Doubly terminated LC fourth-order bandpass filter.

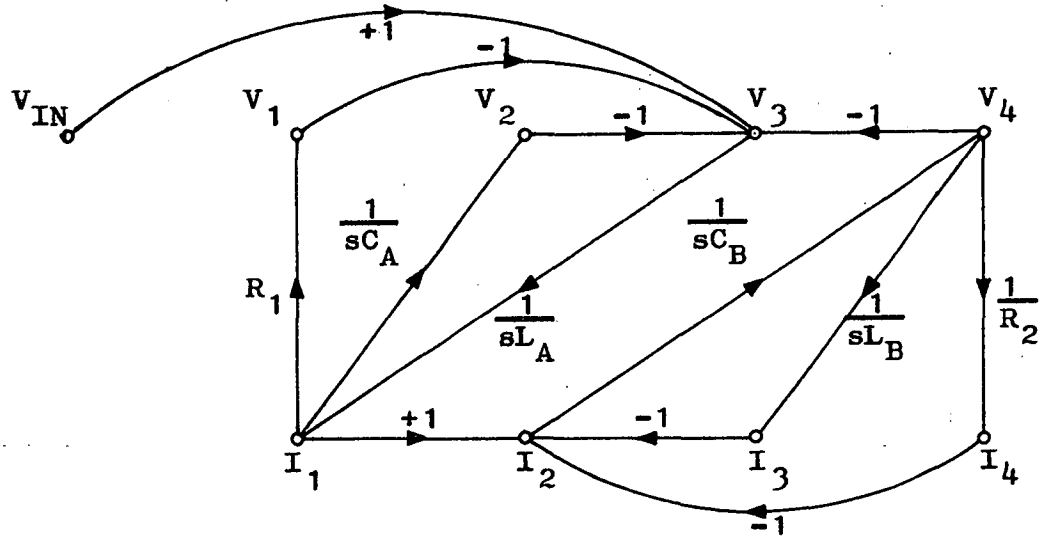


Fig. 6:2 A signal flow graph describing the LC ladder of fig. 6:1.

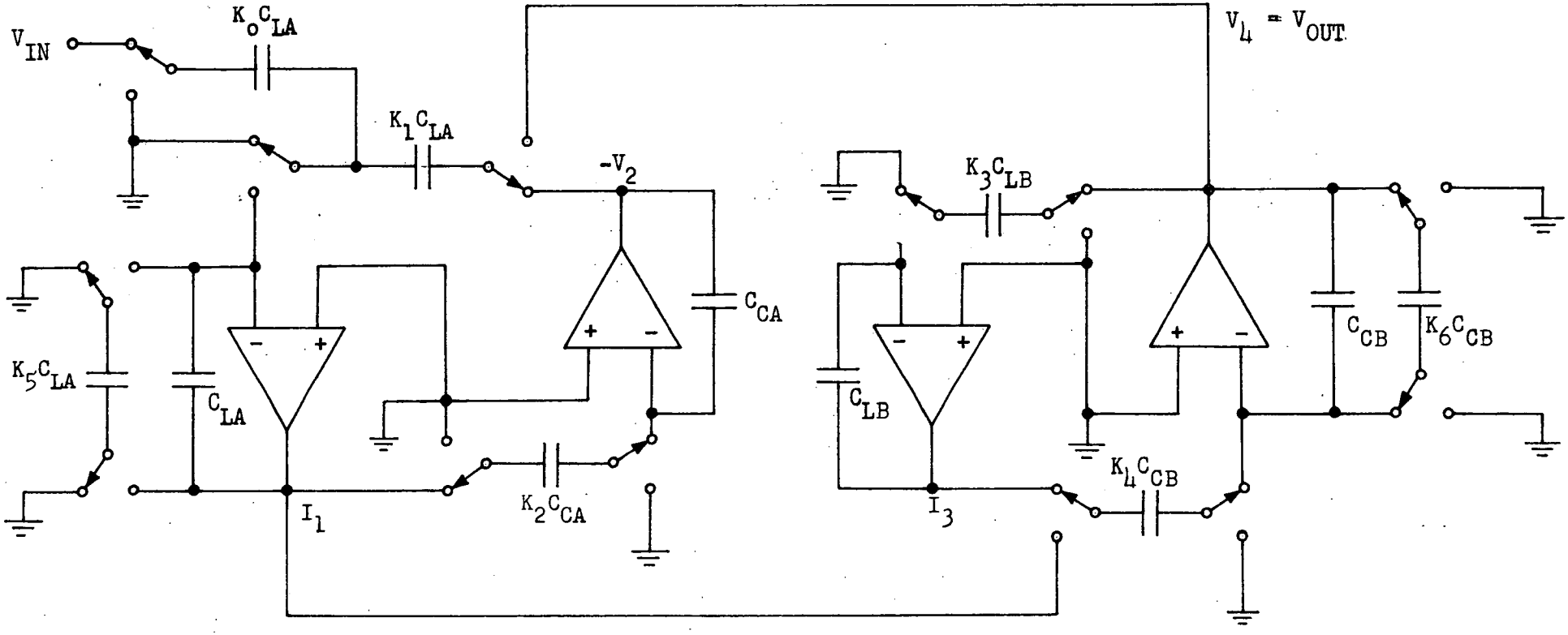


Fig. 6:3 A switched-capacitor implementation of the LC ladder in fig. 6:1

observing figs 6:2 and 6:3, and comparing equations (3:23), (3:24), (3:25) and (6:1). Note that, in this case, the $z^{-\frac{1}{2}}$ term associated with the terminations is approximated by 1, i.e. the circuit in fig. 3:12 is used for the damped SC integrators. The capacitor ratios are given by

$$K_1 = \frac{T}{L_A} \quad , \quad K_2 = \frac{TR_1}{L_A}$$

$$K_2 = \frac{T}{C_A} \quad , \quad K_3 = \frac{T}{L_B} \qquad (6:2)$$

$$K_4 = \frac{T}{C_B} \quad , \quad K_6 = \frac{T}{R_2 C_B}$$

The approximation used for the termination introduces distortion in the frequency response of the filter. As mentioned in chapter 3, this distortion can be made negligible by having a very high clock frequency compared to the frequencies of interest. The following sections describe other methods which can reduce this distortion when lower clock frequency has to be used.

6.2 Minimising distortion by correcting the pole locations

The switched-capacitor implementation of the ladder filter in fig. 6:3 can be represented by the discrete-time flow diagram shown in fig. 6:4. The LDI integrators are represented by the appropriate blocks in the figure. The approximation used in fig. 6:3 results in the termination paths having the $z^{\frac{1}{2}}$ term, i.e. a minus one-half delay, instead of a constant term. The transfer function of the SC circuit can be derived from fig. 6:4, i.e.

$$H(z) = \frac{K_N z^{-1}(1 - z^{-1})^2}{\beta_o + \beta_1 z^{-1} + \beta_2 z^{-2} + \beta_3 z^{-3} + z^{-4}} \qquad (6:3)$$

where

$$\beta_o = (1 + K_1)(1 + K_4) \qquad (6:4a)$$

$$\beta_1 = (1 + K_4)(K_1K_2 - K_1 - 2) + (1 + K_1)(K_3K_4 - K_4 - 2) + K_1K_4 \qquad (6:4b)$$

$$\beta_2 = (K_1K_2 - K_1 - 2)(K_3K_4 - K_4 - 2) + (1 + K_1) + (1 + K_4) - 2K_1K_4 \qquad (6:4c)$$

$$\beta_3 = (K_1K_2 - K_1 - 2) + (K_3K_4 - K_4 - 2) + K_1K_4 \qquad (6:4d)$$

$$K_N = K_oK_4 \qquad (6:4e)$$

The distortion in the filter magnitude function due to the approximation used is minimised by moving the poles of (6:3) back to the "correct" positions.[2] These "correct" poles are determined by mapping the analogue pole positions to the z-plane such that the LDI transformation in (3:10) is satisfied. For a pole $s_k = \delta_k + j\Omega_k$ in the s-plane, where $\delta_k < 0$, let $\hat{s} = sT$ and $P = z^{\frac{1}{2}}$. Then (3:10) yields

$$P^2 - \hat{s}_kP - 1 = 0 \qquad (6:5)$$

One of the roots of (6:5), say P_{k1}, will be inside the unit circle in the P-plane. The correct value of z_k corresponding to s_k is then given by

$$z_k = P_{k1}^2 \qquad (6:6)$$

From these "correct" pole positions, a new set of values for β's in (6:3) are obtained. Using these new values, the non-linear equations (6:4) can then be solved for the correct values of the capacitor ratios, K_1, K_2, K_3 and K_4. In this case, $K_5 = K_6 = 1$. The modification of the capacitor ratios as above will affect the sensitivity characteristics of the ladder structure.[2] Thus the trade-offs between achieving optimum

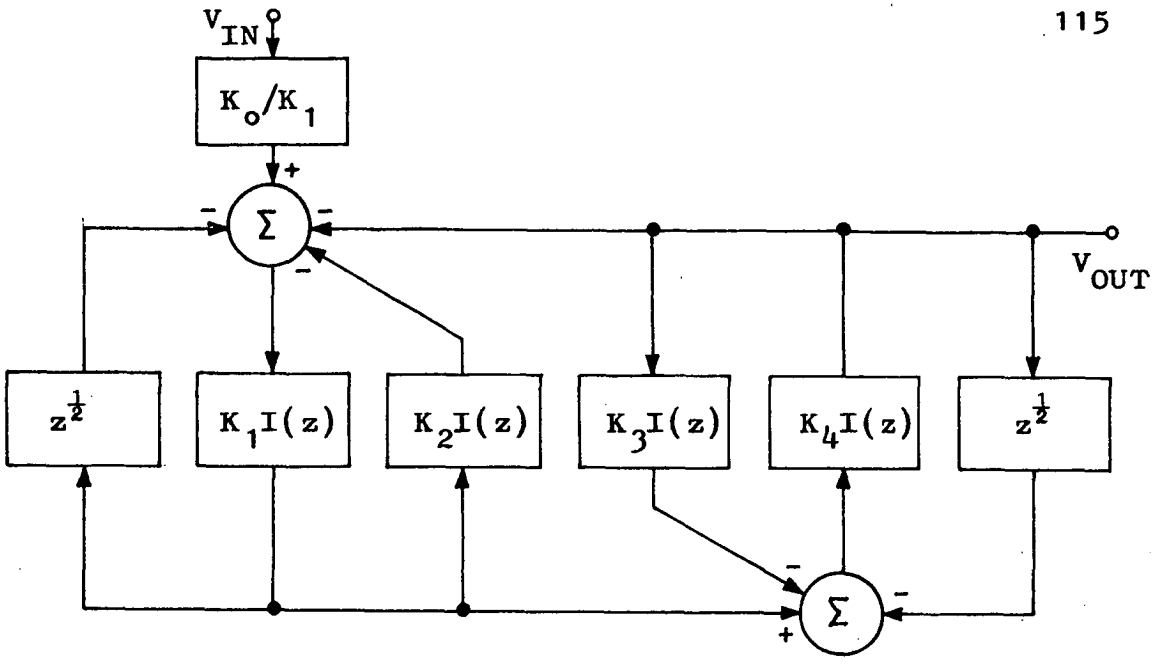


Fig. 6:4 Discrete-time flow diagram of the switched-capacitor ladder filter of fig. 6:3. $R_1=R_2=1$, $I(z) = 1/(z^{\frac{1}{2}} - z^{-\frac{1}{2}})$.

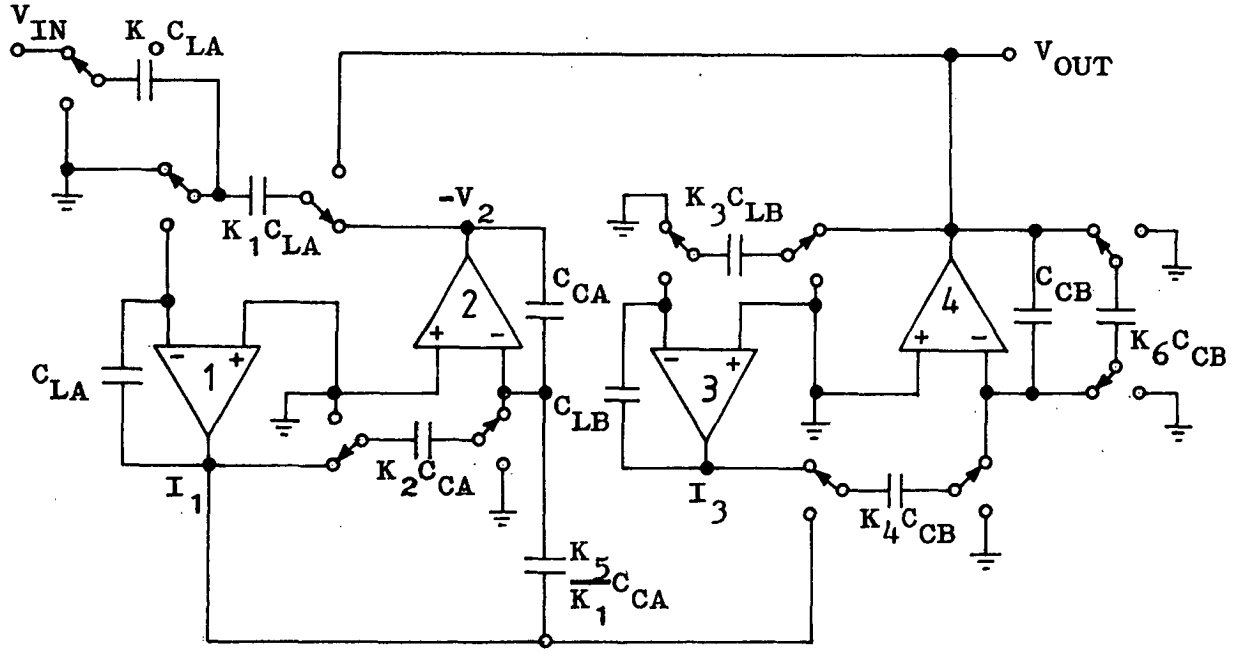


Fig. 6:5 A switched-capacitor ladder filter with complex conjugate terminations simulating the circuit in fig. 6:1.

magnitude response and sensitivity of the filter have also to be examined. Furthermore the transfer function as in (6:3) will become more involved when higher order filters are designed.

6.3 Minimising distortion by using complex-conjugate terminations

This method involves replacing one of the $z^{\frac{1}{2}}$ terms in the termination paths in fig. 6:4 by $z^{-\frac{1}{2}}$, which is the complex conjugate of $z^{\frac{1}{2}}$. The error for a doubly terminated ladder network with complex-conjugate terminations is expected to be less than that for the case when they are not complex conjugates. It has been shown in [3] that a first order improvement can be expected for the SCF with complex conjugate terminations.

The $z^{-\frac{1}{2}}$ term, i.e. an extra half delay in the termination path can be implemented by using the circuit of fig. 3:13(b). The feedback loop in this circuit has a full clock cycle delay as shown in eqn (3:26). For bandpass circuits, another method can be used to implement a full clock cycle delay around the integrator to realise the LDI termination with an extra half delay.

This is shown in fig. 6:5 where there is an extra half delay in the source termination. The output I_1 of the source integrator is inverted through OA 2 and fed back via the non-inverting input of the source integrator. Thus the SC circuit in fig. 6:5 realises the filter with comples conjugate terminations where the capacitor ratios are simply given by (6:2).

6.4 Minimising distortion by using bilinear terminations

It has been shown in chapter 3 that less distortion is obtained if the approximation (c) is used. The LDI integrator with bilinear damping

implementing this approximation is given in fig. 3:14. Using this integrator for the SC OTOB ladder filter results in the same circuit as in fig. 6:3. However the capacitor ratios for the source and load integrators have to be modified. From fig. 3:16,

$$K_1 = \frac{C_1/C_2}{1 - C_5/2C_2} \qquad (6:7)$$

where C_1/C_2 is the ratio of the input SC to the integrating capacitor and C_5/C_2 is the ratio of the feedback SC to the integrating capacitor. Using (6:2) and equation such as (6:7), the modified capacitor ratios for the filter are given by

$$K_1 = \frac{T/L_A}{1 - TR_1/2L_A} \quad , \quad K_5 = \frac{TR_1/L_A}{1 - TR_1/2L_A}$$

$$K_4 = \frac{T/C_B}{1 - T/2R_2C_B} \quad , \quad K_6 = \frac{T/R_2C_B}{1 - T/2R_2C_B} \qquad (6:8)$$

K_2 and K_3 are the same as in (6:2).

6.5 Design Examples

The SC OTOB ladder filter is designed here using the method given in section 6.4. A reasonably low clock frequency, fc = 24fm is chosen. The specification is prewarped according to (3:11) as shown in chapter 4, from which the element values of the LC ladder are obtained. These are given in fig. 6:6. When using a very high clock frequency compared to the frequencies of interest, the specification may not be prewarped. For lower clock frequency, prewarping may also be avoided by using the approximation whereby T in the capacitor ratio expression is adjusted to

$$T' = \frac{2 \sin \omega_o T/2}{\omega_o} \qquad (6:9)$$

where ω_o is the critical frequency in the filter response.[4]

It is also desired for the SC realisation of the ladder network to be scaled for maximum dynamic range. This is done by analysing the passive circuit to determine the maxima of the relevant voltages and currents. These maxima are then used to scale the capacitor ratios such that the maximum outputs of the OAs in the SC circuits are all equal for a constant-amplitude swept frequency input.[5]

In the SC realisation of the RLC ladder, the OA outputs simulate I_1, V_2, I_3 and V_4. The maxima of these values are obtained by analysing the ladder network of fig. 6:6 using a constant amplitude of IV and are given in Table 6:1. In scaling the capacitor ratios using these maxima, it can be observed in fig. 6:3 that for K_1C_{LA}, two different capacitors are required to scale the OA outputs V_2 and V_4. Similarly, two different capacitors are required for K_4C_{CB}.

The SC implementation of the RLC ladder of fig. 6:6 with optimum dynamic range is given in fig. 6:7 where switch sharing is implemented to reduce the number of switches. The expressions for the scaled capacitor ratios are given in Table 6:2. The capacitor values for fc = 24fm are also given in the table where they have been adjusted so that the minimum capacitor value in the circuit is unity. Using the same procedure as above, the SC OTOB ladder filter is also designed with a clock frequency of fc = 48 fm. The final capacitor values are also given in Table 6:2.

Table 6:1 Voltage and current maxima for the circuit in fig. 6:6 with 1V input sinusoid.

Voltage or current	Maxima symbol	Maximum value
I_1	M_1	0.63601A
V_2	M_2	4.96015V
I_3	M_3	3.69892A
V_4	M_4	0.50000V

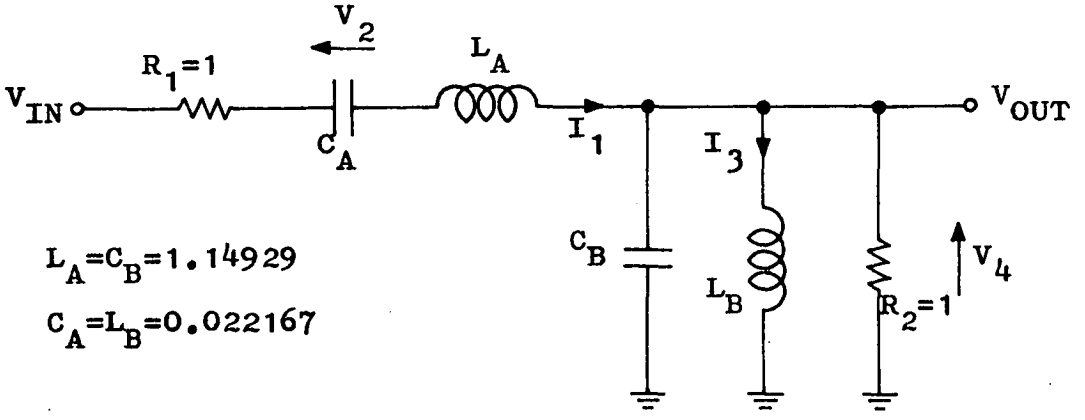


Fig. 6:6 RLC ladder meeting the LDI-prewarped specification for the OTOB filter, $f_c = 24f_m$.

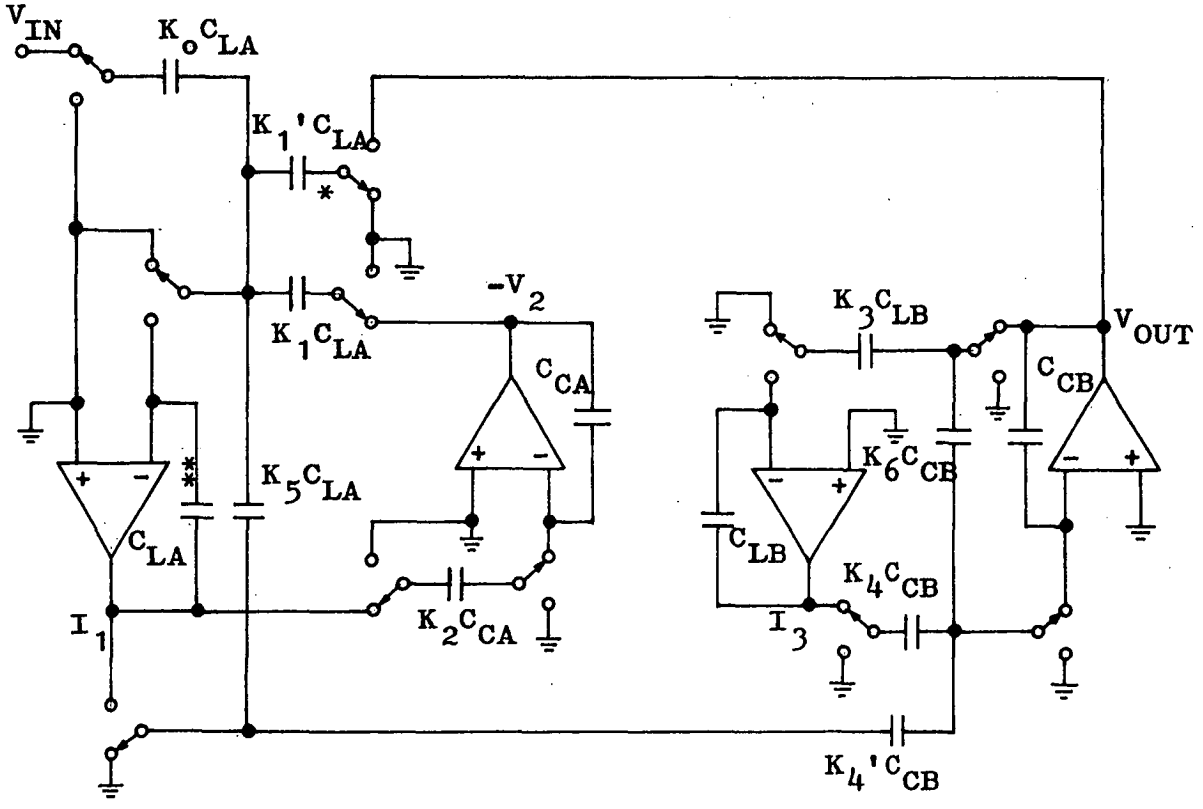


Fig. 6:7 An optimum dynamic range switched-capacitor implementation of the circuit in fig. 6:6.

Table 6:2 Design data for the circuit in fig. 6:7 with fc = 24fm and 48fm.

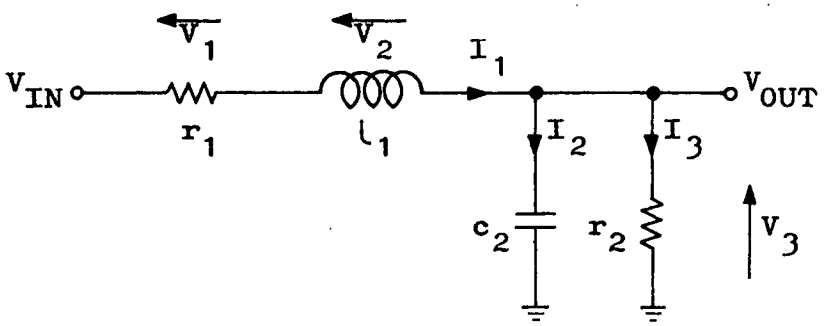
Capacitor Ratio Expressions	Capacitors	Capacitor Values fc = 24fm	fc = 48fm
$K_5=(\frac{TR_1}{L_A})/(1-\frac{TR_1}{2L_A})$	K_5C_{LA}	1.2720	1.2720
$K_o=\frac{1}{M_1}K_5$	K_oC_{LA}	2.0000	2.0000
$K_1=(\frac{M_2}{M_1}\frac{T}{L_A})/(1-\frac{TR_1}{2L_A})$	K_1C_{LA}	9.9201	9.8769
$K_1'=(\frac{M_4}{M_1}\frac{T}{L_A})/(1-\frac{TR_1}{2L_A})$	$K_1'C_{LA}$	1.0000	1.0000
	C_{LA}	34.449	69.051
$K_2=\frac{M_1}{M_2}\frac{T}{C_A}$	K_2C_{CA}	1.0000	1.0000
	C_{CA}	4.1491	8.2834
$K_3=\frac{M_4}{M_3}\frac{T}{L_B}$	K_3C_{LB}	1.0000	1.0000
	C_{LB}	3.9357	7.8557
$K_4=(\frac{M_3}{M_4}\frac{T}{C_B})/(1-\frac{T}{2R_2C_B})$	K_4C_{CB}	7.3978	7.3640
$K_4'=(\frac{M_1}{M_4}\frac{T}{C_B})/(1-\frac{T}{2R_2C_B})$	$K_4'C_{CB}$	1.2720	1.2720
$K_6=(\frac{T}{R_2C_B})/(1-\frac{T}{2R_2C_B})$	K_6C_{CB}	1.0000	1.0000
	C_{CB}	27.083	54.286
Total Capacitance (pF)		95.5	165.3

The design using the LDI transformation can also be used to realise other types of SC ladder filters besides the bandpass. It can be observed that it involves simulating the active elements in the ladder network with LDI integrators. The error in the terminations is minimised by using the approximation suggested. The termination error can be avoided altogether through the use of bilinear integrators which are either sensitive to parasitic capacitance or require a larger number of OAs. A method of design is, however, available where the ladder network is simulated by low sensitivity coupled-biquad structure.[6] From chapter 5, it has been established that parasitic insensitive, two-amplifier biquads can be realised via the bilinear transformation. This method is well-suited for bandpass realisation.

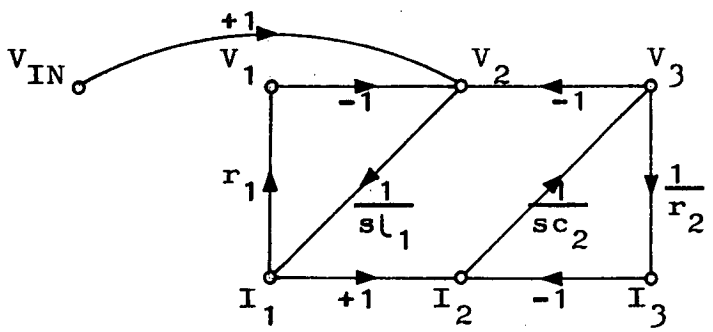
6.6 Coupled-biquad structures from lowpass prototype

This method is used when a geometrically symmetric bandpass filter function is to be realised. For this kind of filter, the specification for the lowpass prototype can be obtained as shown in chapter 4. A lowpass RLC ladder network which realises this prototype can then be obtained. A signal flow graph of this network is obtained as before, from which a diagram consisting of only first-order blocks can be derived. The first-order blocks are transformed into biquad blocks using the lowpass to bandpass transformation to achieve the coupled-biquad structures. The SC biquads can then be designed using the bilinear transformation as in chapter 5.

For the OTOB filter, the corresponding lowpass RLC ladder network shown in fig. 6:8(a) can be derived from chapter 4. From its set of loop and node equations, the signal flow graph in fig. 6:8(b) can be obtained.



(a)



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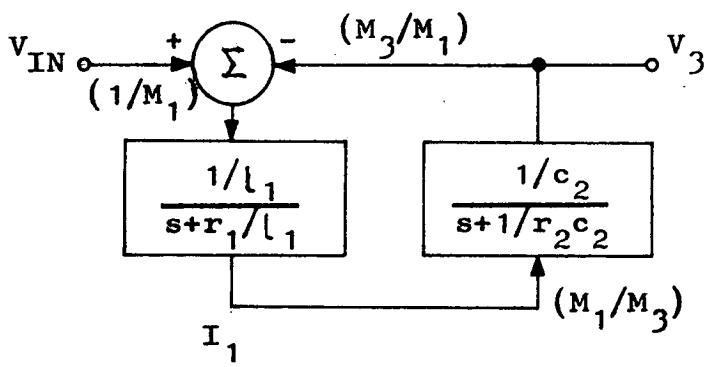
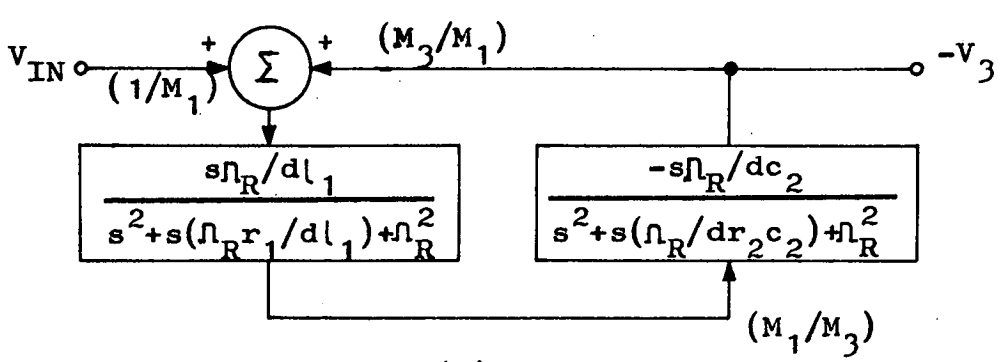


(c)



(d)

Fig. 6:8 Deriving the coupled-biquad structure. (a) RLC realisation of the lowpass prototype. (b) A signal flow graph of (a). (c) Active block diagram simulating (a) with scaling factor to maximise the dynamic range. (d) Coupled-biquad structure derived from (c).

This graph can also be represented by the structure with first-order blocks shown in fig. 6:8(c). The summing coefficients shown in brackets are for the purpose of scaling for maximum dynamic range. M_1 and M_3 are defined, as before, as the maxima of I_1 and V_3 respectively.

Applying the lowpass to bandpass transformation in (4:3) to the first order blocks, the diagram in fig. 6:8(c) is transformed into the coupled-biquad structure in fig. 6:8(d). The second biquad block of the figure is inverted so that both $V_{IN}$and $-V_3$ are summed into the first block. This is also achieved if the first biquad block is inverted but the resulting SC circuit has higher total capacitance and larger capacitor spread. The values of r_1, r_2, ι_1, c_2 d and Ω_R can be obtained from chapter 4 for the bilinearly-prewarped specification, with fc = 16fm. The values of M_1 and M_3 are given by

$$M_1 = 0.636010 \ , \quad M_3 = 0.500000 \qquad (6:10)$$

The denominators of both biquad blocks are the same in this case and are given by

$$\Delta = s^2 + 0.911215\ s + 40.5229 \qquad (6:11)$$

Including the scaling factors in (6:10), the transfer functions involved can be derived as,

$$\frac{I_1}{V_{IN}} = 1.43271 \ \ s/\Delta \qquad (6:12a)$$

$$\frac{I_1}{-V_3} = 0.716353\ s/\Delta \qquad (6:12b)$$

$$\frac{-V_3}{I_1} = -\ 1.15908\ \ s/\Delta \qquad (6:12c)$$

The non-inverting and inverting transfer functions can be designed with the $H_1(z)$ and $H_2(z)$ design in Table 5:2 respectively, using the circuit of fig. 5:5 to realise the SC biquads through the bilinear transformation. The complete circuit for the SC implementation of the coupled-biquad structure is given in fig. 6:9. The final capacitor values are shown in Table 6:3. The capacitor values have been scaled to maximise the dynamic range within the biquad and adjusted so that the minimum capacitance is unity. Table 6:3 also gives the capacitor values obtained when fc = 48 fm is used.

Table 6:3 Capacitor values for the circuit in fig. 6:9 with fc = 16 fm and 48 fm.

Capacitors (pF)	fc = 16fm	fc = 48fm
C_{11}	27.745	44.275
E'_1C_{11}	3.9381	6.2066
E_1C_{11}	10.946	5.7709
A_1C_{11}	1.0000	1.0000
$A_{IN}C_{11}$	2.0000	2.0000
C_{21}	9.4113	9.0920
R_1C_{21}	3.5355	1.1827
K_1C_{21}	1.0000	1.0000
$K_{IN}C_{21}$	2.0000	2.0000
C_{12}	7.1399	7.6633
E'_2C_{12}	1.0000	1.0755
E_2C_{12}	2.7795	1.0000
A_2C_{12}	1.2619	1.3680
C_{22}	29.486	86.222
R_2C_{22}	11.226	11.203
K_2C_{22}	1.0000	1.0000
Total	115.5	182.0

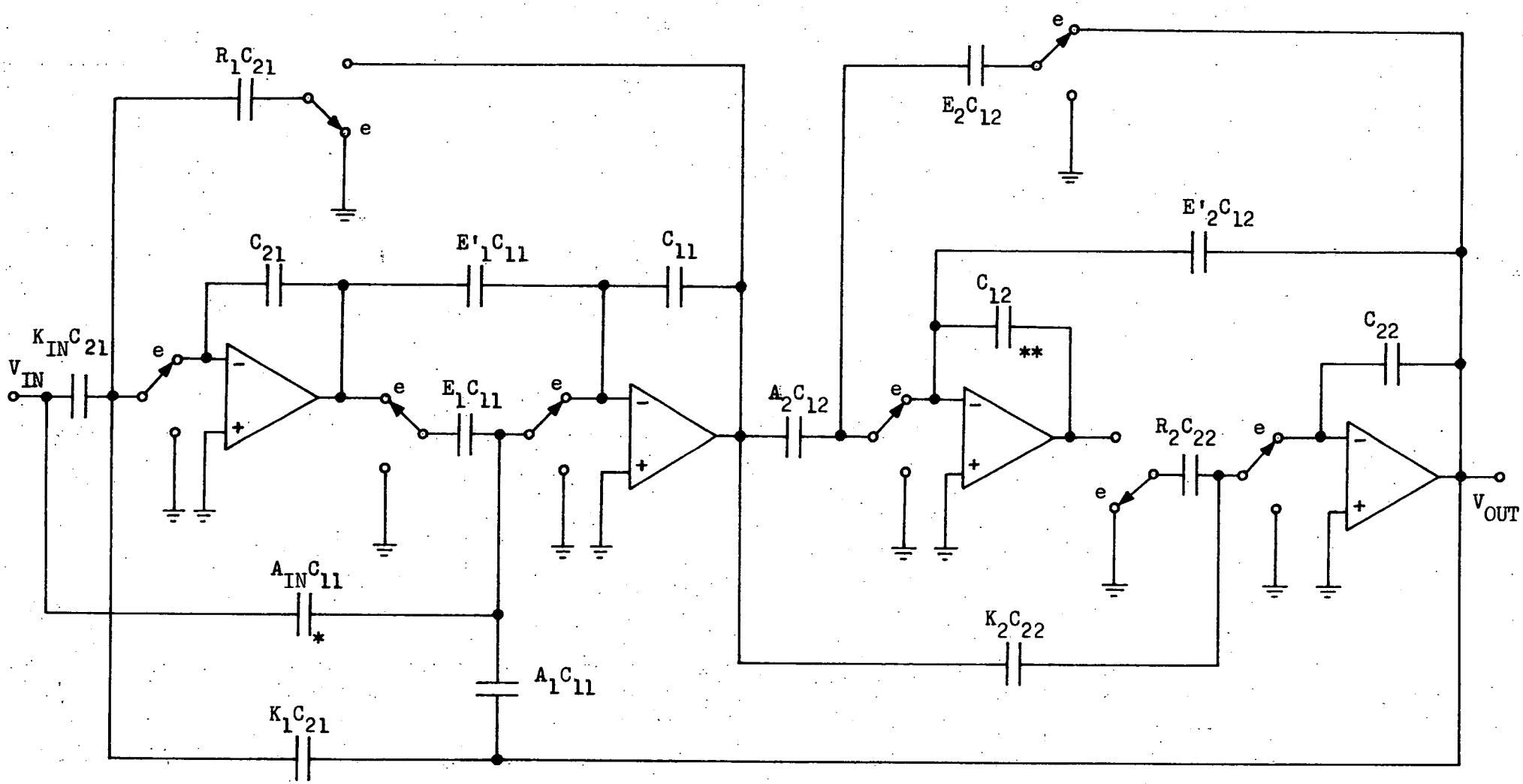


Fig. 6:9 A switched-capacitor implementation of the coupled-biquad structure in fig. 6:8(d).

This design requires more total capacitance than those obtained using the cascade realisation and the SC ladder filter realised using the LDI transformation. However the circuit in fig. 6:9 has good sensitivity and dynamic range properties, is insensitive to parasitic capacitance and can be designed without any approximation to the termination resistances.

6.7 Coupled biquad structures from bandpass prototype

A different procedure is required to achieve the coupled-biquad structure for the general parameter bandpass filter which is not derived from a lowpass prototype. A suitable LC ladder network meeting the prewarped specification has to be obtained using LC synthesis programmes. Then the coupled-biquad realisation is derived using the method to be illustrated below.[6] For simplicity, this illustration uses the bandpass RLC ladder network which satisfies the bilinearly prewarped specification for the OTOB filter as derived in chapter 4. The ladder network is given in fig. 6:10(a).

From this ladder network, equations can be written to express the voltage at each node in terms of voltages at the preceeding and succeeding nodes, i.e.

$$V_X = T_{INX}\, V_{IN} + T_{4X} V_4 \qquad (6:13a)$$

$$V_4 = T_{X4} V_X \qquad (6:13b)$$

where

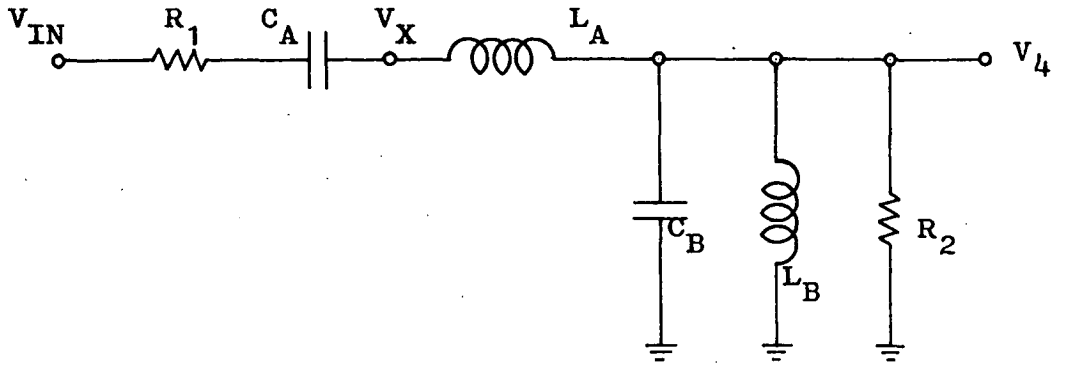
$$T_{INX} = \left.\frac{V_X}{V_{IN}}\right|_{V_4 = 0} = \frac{S^2}{S^2 + \frac{R_1}{L_A} S + \frac{1}{L_A C_A}} \qquad (6:14a)$$

$$T_{4X} = \left.\frac{V_X}{V_4}\right|_{V_{IN}=0} = \frac{\frac{R_1}{L_A}s + \frac{1}{L_A C_A}}{s^2 + \frac{R_1}{L_A}s + \frac{1}{L_A C_A}} \qquad (6:14b)$$

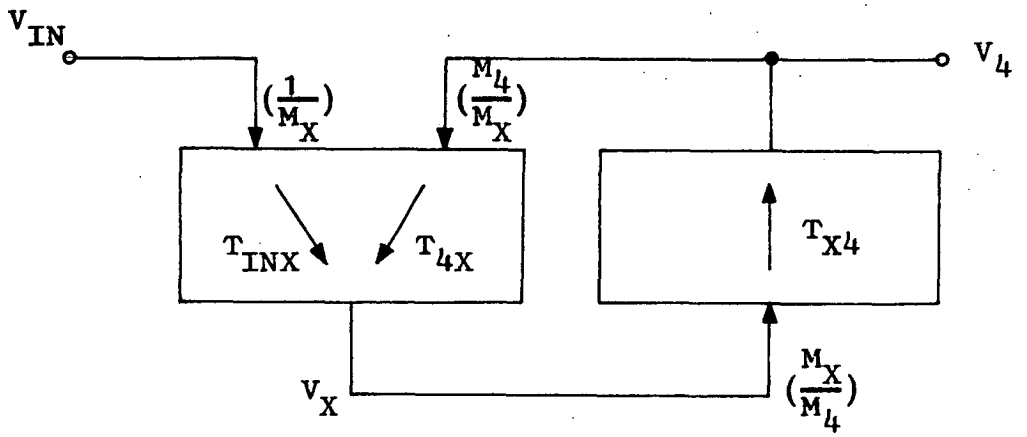
$$T_{X4} = \frac{V_4}{V_X} = \frac{\frac{1}{L_A C_B}}{s^2 + \frac{1}{R_2 C_B}s + \frac{L_A + L_B}{L_A L_B C_B}} \qquad (6:14c)$$

Note that one pair of the transfer functions have the same poles, and can be realised by one biquad. The ladder network can thus be simulated by the active blocks as shown in fig. 6:10(b). The scaling factors for maximum dynamic range are also included in the figure. Actually, the coupled-biquad structure obtained does not fully simulate the ladder operation, but it simulates the interaction of the nodal voltages. However, the sensitivity behaviour of the structure is still good.[6]

This coupled-biquad realisation can be implemented by SC circuits which have been used in chapter 5. The two biquads required for T_{INX}, T_{4X} and T_{X4} can be realised by the SC biquads used in fig. 5:6. This implementation, however, results in very high total capacitance requirement. For fc = 16fm, the total capacitance required is 358pF.



(a)



(b)

Fig. 6:10 (a) RLC ladder meeting the bilinearly-prewarped specification for the OTOB filter. (b) Active blocks simulating the nodal voltages of (a).

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CHAPTER SEVEN

FURTHER APPROACHES FOR SWITCHED-CAPACITOR LADDER REALISATIONS

The low sensitivity property of the doubly terminated ladder network makes it an attractive starting point for the realisation of SCFs. Chapter 6 shows that SC ladder filters simulating the ladder operation can be realised via the LDI transformation. One drawback of this method is that the simulation of the terminating resistances has to be approximated. Chapter 6 also gives another approach where the coupled-biquad structure is used. The structure, however, only simulates the interaction of the nodal voltages of the ladder network. Nevertheless its sensitivity is still good.

This chapter deals with a number of other approaches towards realising the ladder network in SC forms. Each approach is dealt very briefly and realisation of the SC OTOB through these approaches are given.

7.1 Using voltage-controlled current sources

This method involves replacing the series branches of the passive ladder network by voltage-controlled current sources (VCCS) and the shunt branches by current-controlled voltage sources (CCVS).[1] The method is illustrated here for the SC realisation of the first order RC filter shown in fig. 7:1(a). The resistor R is replaced by the VCCS as shown in fig. 7:1(b) without changing the voltage across and the current through capacitor, C.

The node with V_2 is then transformed into virtual ground and $-V_2$ is instead generated as the amplifier output voltage as given in fig. 7:1(c). The voltage across and current through C remain unchanged. Replacing the

grounded capacitor C by the CCVS and creating the virtual ground facilitates the realisation of parasitic insensitive grounded VCCS. If there are two nodes, such as for V_2, connected together by an impedance the sign of the generated voltages at the OA outputs should be opposite.

The relationship for the VCCS in fig. 7:1 is given by

$$I(s) = (V_1 - V_2)/R \qquad (7:1)$$

and the charge-voltage relationship is thus

$$Q(s) = (V_1 - V_2)/sR \qquad (7:2)$$

Using the bilinear transformation in (3:28), the equivalent relationship in the SC realisation is

$$Q(z) = \frac{T}{2R}\frac{1 + z^{-1}}{1 - z^{-1}}(V_1 - V_2) \qquad (7:3)$$

In terms of charge variation $\Delta Q(z)$ for full-cycle sampled-and-held voltages, the relationship is

$$\Delta Q(z) = (1 - z^{-1})Q(z) = \frac{T}{2R}(1 + z^{-1})(V_1 - V_2) \qquad (7:4)$$

This relationship can be realised by the circuit in fig. 7:2. Thus the RC circuit in fig. 7:1 is realised in SC form by the circuit in fig. 7:3. The negative capacitor across the OA can be incorporated with the feedback capacitor, C. This circuit is equivalent to the bilinear integrator shown in fig. 3:16(a).

If the series branch is a capacitor, C_1 then using the same procedure as (7:1) to (7:4), the charge-voltage relationship becomes

$$\Delta Q(z) = C_1(1 - z^{-1})(V_1 - V_2) \qquad (7:5)$$

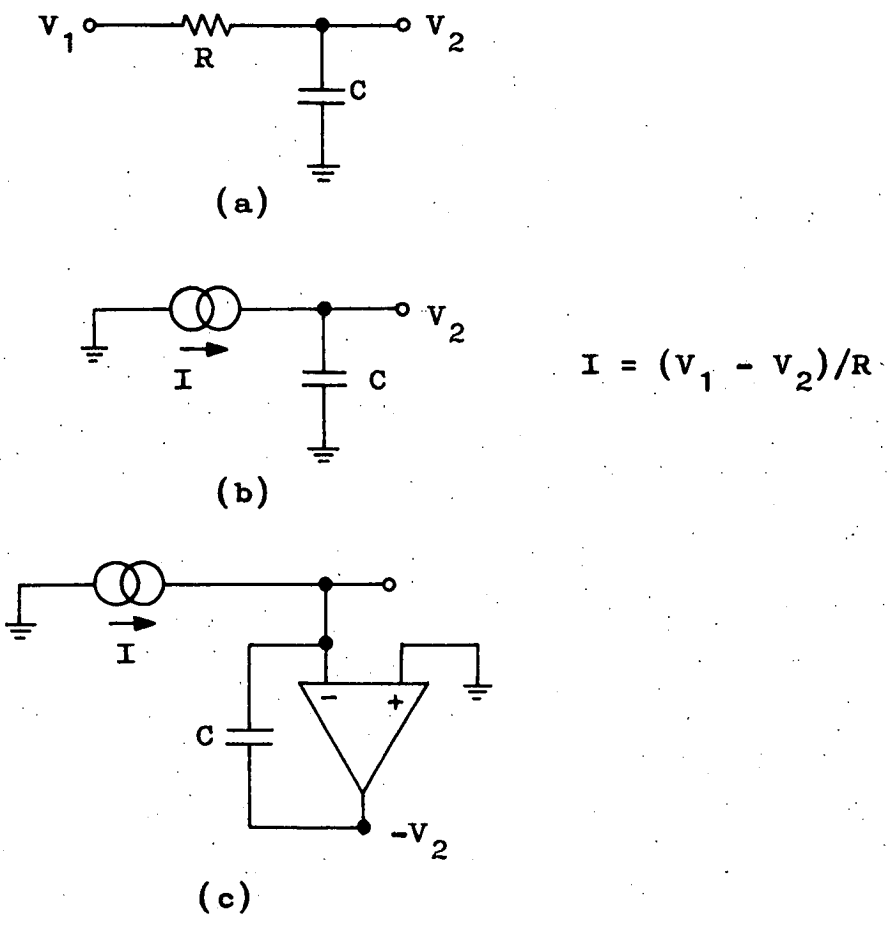


Fig. 7:1 Transformation of the RC circuit for switched-capacitor realisation using voltage-controlled current source.

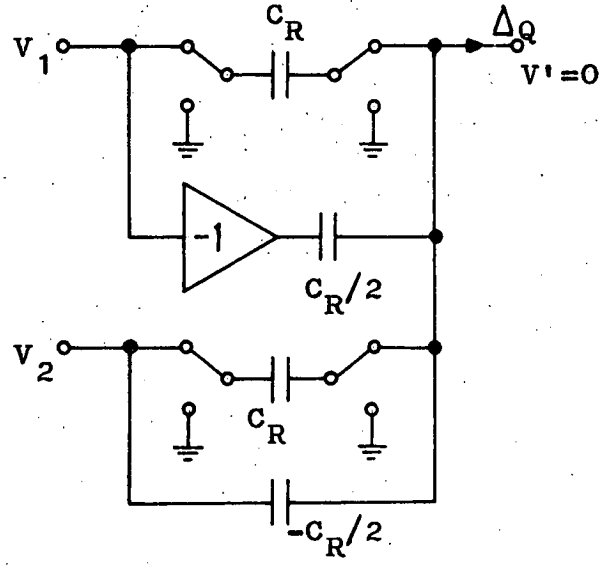


Fig. 7:2 A circuit for the resistive current source, I. $C_R = T/R$

This relationship is simply realised by the circuit in fig. 7:4. For an inductance, L the charge-voltage relationship is

$$\Delta Q(z) = \frac{T^2}{4L} \frac{(1 + z^{-1})^2}{1 - z^{-1}} (V_1 - V_2) \qquad (7:6)$$

The current source for an inductance in the series branch can be realised by the circuit in fig. 7:5 which has the relationship

$$\Delta Q(z) = \frac{C_a C_c}{C_b} \frac{z^{-1}}{1 - z^{-1}} (V_1 - V_2) \qquad (7:7)$$

The expression in z^{-1} can be expressed as

$$\frac{z^{-1}}{1 - z^{-1}} = \frac{1}{4}\left[\frac{(1 + z^{-1})^2}{1 - z^{-1}} - (1 - z^{-1}) \right] \qquad (7:8)$$

Thus the circuit of fig. 7:5 represents a current source of an inductor in parallel with a negative capacitor in the bilinear-transformed domain.[2] For realisation of an inductor, the negative capacitor can be compensated by connecting capacitors as in fig. 7:4, where $C_1 = \frac{C_a C_c}{4C_b}$, across the terminals.

Any ladder network can thus be transformed into an SCF by appropriately replacing the branch elements of the ladder with circuits described above. However, a problem arises in certain realisations such as for the source termination in the case of a highpass ladder network. The overall transfer function of the filter can be written as

$$\frac{V_{OUT}}{V_{IN}} = \frac{V_{OUT}}{\Delta Q_R} \cdot \frac{\Delta Q_R}{V_{IN}} \qquad (7:9)$$

where $\frac{\Delta Q_R}{V_{IN}}$ is the relationship for the source termination given by equation such as in (7:4).

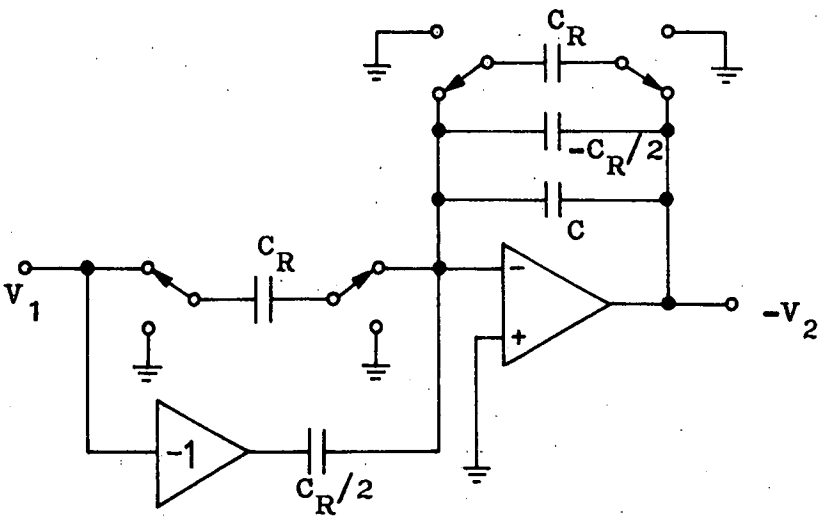


Fig. 7:3 A switched-capacitor realisation of the RC circuit in fig. 7:1.

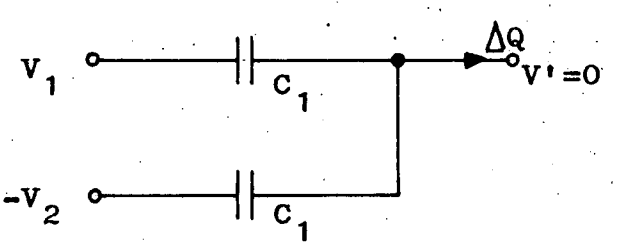


Fig. 7:4 A capacitance current source.

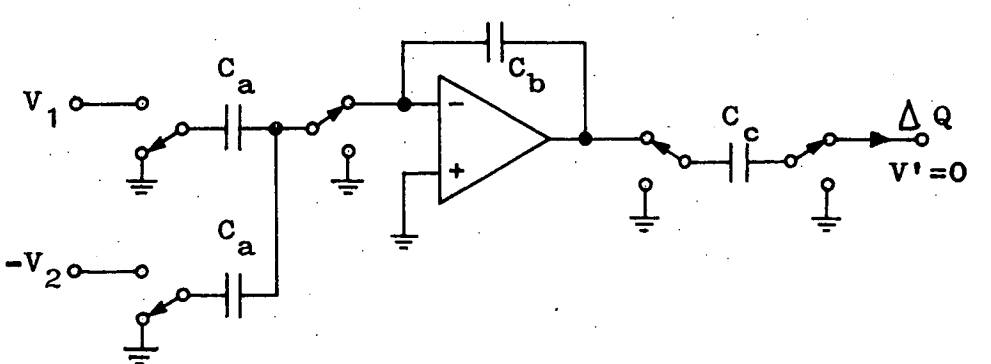


Fig. 7:5 An inductance current source.

For a highpass filter, the passband includes the frequency f = fc/2, i.e. $z^{-1} = -1$, thus $\frac{\Delta Q_R}{V_{IN}} = 0$. This requires $\left|\frac{V_{OUT}}{\Delta Q_R}\right| \to \infty$ which results in instability in the overall highpass circuit.[1] This problem can be overcome by scaling the impedance of the highpass ladder network such as transforming the terminating resistance into a capacitor. In this case, the inductors in the circuit are transformed into resistors and the capacitors into frequency-dependent negative resistors (FDNR).

7.2 Switched-Capacitor OTOB realisation using VCCS

The ladder network which satisfies the specification for the OTOB filter prewarped according to (3:29), is redrawn in fig. 7:6(a). For this ladder, only one grounded capacitor is present and it is not possible to realise all the series branches using circuits given in section 7.1. One suggestion to overcome this is by introducing grounded capacitors C_x and C_y from nodes x and y respectively where $C_x = C_y = 0$.[3] However, for this example, the series branch consisting of R_1, C_A and L_A can be replaced by an equivalent VCCS involving a biquad circuit.

Using steps as in section 7.1, the ladder network can be replaced by the circuit of fig. 7:6(b), where

$$I_1(s) = \frac{s/L_A}{s^2 + sR_1/L_A + 1/L_AC_A}(V_{IN} - V_{OUT}) \qquad (7:10)$$

Using bilinear transformation, the charge-voltage relationship becomes

$$\Delta Q_1(z) = \frac{\frac{T^2}{4L_A}(1 - z^{-2})(1 + z^{-1})(V_{IN} - V_{OUT})}{(1 + \frac{TR_1}{2L_A} + \frac{T^2}{4L_AC_A}) + 2(\frac{T^2}{4L_AC_A} - 1)z^{-1} + (1 - \frac{TR_1}{2L_A} + \frac{T^2}{4L_AC_A})z^{-2}} \qquad (7:11)$$

$$= \frac{T}{2}(1 + z^{-1})H(z)(V_{IN} - V_{OUT})$$

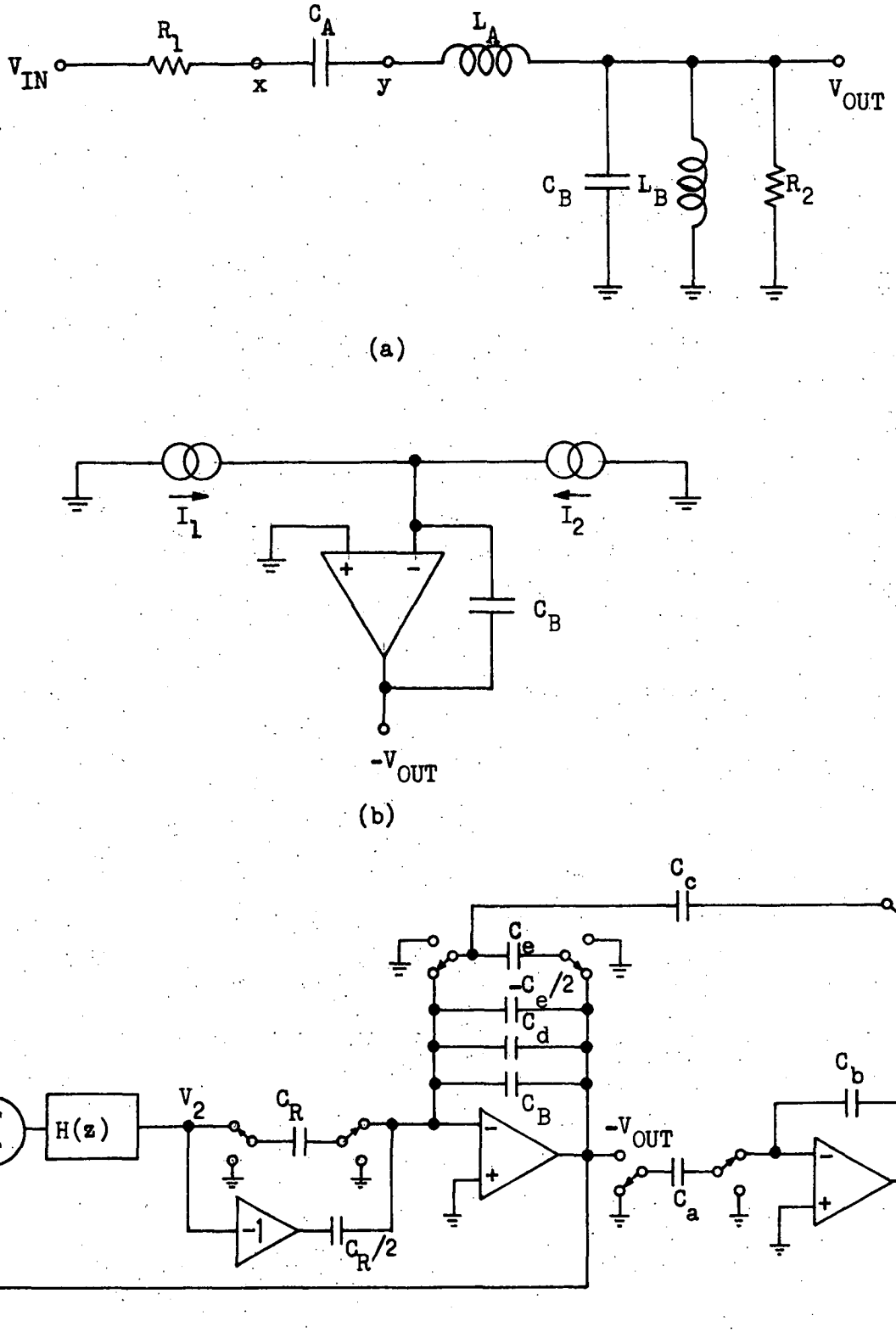


Fig. 7:6 (a) Ladder network for the OTOB filter. (b) Replacing series branches by v.c.c.s. and shunt branch by c.c.v.s. (c) Switched-capacitor realisation. H(z) is a biquad circuit as in fig 5:5.

where H(z) is the transfer function of an SC bandpass circuit realised through the bilinear transformation as discussed in chapter 5. The $\frac{T}{2}(1 + z^{-1})$ factor can be realised by the circuit of fig. 7:2 with C_R=T.

The current source I_2 is given by

$$I_2(s) = (\frac{1}{sL_B} + \frac{1}{R_2})(-V_{OUT}) \qquad (7:12)$$

This can be realised by the VCCS discussed in section 7.1. The inductance current source is realised by the circuit in fig. 7:5 with $\frac{C_a C_c}{C_b} = \frac{T^2}{L_B}$ and using a compensating capacitor, $C_d = \frac{T^2}{4L_B}$. Thus the circuit of fig. 7:6(b) can be realised in SC form by the circuit as shown in fig. 7:6(c), where $C_e = T/R_2$.

The SC circuit of fig. 7:6(c) requires 5 OAs when the two-OA biquad is used for H(z). The OA for the inverter can be avoided if the circuit such as in fig. 7:7 is used for the $\frac{T}{2}(1 + z^{-1})$ factor. This circuit however, is sensitive to top plate parasitic capacitance. Another method to reduce the number of OAs is to make the adjustments as shown in fig. 7:8. It can be observed that these adjustments resulted in a structure similar to the coupled-biquad as described in chapter 6. In fact, the method discussed in section 7.1 involves simulation of the node voltages of the passive ladder network which is also the case in the coupled-biquad realisation. The difference in the approaches towards the SC realisation is only in the way to realise the VCCS.[4]

7.3 Using scaled VCCS

In section 7.1 it was shown that R, L and C branch elements of the ladder network have VCCS equivalents given by the bilinear-transformed charge-voltage relationship. These are

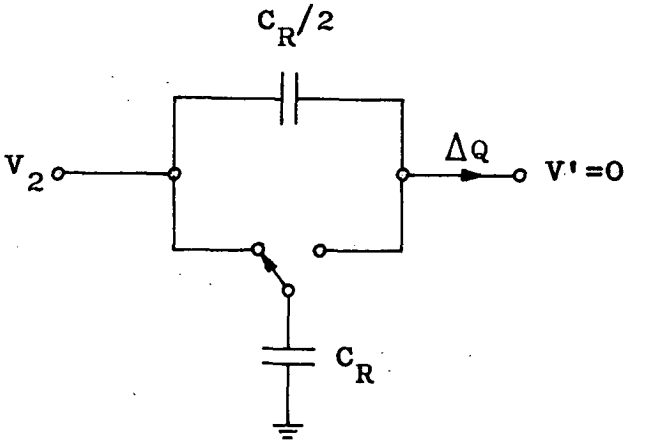


Fig. 7:7 An alternative resistive current source

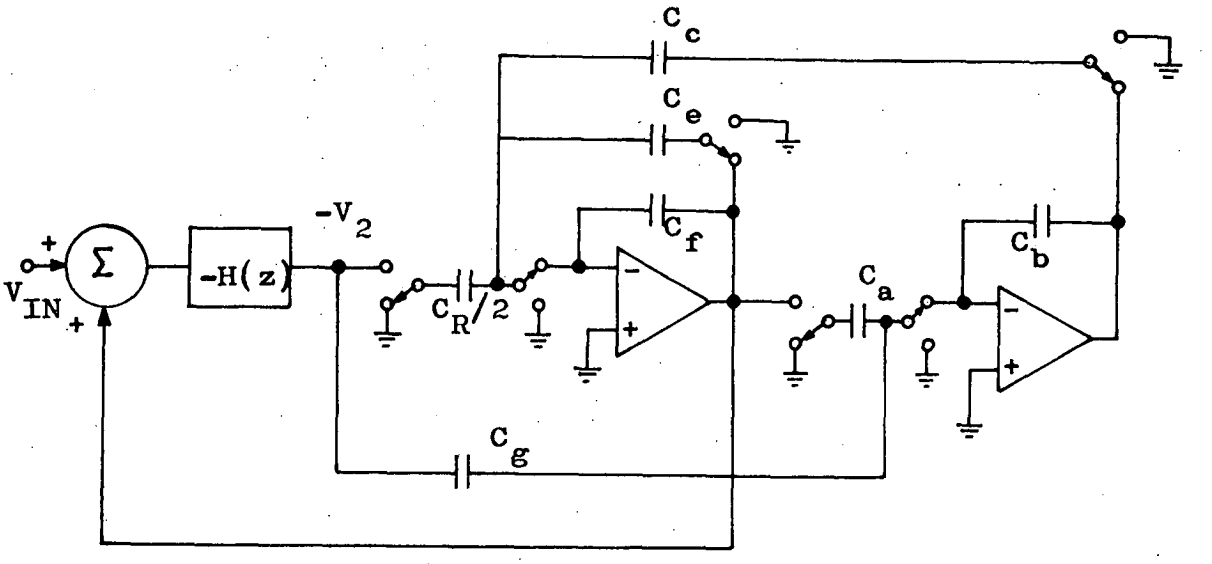


Fig. 7:8 A switched-capacitor realisation of the ladder in fig. 7:6 using four OAs. $C_f = C_B + C_d - C_e/2$, $C_g = C_R C_b / 2C_c$.

$$\frac{\Delta Q}{V} = \begin{cases} C_R(1 + z^{-1}) & (7:13a) \\ C_L \dfrac{(1 + z^{-1})^2}{1 - z^{-1}} & (7:13b) \\ C(1 - z^{-1}) & (7:13c) \end{cases}$$

where $C_R = T/2R$, $C_L = T^2/4L$ for the R, L and C branch elements respectively, which are realisable by parasitic insensitive SC circuits. However, for an inductor, the relationship is recursive and thus requires an OA for its realisation. This OA can be avoided by multiplying the charges in (7:13) with the frequency-dependent factor $(1 - z^{-1})$.[1] Equations in (7:13) become

$$\frac{\Delta Q}{V} = \begin{cases} C_R(1 - z^{-2}) & (7:14a) \\ C_L(1 + z^{-1})^2 & (7:14b) \\ C(1 - z^{-1})^2 & (7:14c) \end{cases}$$

Thus another way to realise the VCCS involving only passive elements, i.e. capacitors and switches, is possible which results in reduced number of OAs required in the overall filter circuit. The OAs are only needed in the shunt branches to create virtual grounds at the appropriate nodes of the ladder network as in the method of section 7.1. The relationships in (7:14) can be realised by the SC circuits such as given in fig. 7:9. There are other possible realisations which include SC circuits for parallel combinations of R, L and C elements.[1]

These circuits, however, are sensitive to top-plate parasitic capacitance and require a more involved clocking scheme. Using the same argument as in (7:9) for the relationships in (7:14), the passband of the overall filter cannot include f = 0 and f = fc/2, i.e. z = 1 and z = -1 respecitvely. Thus the method is best suited only for bandpass realisation.

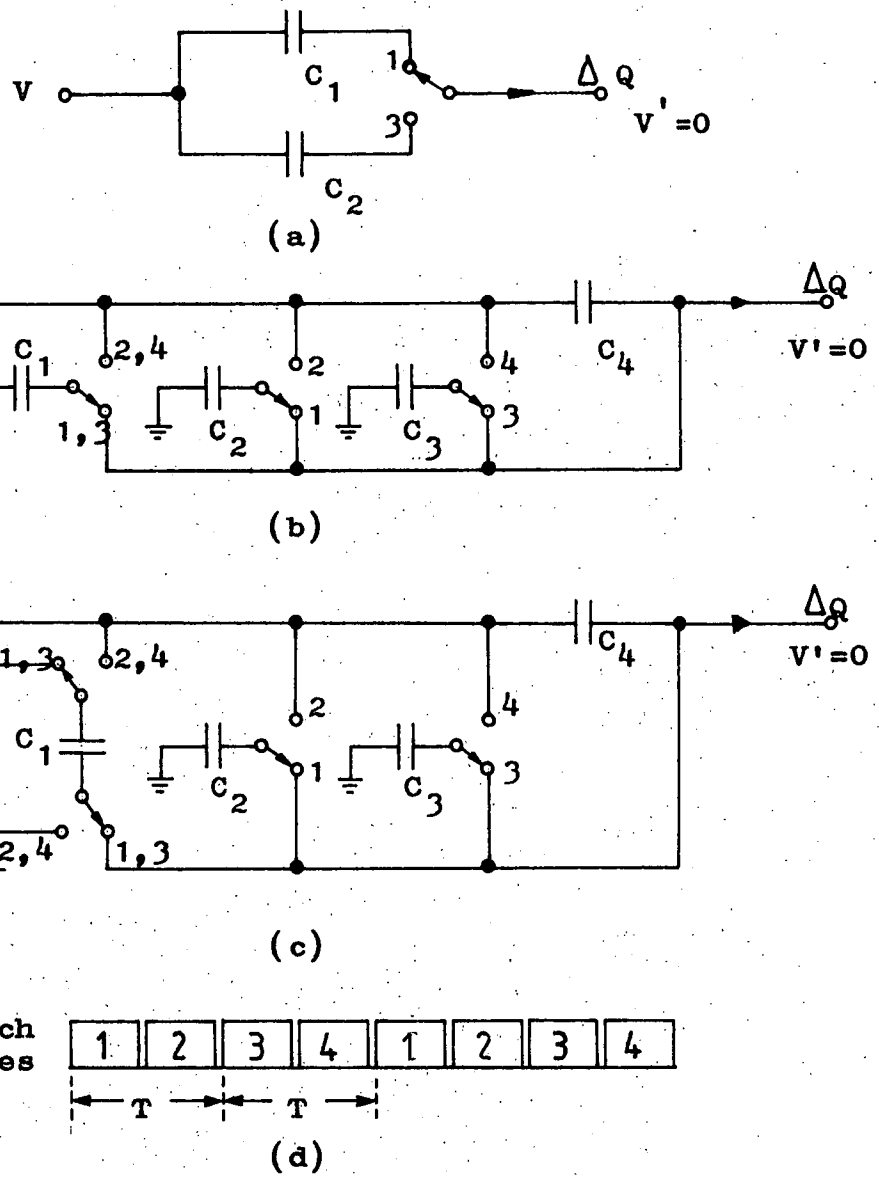


Fig. 7:9 Passive branches for (a) a resistor, $C_1=C_2=C_R$; (b) an inductor, $C_1/3=C_2=C_3=C_4=C_L$ and (c) a capacitor, $C_1=C_2=C_3=C_4=C$. (d) The clocking scheme.

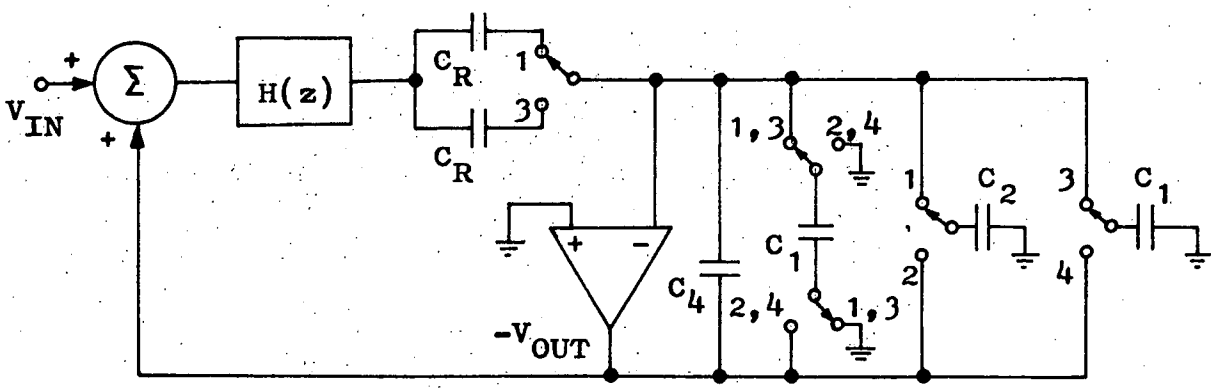


Fig. 7:10 A switched-capacitor realisation of the ladder in fig. 7:6(a) using scaled RLC equivalents.

For the ladder network example such as in fig. 7:6(a), the series R_1, L_A, C_A combination does not have a passive realisation. Using the same procedure as in section 7.2, eqn (7:11) is multiplied by $(1 - z^{-1})$ then the charge-voltage relationship for the series combination becomes

$$\Delta Q = \frac{T}{2}(1 - z^{-2})H(z)(V_{IN} - V_{OUT}) \qquad (7:15)$$

This is realisable by the same biquad circuit as before, in cascade with a resistor equivalent.

$I_2(s)$ in (7:12) is due to the inductor L_B in parallel with resistor, R_2. Together with capacitor C_B, they form the parallel RLC combination. Instead of realising these elements individually, the combination can just be realised by the circuit of fig. 7:9(c) with $C_1 = C - 3C_L - C_R$, $C_2 = C_3 = C + C_L - 3C_R$ and $C_4 = C + C_L + C_R$. Thus the ladder network is realisable in SC form using the scaled RLC equivalents as shown in fig. 7:10. The clocking scheme is as shown in fig. 7:9(d). The switched capacitors in the biquad H(z) are switched as for capacitor C_1.

The overall circuit requires at most three OAs. The four-phase clock does not increase the OA settling time requirement since there are still two clock phases per period. The slew rate requirement may increase with more capacitors to be charged and discharged.

7.4 Using Impedance Simulation Method

This method involves one-to-one replacement of each element in filter ladder network by its SC equivalents. Thus the topology of the ladder is retained in the SCF and the Kirchoff law relations for the voltages and charges are the same. Equations in (7:13) give the charge-voltage

relationships of the R, L and C branches obtained through the bilinear transformation. In the SC realisations of these equations, the virtual ground as for the circuits in section 7.1 is no longer available.

The capacitive branch of the ladder network, however is unchanged in the SCF. The resistive branch is simulated by the circuit of fig. 7:11.[5] A number of SC circuits have been suggested for the inductive branch. A circuit is given in fig. 7:12(a) which has reduced capacitance spread and reduced output swing of the OA.[6] The clocking scheme for the circuit is shown in fig. 7:12(b). The four-phases per sampling period may increase the settling time requirement for the OA compared to realisations of earlier sections.

In the circuit of fig. 7:12, when switches 1 are closed, the charge on C_0 becomes $C_0 z^{-1} V_L(z)$, as an example, and C_2 obtains charge from C_1 equal to $\frac{C_1 C_0 z^{-2}}{C_0 + C_1} V_L(z)$. The charge on C_1 was as a result of charge sharing with C_0 during clock phase 2 of the previous sampling period. Thus when switches 2 are closed again, C_0 has charge $\frac{C_0}{C_0 + C_1} z^{-1} V_L(z)$ which is lost to C_2 during 3. Then the voltage at the output of the OA becomes

$$V_0(z) = - \frac{C_0/C_2}{C_0 + C_1} \frac{C_0 z^{-1} + C_1 z^{-2}}{1 - z^{-1}} V_L(z) \qquad (7:16)$$

During clock phase 4, this voltage is connected across C_0. Thus when C_0 is connected again to $V_L(z)$ during 1 of the new sampling period, the charge variation is

$$\begin{aligned} \Delta Q(z) &= C_0 V_L(z) - C_0 V_0(z) \\ &= C_0 \left[\frac{1 + \left(\frac{C_0^2}{C_2(C_0 + C_1)} - 1 \right) z^{-1} + \frac{C_0 C_1}{C_2(C_0 + C_1)} z^{-2}}{1 - z^{-1}} \right] V_L(z) \end{aligned} \qquad (7:17)$$

Comparing (7:17) with the charge-voltage relationship for an inductor in (7:13), the capacitor values are determined to be

$$C_0 = 3C_1 = 4C_2 = C_L = \frac{T^2}{4L} \qquad (7:18)$$

The circuit of fig. 7:12 can also be used to realise a parallel LC circuit if $3C_L > C$ and the capacitors in the circuit are given by

$$C_0 = C_L + C,\ C_1 = \frac{C_0^2}{3C_L - C},\ C_2 = \frac{C_0^2}{4C_L} \qquad (7:19)$$

If $C \geq 3C_L$ then a better circuit, in terms of capacitor spread and OA output swing is available and is shown in fig. 7:13. Its clocking scheme is the same as in fig. 7:9(d) which means a faster OA is not required. It is also advantageous with respect to the effects of element tolerance and finite gain-bandwidth of the OA though it is more sensitive to stray capacitance.[6] The capacitor values are given by

$$C_0 = 4C_L,\ C_1 = C - 3C_L \qquad (7:20)$$

Using the above branch equivalents, the SC realisation of the ladder network of fig. 7:6(a) is shown in fig. 7:14(a). One possible clocking scheme for the circuit is given in fig. 7:14(b). Since the topology of the ladder network is retained, the sensitivity of this SCF to element variation is very close to that of the ladder network. The slightly unfavourable effects are in the element variation inside the active circuit simulating the inductor. The number of OAs required for this SCF is equivalent to the number of inductors in the ladder network.

The direct simulation, however, results in the overall filter having a basic loss of 6dB which has to be corrected to satisfy the OTOB specification. Also, this realisation is very susceptible to stray

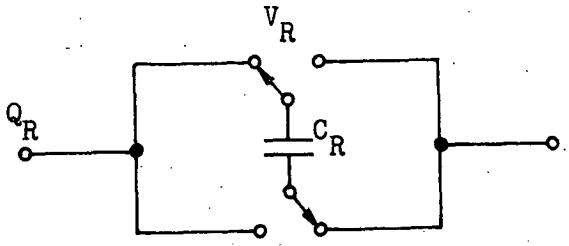
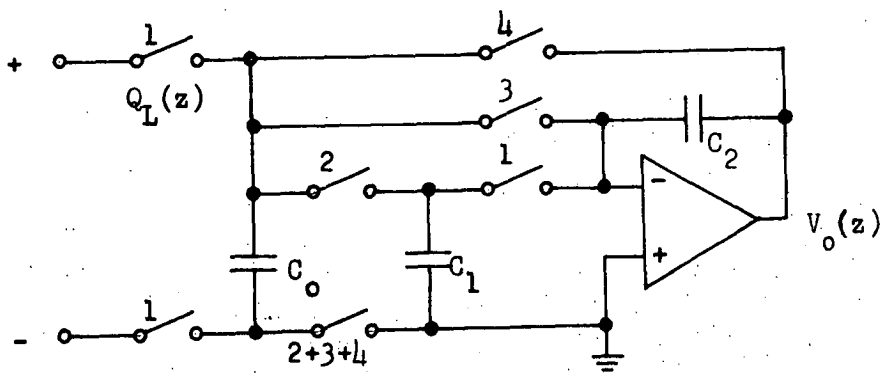


Fig 7:11 Bilinear switched-capacitor "resistor".



(a)

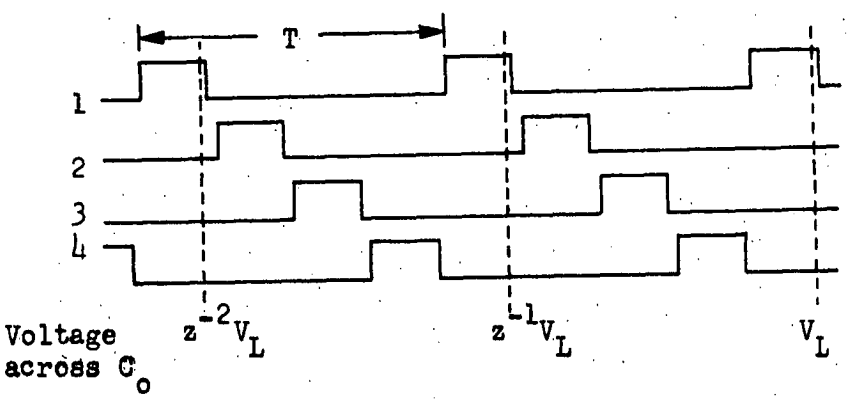


Fig. 7:12(a) A switched-capacitor circuit simulating an inductor.
(b) Its clocking scheme.

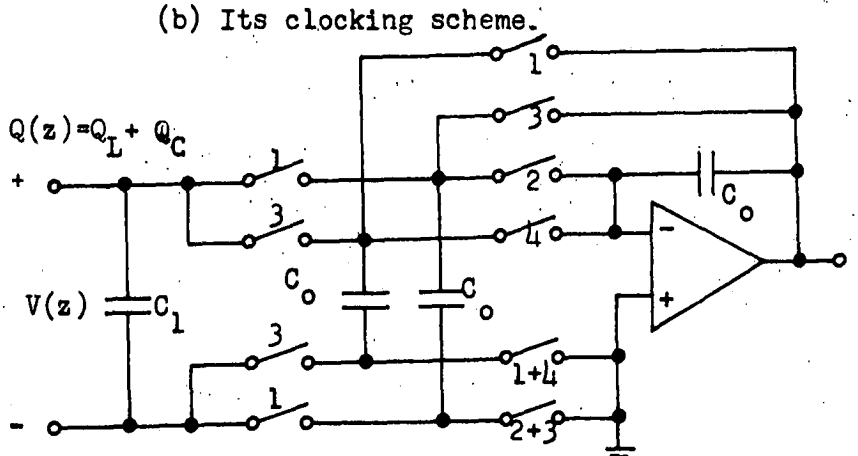


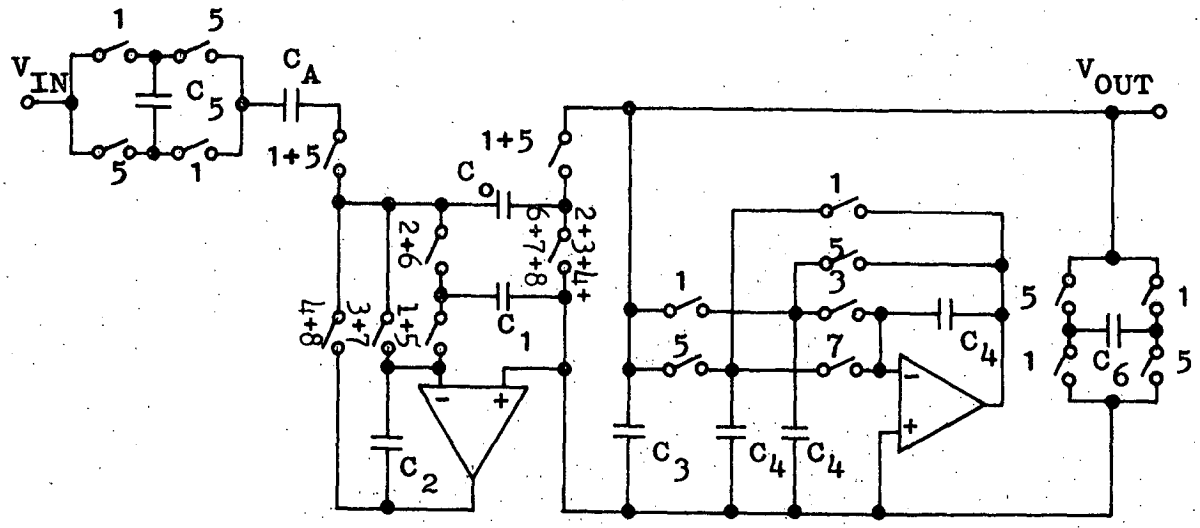
Fig. 7:13 A switched-capacitor circuit simulating a parallel LC.

capacitances especially when floating inductance is required. Floating inductance may be avoided by scaling the ladder network into a circuit containing FDNR but SCF derived from this is more sensitive to stray capacitance.[5]

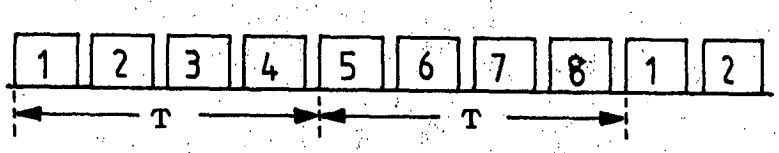
Another method is to use the "reactive-active" scheme to obtain a starting ladder network which contains only grounded inductors.[7] The SCF will then have reduced sensitivity to stray capacitance. However, negative capacitance may be present in the ladder network which has to be realised using additional OA and the sensitivity of the filter to element variation is increased due to this.

An inductor can also be simulated by SC circuit through the LDI transformation which needs only a two-phase clock. Under this transformation, a capacitor remains unchanged. The resistor, however, has to be approximated. Thus the overall SCF realisation is not exact. Also, the realisation is sensitive to top-plate parasitic capacitance.[8]

The simulation of a resistor by a series switched-capacitor has been discussed as shown in fig. 1:3. In chapter 3, it is shown that this simulation is equivalent to implementing the backward difference transformation. A capacitor is also unchanged under this transformation and grounded and floating inductors can be simulated by simple switched-capacitor circuits needing only a two-phase clock.[9][10] The SCF realisation, however, is sensitive to stray capacitance. It also requires that the clock frequency be much greater than the frequencies of interest or that prewarping be done.[11]



(a)



(b)

Fig. 7:14 (a) A switched-capacitor realisation of the ladder in fig. 7:6(a) using impedance simulation method based on the bilinear transformation. (b) Its clocking scheme.

7.5 Using Voltage Inverter Switches

Another approach for simulating the branches of the ladder network is by equating the voltage V(s) and current I(s) of the analogue ladder circuit as follows,

$$V(s) = \frac{V_a(z) + V_b(z)}{2} \qquad (7:21a)$$

$$I(s) = \Delta Q(z)/T \qquad (7.21b)$$

where $V_a(z)$ and $V_b(z)$ are z-transforms of voltages across the discrete circuit after and before a current pulse arrival, respectively. For a capacitor in the discrete circuit,

$$I(s) = C(V_a(z) - V_b(z))/T \qquad (7:22a)$$

$$V_b(z) = z^{-1}V_a(z) \qquad (7:22b)$$

Thus, from (7:21a) and (7:22),

$$\frac{V(s)}{I(s)} = \frac{T}{2C}\,\frac{1 + z^{-1}}{1 - z^{-1}} = \frac{R}{s} \qquad (7:23)$$

taking the step resistance definition of resonant transfer circuits, [12]

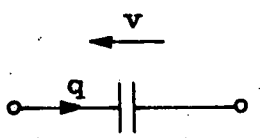
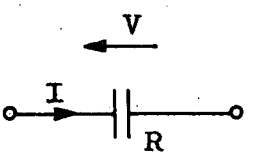
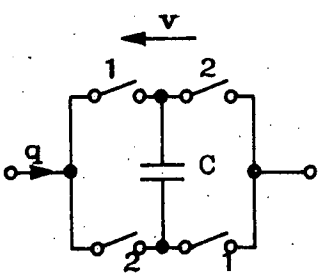
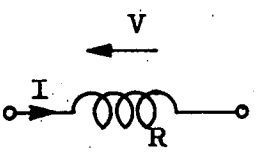
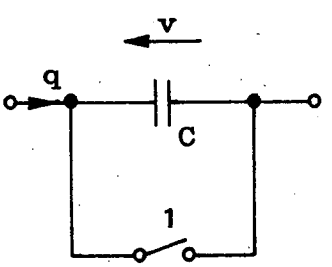
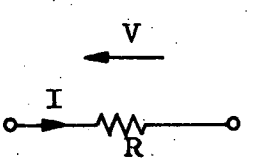
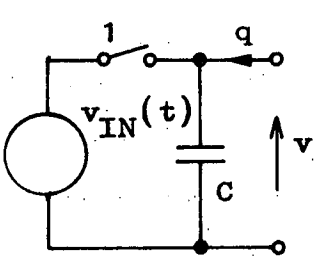
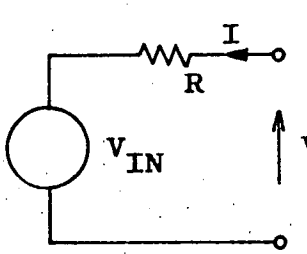
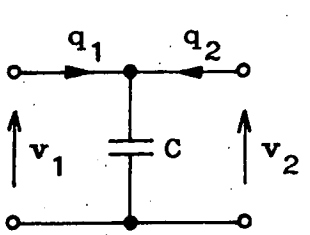
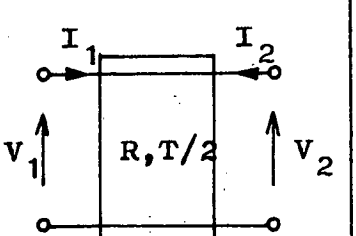
$$R = T/2C \qquad (7:24)$$

and using a normalised version of the bilinear transformation in (3:28), i.e.

$$s = \frac{1 - z^{-1}}{1 + z^{-1}} \qquad (7:25)$$

Eqn (7:23) shows that a capacitor in the analogue circuit is also realised by a capacitor in the SC circuit. The SC realisations of other elements of the ladder network are given in Table 7:1.[13] All the realisations use only capacitors and switches.

Table 7:1 Switched-capacitor realisations of capacitance, inductance, resistive sources and grounded unit element using equivalences in eqn. (7:21).

SC realisation	Network element in s-domain	equation in s-domain
		$V = \frac{R}{s}.I$
		$V = sRI$
		$V = IR$
		$V = V_{IN} + IR$
		$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \frac{1}{\sqrt{1-s^2}} \begin{bmatrix} 1 & sR \\ \frac{s}{R} & 1 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$

When these SC elements are interconnected, Kirchoff Laws have to be fulfilled. The current law is automatically satisfied. The voltage law is only satisfied if each critical loop, containing at least one switched capacitor is closed via a voltage inverter switch (VIS). Including the VIS in the loop, the voltage across the VIS, $V_v(s)$ must be zero. Therefore from (7:21a)

$$V_{va}(z) = - V_{vb}(z)$$

Thus the VIS is a switch which periodically inverts its terminal voltage. It controls the pulse currents flowing in the SC circuit and prevents the operation of the switches in the simulated elements from causing charge flow.

The symbol given in fig. 7:15(a) is used for the VIS. A number of circuits have been given for the realisations of grounded VISs. The implementation in fig. 7:15(b) makes use of a voltage follower amplifier for voltage inversion.[14] When switches 1 are closed, the voltage across C_H becomes equal to the voltage, V_{v1} at the terminals. When switches 2 close, the voltage appearing across the terminals becomes $V_{v2} = - V_{v1}$.

The VIS in fig. 7:15(c) uses an integrator.[15] During 1, the output of the OA becomes $- \frac{C_T}{C_H} V_{v1}$ where C_T is the total capacitance of the network at the VIS terminals. During 2 the OA output is connected to the terminals. If $C_H = C_T$, voltage inversion is obtained as required. Switch 3 is required to initialise the VIS. The VIS in fig. 7:15(d) makes use of the principle of inverse recharging.[16] During 1, the terminal voltage is made zero, the charges are made to flow out from the network and are stored on C_H. During 2, the same charges are made to flow through the terminals in the same direction as during 1. This produces the voltage inversion at the terminals.

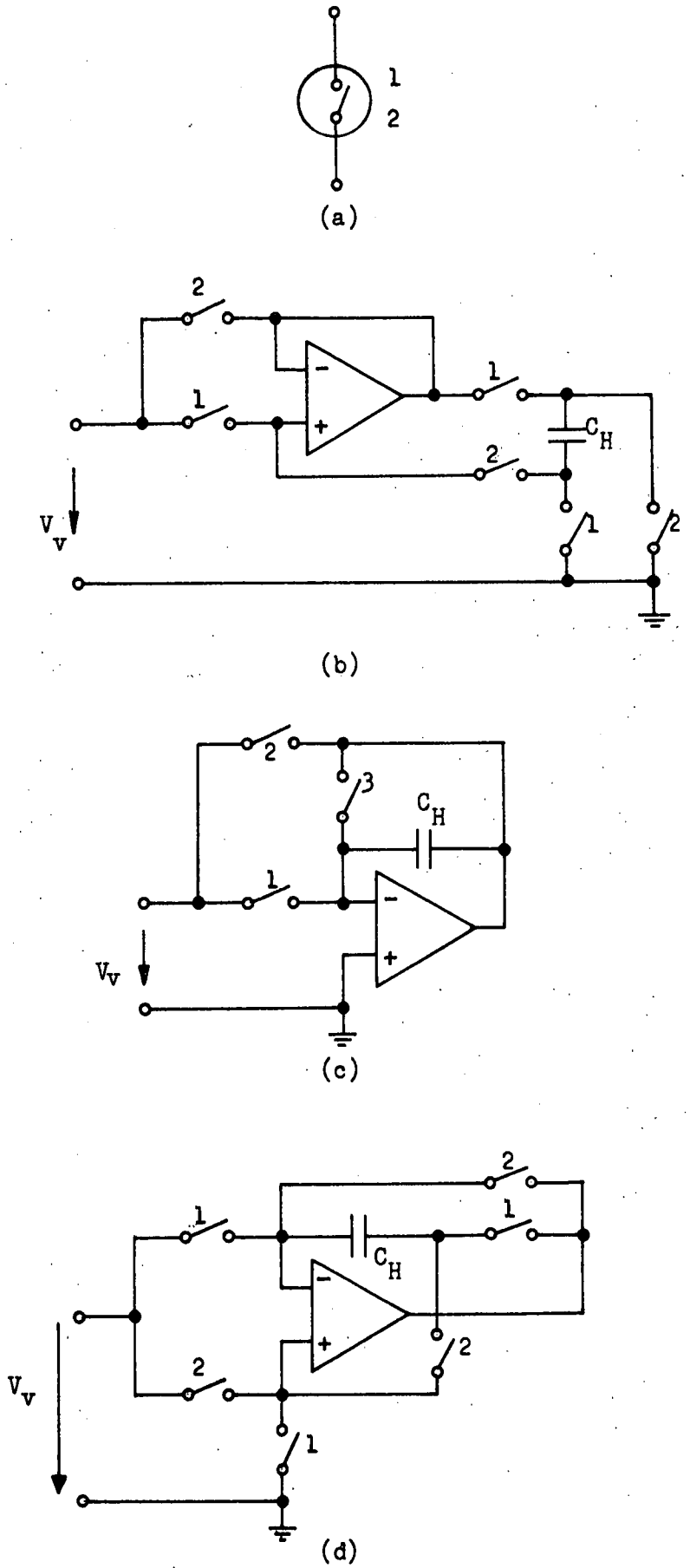


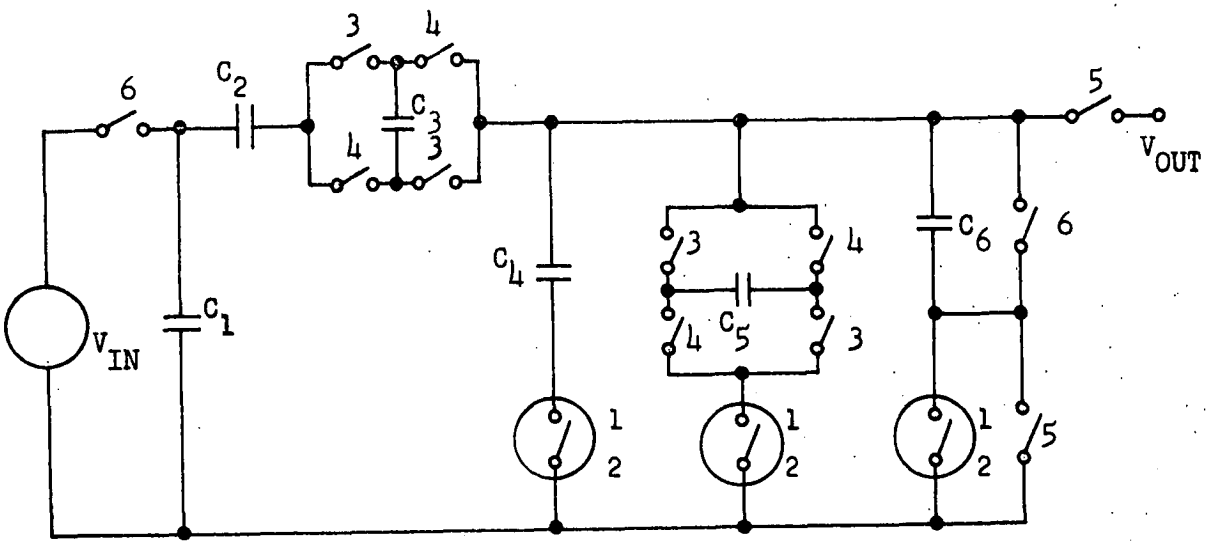
Fig. 7:15 (a) The VIS symbol. Realisations of the VIS using (b) a voltage follower amplifier, (c) an integrator and (d) the inverse recharging principle.

The ladder network for the OTOB filter in fig. 7:6(a) can be replaced by the elements of Table 7:1. This is shown in fig. 7:16(a) together with the necessary VISs. Fig. 7:16(b) shows the clocking scheme for the filter. If the integrator VIS is used, it can be initialised during 6. Switches 5 are added to sample the filter output across C_6. No 6dB loss is incurred in this case.

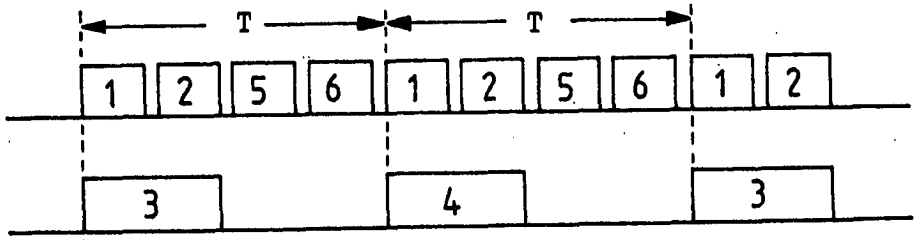
It can be seen that the SC realisation in fig. 7:16(a) is sensitive to both top and bottom plate parasitic capacitance. The number of OA is reduced to the number of required VISs. The complicated clocking scheme, however, increases the settling-time requirement of the OA. The influence of the bottom plate parasitic capacitance can be eliminated if all capacitors in the filter realisation are grounded directly or via VISs. This is possible through the use of unit elements as in Table 7:1 or by transforming floating elements into grounded ones.[17]

Grounding via VIS is possible if the integrator VIS in fig. 7:15(c) is used. The requirement that $C_H = C_T$ for voltage inversion, however, increases the sensitivity to the network element variations. This disadvantage can be overcome by using modified voltage follower or inverse recharging VIS but this method requires an amplifier for each reactive element in the circuit.[18]

Despite these modifications, the filter realisations using these VISs are still sensitive to top plate parasitic capacitance and usually require complicated clocking scheme. A few recently-proposed VIS circuits do allow the possibility for fully stray-insensitive realisation of filters with grounded elements.[19] These VISs make use of dynamic amplifiers [20] and their performance depends on the matching of capacitors. They also require more components than the circuits in fig. 7:15.



(a)



(b)

Fig. 7:16(a) A switched-capacitor realisation of the ladder in fig 7:6(a) using voltage inverter switches. (b) Its clocking scheme.

7.6 Summary

A few more design methods for SC ladder realisations have been described in this chapter. The realisation using VCCS can be made parasitic insensitive and the resultant circuit is similar to the coupled-biquad structure. When the scaled VCCS is used, it is possible to reduce the number of OAs but the filter becomes sensitive to the top-plate parasitic capacitance.

The possibility of simulating an inductor by SC circuit allows each element of the ladder network to be replaced directly by its corresponding SC equivalent. Only the inductors require OAs. The ladder network elements can also be replaced directly by passive SC circuits with the inclusion of the VIs in each critical loop. Both these realisations are sensitive to parasitic capacitances which can be overcome by the inclusion of additional components which in turn increases their sensitivity to element value variations.

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CHAPTER EIGHT

IMPLEMENTATION OF SWITCHED-CAPACITOR FILTERS

A number of considerations for designing and implementation of SCFs have been listed in chapter 1. Some of these have been noted when designing the SC OTOB filters in previous chapters. These considerations and a few other aspects of SCF implementation will be further discussed in this chapter. Particular reference is given to the possibility of implementing the SC OTOB filter with all its accessories on a single chip.

Among the filters designed in preceding chapters, the parasitic-insensitive realisations are most suitable for integration. Thus only these filters are further considered here. Their requirements under the various considerations are compared. Also, their performances are tested by implementing them using discrete circuits. From these, conclusions are made on circuits which can suitably be used to realise variable frequency OTOB filter in integrated form.

8.1 Antialiasing and Smoothing Filters

An antialiasing filter (AAF) is required at the input stage of an SCF to bandlimit its input signal. To avoid any external components, the continuous-time AAF has also to be realised on the same chip with the SCF. The Sallen and Key (S & K) section, designed to have a second-order Butterworth lowpass response, is usually used and is shown in fig. 8:1. The resistors are implemented by the polysilicon layer of the IC. The absolute value of the resistance formed in this way has large variation though the ratio of two resistors will generally track very closely. Thus the Q of the pole pairs of the AAF remains constant while its cut-off frequency, f_o varies with the resistance absolute value.[1]

The variation of f_o of the AAF imposes requirement for a higher clock frequency of the SCF. For the OTOB filter, if 0.15dB droop is allowed at $\sqrt[12]{2}f_m$ then the minimum f_o has to be about 2.5 f_m. Assuming 2:1 variation in the absolute value of the RC time constant [2], then the maximum f_o is $5.0f_m$. Thus f_c needs to be at least $160f_m$ so that the AAF has 60dB attenuation at $f_c - f_m$.

Furthermore, the f_m is variable between 10Hz and 20kHz. Thus it is desired that the AAF has enough attenuation at f_c for the 10Hz filter while not affecting the 20kHz filter. Hence the required f_c becomes extremely large compared to the f_m. One alternative is for a variable AAF to be employed on-chip but problems arise when large RC has to be realised for low f_o.

A better solution, however, is found with the application of a recently proposed circuit. An SC Decimator circuit is shown in fig. 8:2 with its timing diagram.[3] Its input signal is sampled at a higher frequency, nf_c and then integrated over C_o. The output is sampled by the following S/H circuit at the clock frequency, f_c after which C_o is short-circuited as shown in fig. 8:2. Adding the samples in this way results in the transfer function,

$$H(z) = \frac{C_1}{C_o} z^{-1/2n}\left[\sum_{i=o}^{n-1} z^{-i/n}\right] = \frac{C_1}{C_o} z^{-1/2n}\left[\frac{1 - z^{-1}}{1 - z^{-1/n}}\right] \qquad (8:1)$$

The magnitude response is given by

$$H(f) = \frac{C_1}{C_o}\left[\frac{\sin\pi f/f_c}{\sin\pi f/nf_c}\right] \qquad (8:2)$$

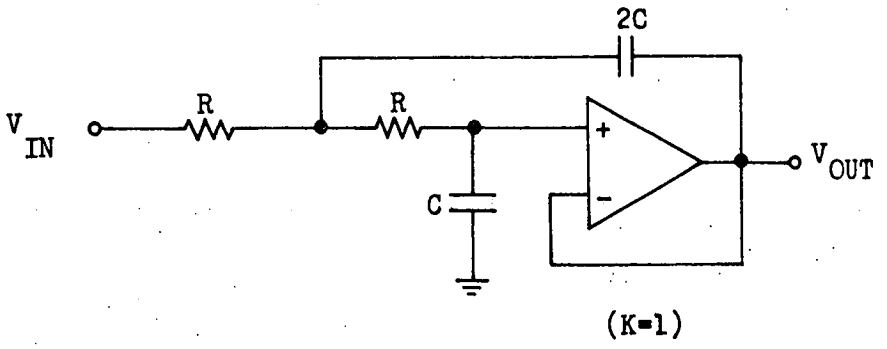
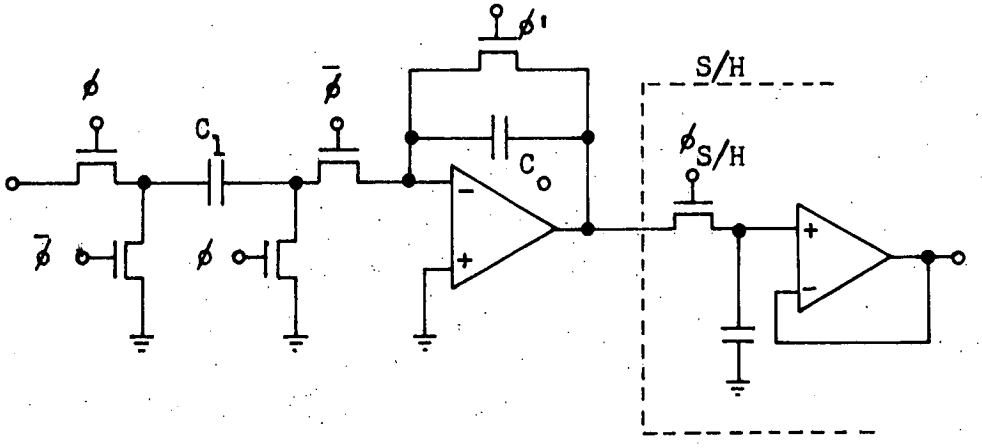
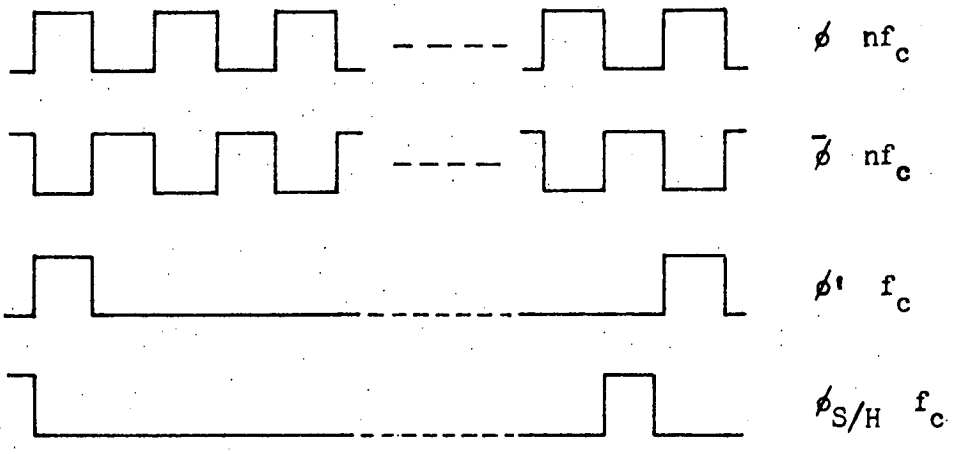


Fig. 8:1 Sallen and Key lowpass for antialiasing filter.



(a)



(b)

Fig. 8:2 (a) A switched-capacitor decimator circuit with a sample-and-hold circuit at its output. (b) Timing diagram.

which has zeros at integer multiples of f_c up to $(n-1)f_c$. Thus the decimator circuit (DEC) attenuates the input signal with frequencies around these multiples of f_c. The AAF which is now placed before the DEC is only required to attenuate the signal components at nf_c and above. The term in bracket in (8:2) has a dc gain of n.

The S/H circuit provides a full cycle S/H input to the SCF as required by circuits designed in previous chapters. Also, it provides further attenuation around the integer multiples of f_c. A suitable f_c can then be chosen for which the attenuations around its integer multiples up to $(n-1)f_c$ are all above 60dB. Choosing f_c = 48fm, the AAF needs only to have -26.6dB at 47fm after taking into account the effect of the S/H operation. Choosing a nominal f_o of 70kHz (R = 160kΩ, C = 10pF) the droop on the 20kHz filter will be less than 0.15dB, and 60dB total attenuation is achieved above 500kHz. Thus for f_c lower than 500kHz, the DEC is included.

The DEC is particularly suitable for the variable frequency OTOB filter since the values of n can be easily varied instead of varying the AAF. However, it is undesirable to have large n since the capacitor ratio C_1/C_o will be inaccurate. Thus it is necessary to have at least another AAF response with a lower f_o. This will require large values of R and C, and occupy a sizeable portion of the chip.

Table 8:1 gives one possible arrangement for providing sufficient prefiltering to the various f_m of the OTOB filter. The change in capacitor ratio corresponding to n can be effected by using a bivary-weighted capacitor array as used in [4]. Another possibility of avoiding large capacitor ratio C_1/C_o to achieve the required n is by cascading two DECs together.[5]

A smoothing filter (SF) is sometimes required at the output of an SCF to attenuate the residual high frequency component of its S/H output. The SF is usually implemented in the same way as for the AAF. Variable f_c such as for the OTOB filter can be accommodated, through the use of an interpolator circuit (INT) before the SF. The INT increases the sample rate of the S/H signal to nf_c and thus attenuating the residual frequency components around the lower integer multiples of f_c. This necessitates the SF to attenuate only the components around nf_c and above.

Table 8:1 Prefiltering arrangement for all the preferred midband frequencies of the OTOB filter as given in Table 4:2. $f_c = 48fm$.

f_c or nf_c (kHz) / f_m (kHz)		Antialiasing Filter Requirement f_o=70kHz(R=160k , C=10pF)			f_o=2.8kHz(R=800k , C=50pF)		
		960	768	608	30.5	24.2	19.2
Without Decimator		20	16	12.5			
n values for Decimator Circuit	2	10	8.0	6.3	0.315	0.25	0.20
	4	5.0	4.0	3.15	0.16	0.125	0.10
	8	2.5	2.0	1.6	0.080	0.063	0.050
	16	1.25	1.0	0.80	0.040	0.0315	0.025
	32	0.63	0.5	0.40	0.020	0.016	0.0125
	64				0.010		

An SC interpolator is shown in fig. 8:3 with its timing diagram.[6] The output of OA 1 is held at a value proportional to the SCF output voltage step. A charge proportional to this voltage is then fed into C_4 by C_3 n times before the output of OA 1 is updated. The capacitor ratios satisfy

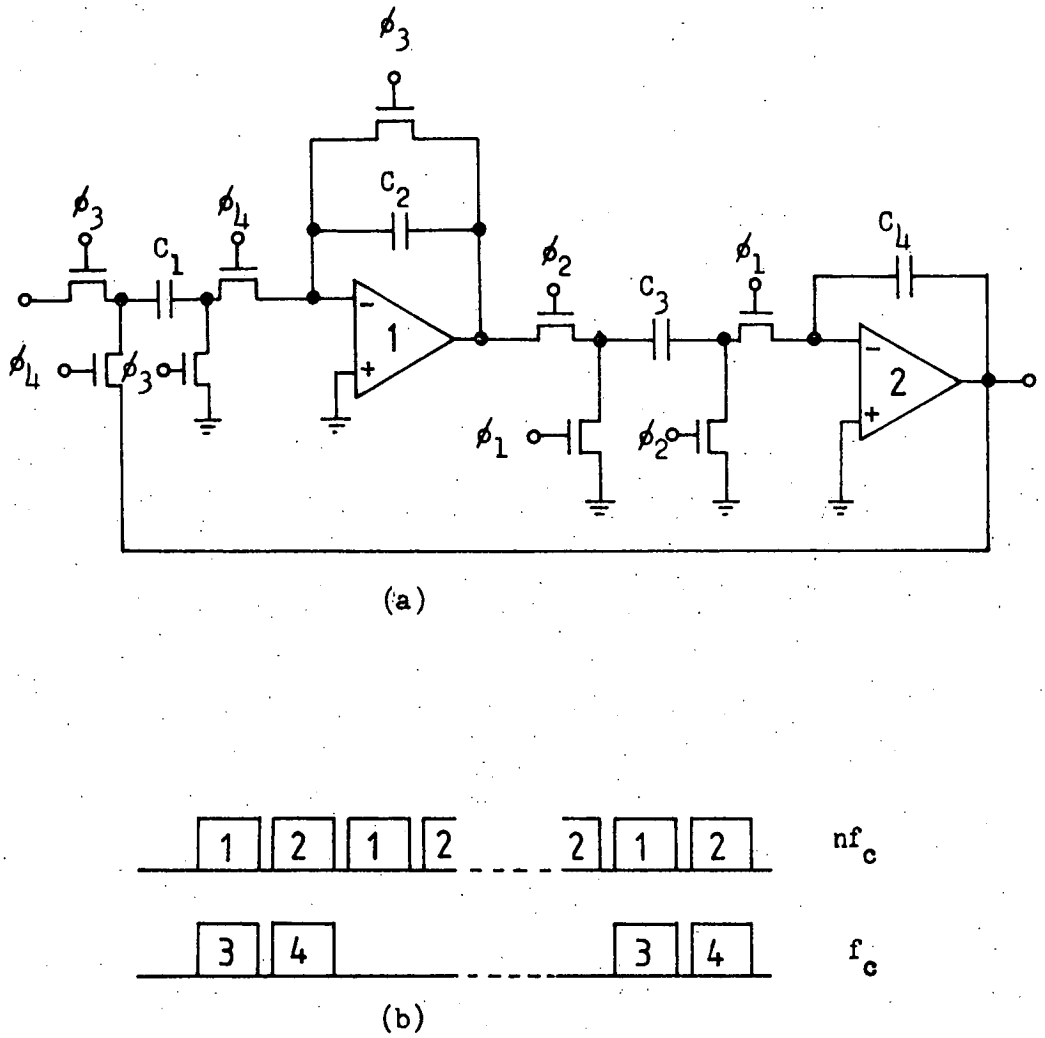


Fig. 8:3(a) A switched-capacitor Interpolator. (b) Its timing diagram.

$$\frac{C_2}{C_1} \cdot \frac{C_4}{C_3} = n \qquad (8:3)$$

Large n is thus possible, in this case, without excessive increase in the capacitor ratios.

8.2 Requirements on the MOS components

The maximum clock frequency required when using the arrangement in section 8.1 is 960kHz. This is now possible, and SCF clocked at 4mHz has been reported.[7] Since the circuits to be considered are parasitic insensitive, the capacitance values on-chip can be made as small as 0.1pF. Thus the effect of switch on resistance is still negligible at this high f_c. The OAs require unity-gain bandwidth of about 5mHz for its effect to be negligible as discussed in chapter 3. Fast MOS OA is now available without significant increase in power and area.[8]

The MOS OA settling time and slew rate, now achieved, are also sufficient at the required f_c. The OA of the DEC and OA 1 of the INT need more stringent settling time and slew rate properties due to their outputs being set to zero periodically. However, when using ± 5V supply voltages, the OAs such as in [8] can meet these requirements.

When implementing the SCF with discrete components, the capacitance level is increased significantly. The bandwidth of the OAs used are comparable to the above. In this case the RC due to the switch on-resistance and the maximum input switched-capacitor to the integrators usually determines the maximum allowable clock frequency.

8.3 Requirements of OTOB filter realisations

Table 8:2 lists out the requirements of the parasitic insensitive circuits realising the OTOB filter in chapters 5 and 6. The sensitivity of the filter to variation of a single capacitor value is calculated using λ in (1:3). Each capacitor is varied until the filter frequency response fails to meet the specification after allowing for droops caused by the AAF, SF and S/H responses. The frequency response is calculated using the minimum clock frequency possible for the filter.

The most and least sensitive capacitors for each circuit and their values for λ are given in Table 8:2. The most sensitive capacitors are marked (**) and the least by (*) on the circuit diagrams of the filters in chapters 5 and 6. Table 8:2 also lists the capacitance requirements and the capacitor spread of the filters at both the minimum clock frequency and f_c = 48fm. Other requirements listed are the number of capacitors and switches needed by the circuits.

The Table shows that the LDI ladder provides the least sensitive realisations while the coupled-biquad structure gives an improvement over the cascaded biquad circuits. However, these realisations require large capacitor spread and total capacitance especially with f_c = 48fm. The cascaded circuits are more sensitive but some realisations require significantly less capacitance and have less capacitor spread.

The increase in sensitivity of the cascaded circuits is not very drastic since, in this case, only two biquads are involved. It is still possible to implement them on a chip. This is considering that capacitors in integrated circuit generally track each other giving quite accurate ratios especially if the capacitor spread is small. Taking also the

Table 8:2 Comparison of Filter Requirements

Filter Circuit	Fig.	min. f_c	Sensitivity		Total Capacitance in pF		Capacitor spread		no. of capacitors	no. of switches
			λ(%)	Capacitors	min.f_c	f_c=48fm	min.f_c	f_c=48fm		
Cascaded BP10 (H1 Design)	5:8	$16f_m$	1.92-179	R_2C_{22}-A_2C_{12}	69.8	89.8	1:22.7	1:35.7	14	16
Cascaded BP10 (H2 Design)		$16f_m$	2.14-299	C_{11}-K_2C_{22}	106.0	215	1:40.1	1:118	14	16
Cascaded BP01 (H2 Design)	5:7	$48f_m$	1.90-13.4	E_2C_{12}-E'_2C_{12}		40.1		1:8.3	12	16
Cascaded HP-LP (H1 Design)	5:6	$16f_m$	1.93-56.2	R_2C_{22}-A_2C_{12}	56.7	282	1:14.2	1:119	14	18
LDI Ladder	6:7	$24f_m$	5.65-21.2	C_{LA}-$K_1'C_{LA}$	95.5	165.3	1:34.4	1:69.1	13	22
Coupled-Biquad	6:9	$16f_m$	3.13-176	C_{12}-$A_{IN}C_{11}$	115.5	182.0	1:29.5	1:86.2	16	16

antialiasing requirement into consideration, with f_c = 48fm, the cascaded BP01 circuit is the most economical realisation needing the least total capacitance and smallest capacitor spread.

All the circuits considered in Table 8:2 require four OAs and two-phase clocking scheme. This number is usually needed for a parasitic-insensitive fourth-order circuit. Reduction in the number increases its sensitivity to parasitic capacitance as shown in chapter 7 and also complicates the clocking scheme. Another possible method to reduce the number of OAs while retaining a two-phase clock is through time-sharing the integrator OAs in the biquad or the ladder circuit. The circuit, however, is still either sensitive to parasitic capacitance at some nodes [9], or that parasitic capacitances at two nodes are assumed matched as for the parasitic-compensated integrator of fig. 3:6.

8.4 Performance of SC OTOB filter

The circuits compared in Table 8:2 were implemented using discrete components. The CD4016 CMOS switches and TL084 quad JFET-input operational amplifiers were used. The capacitor values were chosen in the 100pF-10nF range. In implementing the cascaded circuits, the switched-capacitors determining the integrator gain constants have to be chosen accurately with the integrating capacitors to achieve the desired result. On the other hand, for the LDI ladder circuit, the capacitors were just chosen to within ± 1%.

Fig. 8:4 gives the gain response of the OTOB filter implemented by the LDI ladder circuit using discrete components with f_c = 48fm. The plot is made with f_c = 48kHz. Fig. 8:5 gives the passband on an expanded frequency scale. The figures show that the specification is met

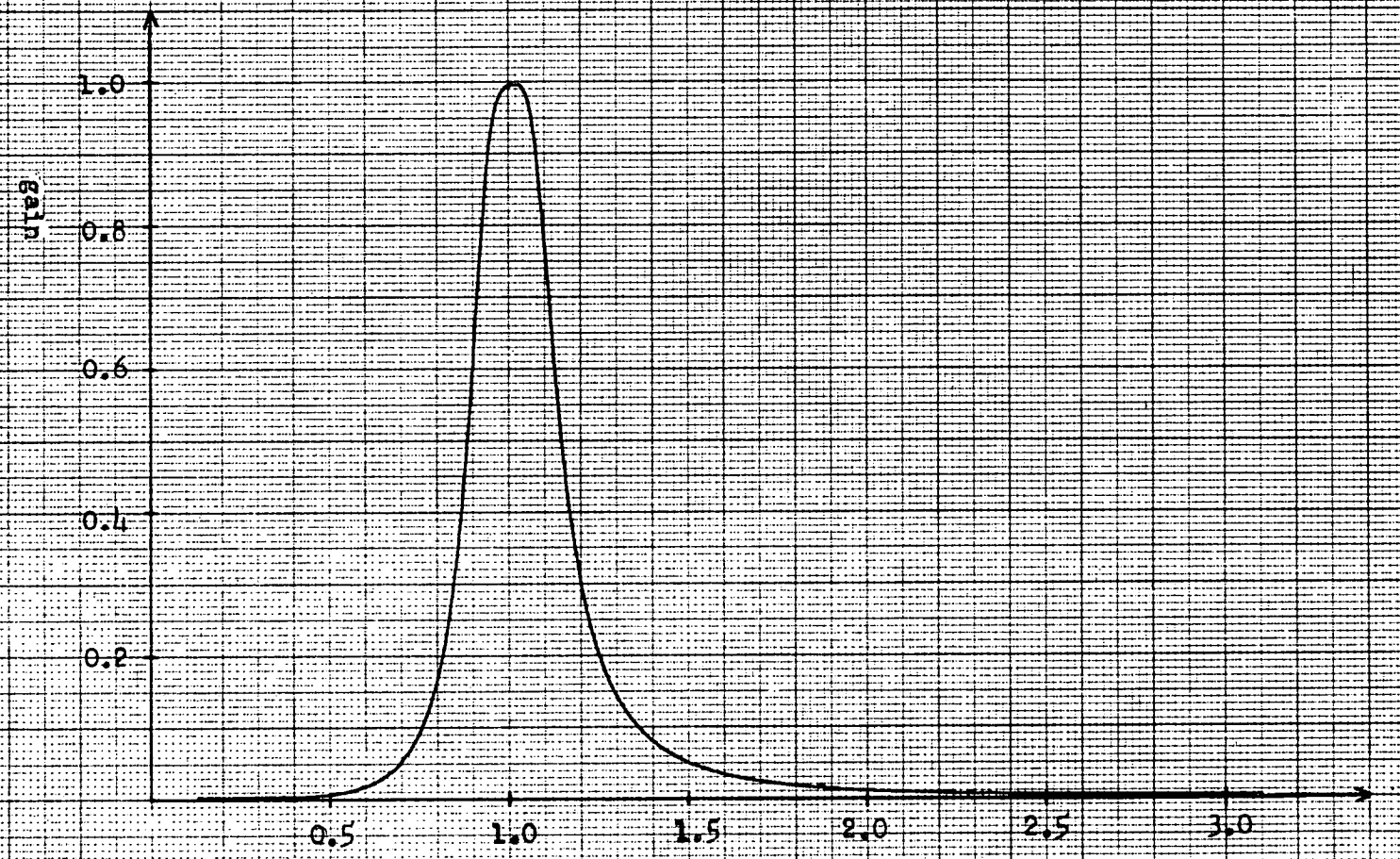


Fig. 8.4 Gain response of the OTOB filter implemented by the LDI ladder circuit, f_c = 48kHz.

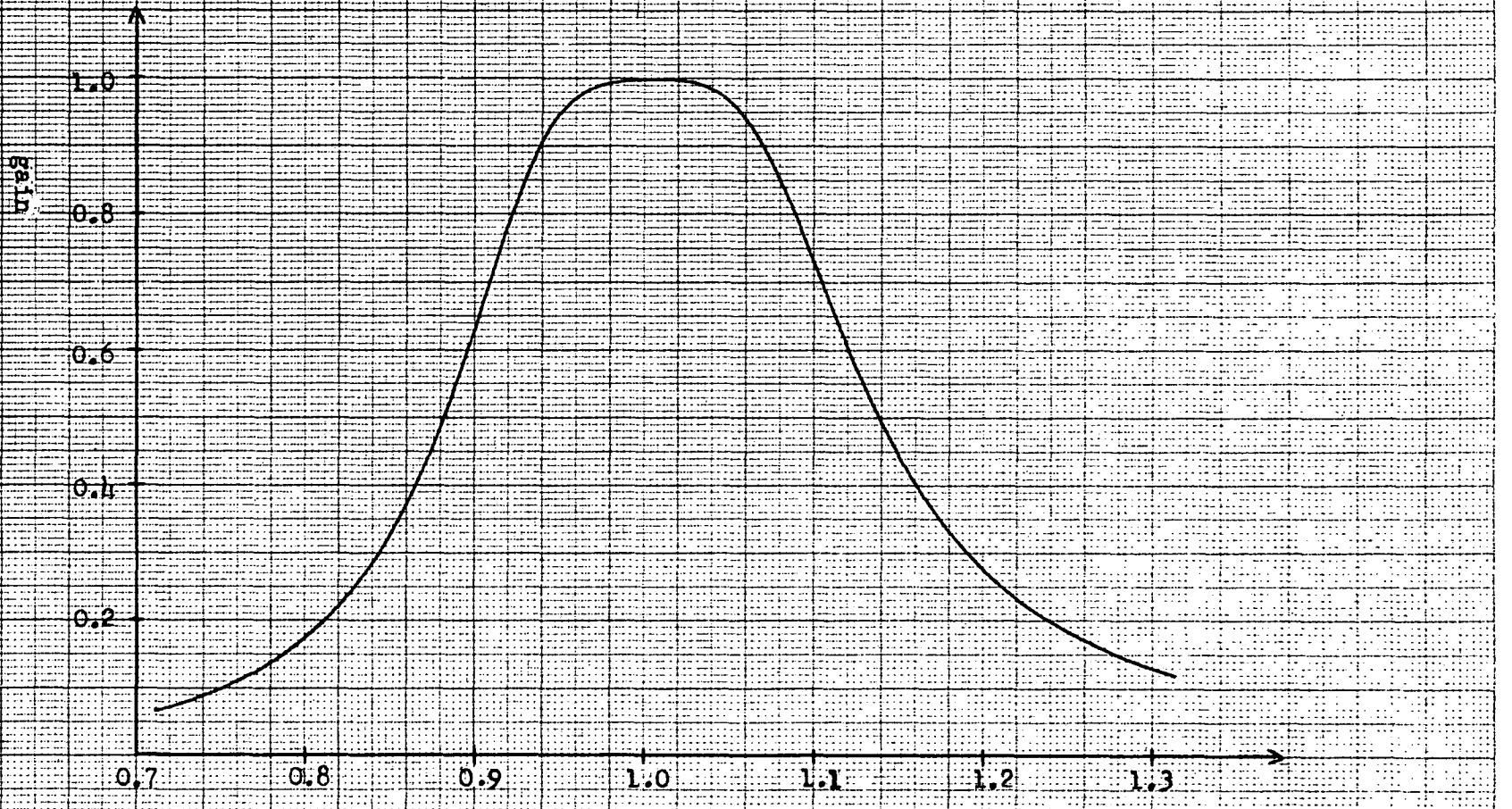


Fig. 8:5 Passband of the response in fig. 8:4 on expanded frequency scale.

satisfactorily with f_m = 1kHz achieved. Satisfactory results are also obtained for lower clock frequencies with similar performances achieved even for f_m = 10Hz. For higher frequencies, the results become unsatisfactory as the clock frequency exceeds 60kHz. These are due to the level of capacitance chosen being about 1nF for the maximum switched-capacitance.

The performance achieved as shown in fig. 8:5 is also typical of the other circuits. This is also the case when f_c = 24fm is used for the LDI ladder circuit and f_c = 16fm for the cascaded circuits except the cascaded BP01.

8.5 Conclusion

SCFs have been shown to be derivable through a number of design approaches. The designs which can suitably be considered for accurate implementation are mostly based on the parasitic-insensitive two-integrator loop such as shown in fig. 3:5. This integrator loop is used in the SC biquad circuits which can be cascaded or coupled to realise higher order filters. The LDI SC ladder circuit simulating the doubly-terminated LC ladder network also uses the two-integrator loop.

The LDI SC ladder circuit gives the least sensitive realisation though it requires more capacitance. The coupled-biquad structure overcomes the termination error present in the LDI ladder while retaining good sensitivity but its capacitance requirement is also large. Some cascaded biquad realisations, on the other hand, require very low total capacitance with increase sensitivity. The fourth-order circuit required by the OTOB filter, however, can sufficiently be realised by the cascaded biquads.

Insensitivity to parasitic capacitances and low sensitivity to element value variations enable SCFs implemented on-chip to be very accurate and reproducible. These have made the SC technique the most attractive in a number of applications. A wide range of interest in SCF design is pointing to further use of the technique in more applications.

The variable frequency OTOB filter for use in noise measurement and vibrational analysis requiring midband frequencies from 10Hz to 20kHz can also be implemented on chip. The problem of providing antialiasing response for the different midband frequencies can be overcome through the use of the SC Decimator circuit. SC Interpolator circuit can also be used to supplement the smoothing filter operation. These circuits, together with the digital control for varying the clock frequencies can all be implemented on the same chip as the SC OTOB filter.

High clock-to-midband frequencies ratio (f_c/f_m) is used for the OTOB filter to simplify its antialiasing requirement. This permits the use of the cascaded BP01 circuits. For higher frequency applications, when the highest clock frequency is reached, it is necessary to reduce the f_c/f_m. In this case, circuits based on the bilinear transformation are most suitable. If antialiasing filter is required, then higher order continuous-time filter need to be realised on-chip or that improvement be made on the variation of the on-chip resistors.

Developments in MOS operational amplifier fabrication allows the possibility for further increasing the clock frequency of the SCF while also decreasing its size. Thus video frequency applications for the SCF may soon be realised.

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APPENDIX A

TRANSFER FUNCTION OF SWITCHED-CAPACITOR INTEGRATOR WITH FINITE OPERATIONAL AMPLIFIER BANDWIDTH

The derivations of the transfer functions for the integrators in fig. 3:5 including the effects of finite OA bandwidth given here follow those shown in [A1]. It is assumed that a step input is applied to the OA and the output is sampled one half-clock period later. The non-inverting integrator 1 in fig. 3:5 is redrawn here in fig. A:1(a) with V_a grounded. The clock timing of fig. 1:2(b) is redrawn in fig. A:1(b).

Neglecting p_o in (3:15), the OA transfer function can be written as

$$A(j\omega) \simeq \frac{\omega_t}{j\omega} = \frac{V_d(\omega)}{V_1(\omega)} \qquad \text{(A:1)}$$

This can be expressed in the time domain as

$$\frac{dv_d(t)}{dt} = -\omega_t v_1(t) \qquad \text{(A:2)}$$

Thus although $v_1(t)$ can be discontinuous at the switching instants, the output signal $v_d(t)$ will be continuous. Fig. A:1 shows that $v_1(t)$ will be discontinuous at $t = (n-\frac{1}{2})T$. At this instant, capacitor C_3 is connected to the negative input of the OA and charge on C_3 is instantaneously distributed between C_3 and C_4 according to

$$v_1(n-\tfrac{1}{2})^+ = Kv_1(n-\tfrac{1}{2})^- - (1-K)v_b(n-\tfrac{1}{2}) \qquad \text{(A:3)}$$

where $K = C_4/(C_3 + C_4)$ and, $v_1(n-\frac{1}{2})^-$ and $v_1(n-\frac{1}{2})^+$ refer to v_1 before and after the discontinuity respectively.

The analysis then considers the transients during clock phases, ϕ_e and ϕ_o as in (3:16) and (3:18) but now assumes all resistances to be zero. During ϕ_o,

$$v_d(t) - v_d(n - \tfrac{1}{2}) = \frac{1}{K}[v_1(t) - v_1(n - \tfrac{1}{2})^+] \qquad (A:4)$$

Differentiating (A:4) gives

$$\frac{dv_d(t)}{dt} = \frac{1}{K}\frac{dv_1(t)}{dt} \qquad (A:5)$$

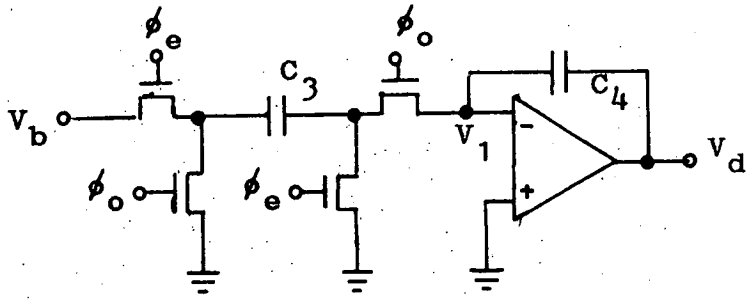
Substituting (A:5) in (A:2) and solving results in the value of v_1 at $t = nT$ as

$$v_1(n) = v_1(n - \tfrac{1}{2})^+ \exp(-k_1) \qquad (A:6)$$

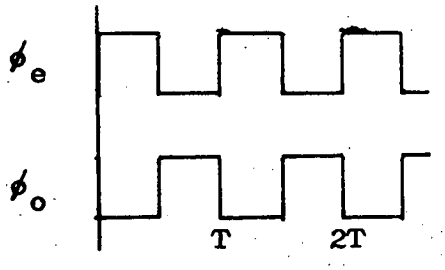
where $k_1 = K\omega_t T/2$. Putting (A:6) in (A:4) gives

$$v_d(n) = v_d(n - \tfrac{1}{2}) - \frac{1}{K}(1 - \exp(-k_1))v_1(n - \tfrac{1}{2})^+ \qquad (A:7)$$

During ϕ_e,



(a)



(b)

Fig. A:1 (a) Non-inverting switched-capacitor integrator.
(b) Timing diagram.

$$\upsilon_d(t) - \upsilon_d(n-1) = \upsilon_1(t) - \upsilon_1(n-1) \qquad (A:8)$$

and following in a similar manner as above,

$$\upsilon_1(n-\tfrac{1}{2})^- = \upsilon_1(n-1)\exp(-k_2) \qquad (A:9)$$

where $k_2 = \omega_t T/2$. Putting (A:9) in (A:8)

$$\upsilon_d(n-\tfrac{1}{2}) = \upsilon_d(n-1) - (1-\exp(-k_2))\upsilon_1(n-1) \qquad (A:10)$$

If the output, υ_d is sampled at $t = nT$, then using (A:3), (A:9) and (A:10) in (A:7),

$$\upsilon_d(n) = \upsilon_d(n-1) + \frac{(1-K)}{K}(1-\exp(-k_1))\upsilon_b(n-\tfrac{1}{2}) - [1-\exp(-k_1-k_2)]\upsilon_1(n-1) \qquad (A:11)$$

Also, using (A:3) and (A:9) in (A:6)

$$\upsilon_1(n) = K\exp(-k_1-k_2)\upsilon_1(n-1) - (1-K)\exp(-k_1)\upsilon_b(n-\tfrac{1}{2}) \qquad (A:12)$$

From the z-transforms of (A:11) and (A:12), the transfer function, H^{oe} of the non-inverting integrator can then be solved as,

$$\frac{V_d^e(z)}{V_b^o(z)} = \frac{C_3}{C_4}\,\frac{z^{-\frac{1}{2}}}{1-z^{-1}}\left[\frac{1 - [1-Kz^{-1}(1-\exp(-k_2))]\exp(-k_1)}{1 - Kz^{-1}\exp(-k_1-k_2)}\right] \qquad (A:13)$$

The transfer function, H^{oo} when the output is sampled one clock period after the discontinuity can also be solved from the above. This is given by [A2],

$$\frac{V_d^o(z)}{V_b^o(z)} = \frac{C_3}{C_4}\,\frac{z^{-1}}{1-z^{-1}}\left[\frac{1 - [1-K(1-\exp(-k_2))]\exp(-k_1)}{1 - Kz^{-1}\exp(-k_1-k_2)}\right] \qquad (A:14)$$

The magnitude errors of both transfer functions are approximately equal.[A1] Thus it is reasonable to assume that υ_d is constant during ϕ_e.

With this assumption, the inverting integrator 2 in the loop of fig. 3:5 can also be analysed using similar procedures as for obtaining (A:13). In this case, $v_1(t)$ is discontinuous at $t = (n-1)T$ and the output, v_b is sampled at $t = (n-\frac{1}{2})T$. The transfer function H^{eo} has the same expression as given in (A:13) except that it has a negative sign.

Note that the loop of fig. 3:2 does not require the assumption that the integrator output is constant during any of the clock phases for the above analysis to be used.

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